Class 1 bluetooth power amplifier with 24dBm output power and 48% PAE at 2.4GHz in 0.25um CMOS

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Abstract

In this paper, we report an RF power amplifier design in digital CMOS technology for the Class 1 power level specification (20 dBm) in the Bluetooth Communications standard. We have also investigated hot carrier effects under large signal RF operation of the power amplifier. The two stage circuit, designed in 0.25 μm CMOS technology, utilizes a high-density ring capacitor structure for interstage matching. In a chip-on-board configuration tested at 2.4 GHz, this CMOS power amplifier delivers an output power of 24 dBm with 48% PAE at a supply voltage of 2.5V.

1. Introduction

The Bluetooth communications protocol is widely perceived as the de facto standard for WLAN applications in the future. Class 1 (20 dBm), Class 2 (4 dBm) and Class 3 (0 dBm) are three classes of transmitter power requirements in this protocol based on the signal transmission distance. The low radio power requirements for this protocol have prompted heavy research interest in the area of using CMOS to implement the various RF component blocks required [1-2]. This will result in the ability to integrate both the baseband and RF functionalities using a single CMOS technology and produce a one-chip transceiver solution for Bluetooth applications.

Although commercial single chip transceiver solutions have recently been demonstrated using CMOS at 2.4 GHz [3-4], they have not addressed the Class 1 power requirement for the standard. Therefore, a second power amplifier chip is necessary to complete the requirements for this class in the Bluetooth standard.

In this paper, we demonstrate a CMOS RF power amplifier capable of meeting the requirement specifications of the Bluetooth Class 1 standard. Since Bluetooth employs a constant envelope modulation scheme, we have focused on achieving the required high saturated power while maximizing Power Added Efficiency (PAE). In Section 2, we discuss the details of the circuit design and layout issues for this power amplifier. Experimental results and discussion are provided in Section 3, followed by a brief conclusion in Section 4.

2. Circuit Design and Layout

We have employed a single-ended two-stage common-source topology with on-chip interstage matching for the design of our power amplifier (Fig. 1). For accurate simulation purposes, we have used MOS transistor models developed specifically at Philips for use at high frequency and low supply voltages [5]. The "RF" transistor model which includes gate resistance, source and drain resistance and substrate resistance effects is developed around the Philips MM9 model core.

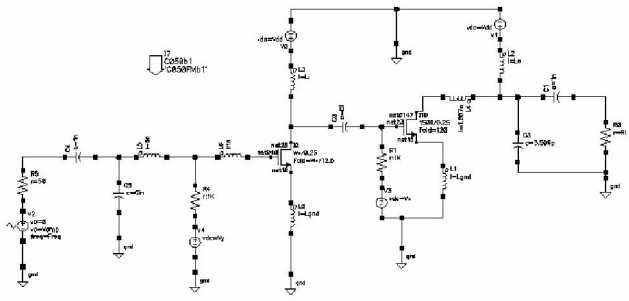

Figure 1. Class AB power amplifier schematic

A 1.5mm output stage biased close to class A region has been used along with a 0.5mm driver biased in deep class AB region for achieving the required output power of 24 dBm at 2V supply. In this design enough headroom has been allotted from the supply voltage limit of the technology (2.5V) to allow for process/chip assembly variations and achieve our goal of attaining more than 23 dBm saturated output power with a gain of 20 dB and an associated PAE of more than 45%. Meeting the above specification would allow direct interface on the same chip to the 0 dBm transceiver to

meet the Class 1 transmission requirements. For a cost effective solution, we have minimized the number of off-chip components and also avoided a flip-chip configuration. The ground inductance on the MOSFET sources due to the bond wires was set at an achievable value of 0.2 nH for both stages while performing these simulations. Resistive gate biasing is adopted to prevent unwanted oscillations. We have used the bondwire inductance for the driver stage drain connection along with an on-chip ring capacitor structure (details outlined in section 3) to provide the interstage matching. Input and output matching was done using lumped element components for simulation purposes.

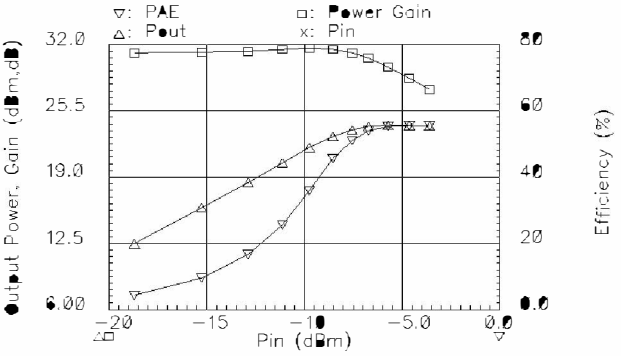

Figure 2. Simulated PA performance w/o parasitics

The simulated performance of this two stage design at 2V supply voltage is shown in Fig. 2. The design can provide 31.5 dB of small-signal gain and a saturated power of 24 dBm can be obtained with 55% PAE.

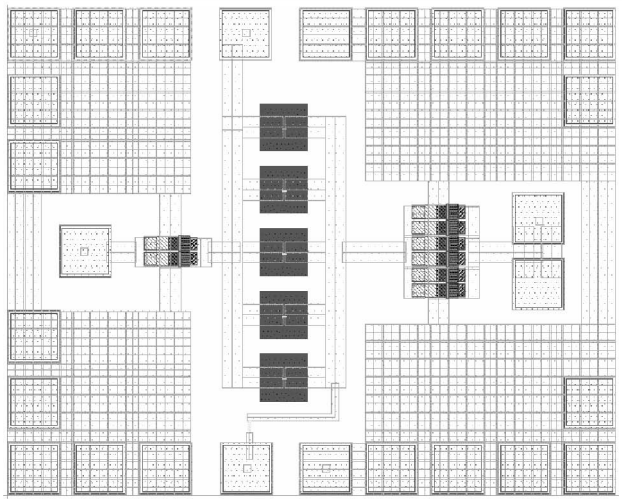

Figure 3. Layout of the power amplifier chip

The layout of the chip is shown in Fig. 3. Both the driver and output stages have been built up from a 20 finger interdigitated unit cell of width 250 μm resulting in a gate finger length of 12.5 μm. The substrate is tied to the source of the unit cell to prevent any substrate bias effects. The RF signal path is kept as short as possible between the stages and multiple ground pads are used to minimize the ground inductance from bondwires for the stages. The 10 pF interstage matching capacitance has been formed with five 2 pF unit capacitors which have a ring shaped structure to minimize occupied chip area (Fig. 4). The ring capacitor utilizes both the cross-over capacitance and the fringe capacitance between multi-level interconnect metals in minimum geometry configurations in our CMOS technology to achieve a high capacitance density (2-3X) compared to the conventional metal-sandwich structure [6].

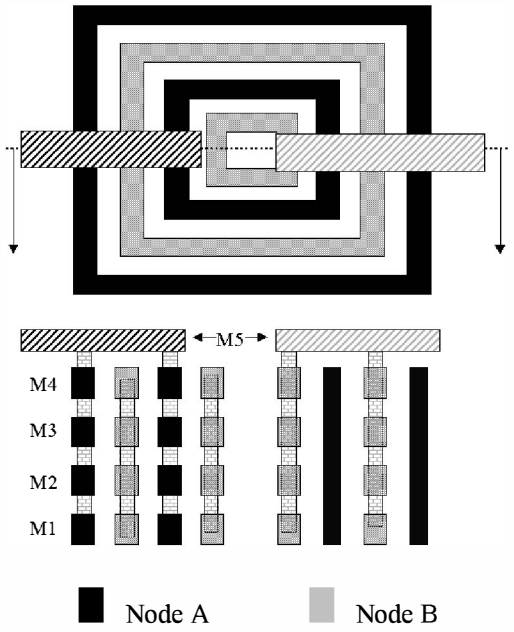

Figure 4: Ring Capacitor top and side view

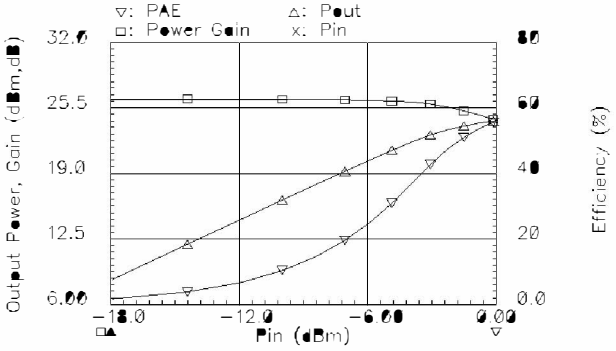

Figure 5: Post-Layout Circuit performance

Post-layout simulation results, which include the effect of parasitic capacitances extracted from the layout are shown in Fig. 5. As seen from this figure, the most

prominent effect of the parasitics is a degradation in the small signal gain by almost 5 dB due to extra gate-drain capacitance for the two stages from the layout. However, the original saturated power and PAE can still be obtained using a higher input level.

3. Results and Discussion

3.1 Large signal Measurements

The power amplifier was fabricated in a five metal level 0.25 µm low resistivity substrate (0.01 Ohm-cm) CMOS process at the Philips MOS4YOU facility at Nijmegen, Holland. The silicon was thinned down to 280 µm to help reduce the ground bondwire lengths. The die was then bonded to the PCB using a conducting glue which also provides a well defined ground to the backside of the chip. Bond wires were used to connect the bondpads to the respective traces on the PCB as shown in Fig. 6.

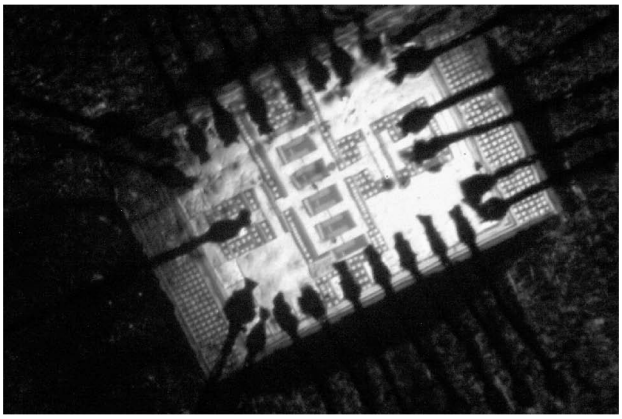

Figure 6. Photograph of Chip on Board Assembly

Large signal loadpull measurements were then performed on the power amplifier using an automated passive loadpull system. Fig. 7 shows the measured output power and gain at 2.4 GHz for the power amplifier as a function of the input power level for three supply voltage levels. It can be seen that the saturated output power of 22 dBm for a supply voltage of 2V is about 2 dB lower than simulated results with an associated PAE of 46%. We believe that the above is due to a higher than designed value for the drain bondwire inductance of the driver along with a slightly undersized driver stage which results in a larger than expected power gain drop-off. Both of these shortcomings can be easily remedied by a simple redesign of the PCB and an increase in the size of the driver stage. For the current design, at a supply voltage to 2.5V, we can achieve a saturated output power of +24 dBm. The output stage and the driver draw supply currents of 184 mA and 28 mA respectively at this output power level resulting in an associated PAE (which is the same as the total drain efficiency since the gain of the circuit is > 20 dB) of 48%. A plot of the saturated output power and the associated PAE shown in Fig. 8 as a function of the supply voltage indicates that we can achieve our power amplifier performance goals at 2.25V supply.

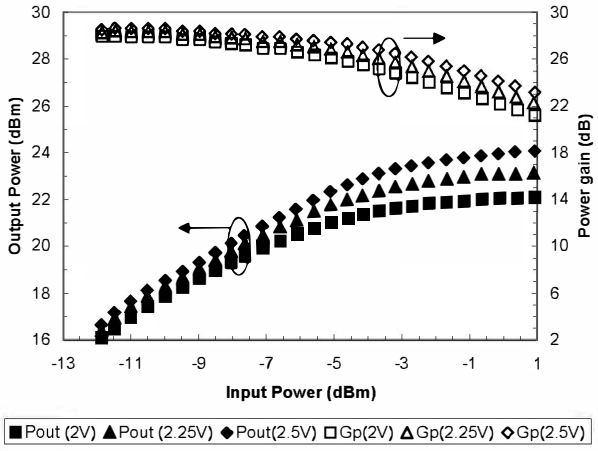

Figure 7. Measured Output power and power gain

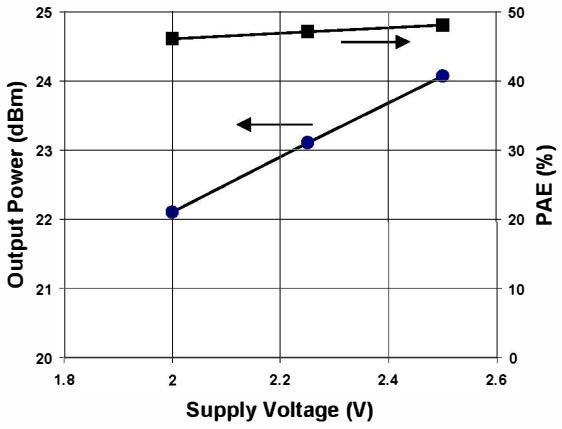

Figure 8. P_{out} and PAE versus supply voltage

3.2 Hot carrier induced degradation study

Issues of significance in the area of RF CMOS power amplifier design include catastrophic gate oxide breakdown (6V for 0.25 µm CMOS) and the effect of hot carrier induced device degradation on the RF performance of the amplifier. The hot carrier effect is a phenomenon where under high electric fields near the drain, the channel electrons can cause damage to the Si-SiO_2 interface thereby increasing threshold voltage, decreasing transconductance and degrading MOSFET

performance. Unlike gate breakdown, which is a catastrophic phenomenon, the hot carrier effect is a reliability issue and affects the long term power amplifier performance. So far, CMOS RF power amplifier papers have only considered the issue of gate breakdown and not the hot carrier effect even though they are operated at DC+RF voltage levels exceeding the recommended DC limit for hot carrier reliability [7-8]. Although DC/transient reliability testing has been performed to study hot carrier induced degradation [9-11], there have been no studies on hot carrier effects under large signal steady state RF operation in CMOS.

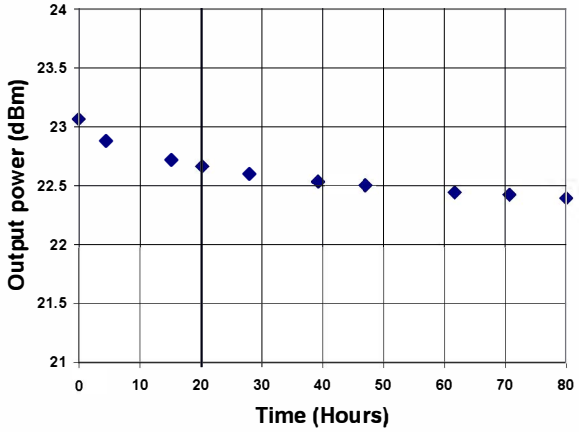

Figure 9. RF Hot Carrier reliability measurement

In this paper, we study the effect of hot carriers on the saturated output power of the designed power amplifier. The supply voltage limit for this technology from a hot carrier standpoint is 2.5V DC. We operated our power amplifier at Vdd=2.25 V to deliver 23 dBm initial output power. However, under saturated large signal operation, the instantaneous RF voltage swing at the drain of our transistor can reach upto 4.5V (2Vdd), well exceeding the DC limit for this technology.

As seen from Fig. 9, the output power of the amplifier decreases with an exponential time constant indicative of classical hot carrier degradation and the slope of the decrease becomes quite small after about 70-80 hours of testing suggesting that most of the created trap sites at the interface have been filled by electrons. The original performance can be recovered by increasing the gate bias (0.2V to get Pout=22.9 dBm, PAE=46.5%) to the two stages indicating that the degradation is mainly due to an increase in threshold voltage of the MOSFETs.

4. Conclusions

We have presented a Class 1 Bluetooth RF power amplifier design in 0.25 μm CMOS technology, which delivers a saturated output power of 24 dBm with an associated PAE of 48% at 2.4 GHz and 2.5 V supply.

The design incorporates a high density ring capacitor structure for the interstage matching network to minimize chip area. Preliminary hot carrier reliability measurements suggest that when the devices are operated at instantaneous RF+DC voltage levels exceeding the DC supply voltage limit imposed by hot carrier concerns, there is an exponential decay of the output power, which settles to a slightly lower value after 70-80 hours of testing. Therefore, hot carrier induced reduction in output power has to be taken into consideration while designing power amplifiers in submicron CMOS.

Acknowledgements

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References

[1] M. Madihian, L. Desclos, T. Drenski, Y. Kinoshita, H. Fujii and T. Yamazaki, "CMOS RF ICs for 900MHz-2.4GHz Band Wireless Communication Networks", IEEE RFIC Symposium, 13-16, 1999.

[2]F. Behbahani, J. C. Leete, Y. Kishigami, A. Roithmeier, K. Hoshino and A. A. Abidi, "A 2.4 GHz low-IF receiver for wideband WLAN in 0.6 μm CMOS. I. Architecture and front-end circuits", Microelectronic Engineering, V54, N1-2, 63-71, 2000.

[3] Signia Technologies, www.signiatech.com.

[4] Ericsson, www.ericsson.com/bluetooth.

[5] A. Scholten, L. Tiemeijer, S. Onneweer and D. Klaassen, "MOS Model 9-base macromodels for RF CMOS Circuit Design", Philips NL-Rep. 7125, 2000.

[6] T. Sowlati, V. Vathulya and D. Leenaerts, "High Density Capacitance Structures in submicron CMOS for RF applications", To be presented at ISLPED 2001.

[7] K. Tsai and P. Gray, "A 1.9 GHz, 1W- CMOS Class-E Power Amplifier for Wireless Communications", IEEE Journal of Solid State Circuits, V34, N7, 962-970, 1999.

[8] T. Kuo and B. Lusignan, " A 1.5W Class-F RF Power Amplifier in 0.2 μm CMOS Technology", 154-155, IEEE ISSCC'2001.

[9] E. Takeda and N. Suzuki, "An Empirical Model for device Degradation due to Hot carrier Injection", IEEE Electron Device Letters, EDL-4, 111-, 1983.

[10] J. Choi, P. Ko and C. Hu, "Hot Carrier–Induced MOSFET Degradation: AC versus DC Stressing", VLSI Technology Symposium Digest, 45-, 1987.

[11] W. Weber, C. Werner and A. Schwerin, "Lifetimes and substrate currents in static and dynamic hot carrier degradation", IEDM Technical Digest, 390-, 1986.