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Analysis of 60 GHz Flip-Chipped Package Using EM Tool-based Time-Domain Reflectometry

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Abstract—A systematic approach based on 'package-peeling' together with time-domain reflectometry (TDR) for package characterization using an EM-tool is presented. The said methodology is applied to investigate and address the possible causes of transmission losses for a measured 60 GHz flip-chipped package, embedding a power amplifier (PA) and a balanced-fed-aperture-coupled-patch (BFACP) antenna with an anisotropic conductive adhesive (ACA) flip-chip interconnection scheme. The proposed technique caters for TDR measurement system limitations and aids in investigation and improving the performance of the millimeter-wave flip-chipped packages.

I. INTRODUCTION

The 60 GHz frequency band has inspired next-generation wireless broadband communication, due to an availability of around 9 GHz unlicensed bandwidth. However, the realization of a single integrated package, comprising antennae and IC, is an important issue for the success of low-cost 60 GHz applications like wireless gigabit ethernet, wireless HDTV, telecom backhaul, etc.

The interconnection between IC and antenna-on-substrate is usually accomplished using wire or flip-chip bonding. The flip-chip interconnection provides better electrical behaviour, due to smaller electrical size and controllable relevant parameters. However, the flip-chip integration puts an IC in the close proximity of the substrate, which may affect the performance of an integrated package. Different schemes for characterization of flip-chipped packages, mostly relying on measurement-based-extraction, are found in literature. The flip-chip interconnect characterization via non-destructive *In Situ* measurement [1] requires accurately known programmable on-chip terminations, that need to be measured on-wafer as an initial step before flip-chip mounting. The results are reported up to 40 GHz because the sensitivity of the reconstructed scattering parameters depends strongly on the impedance separation of the integrated on-chip terminations. The approach based on extraction of de-embedded interconnect properties [2] does not (accurately) take into account EM-field coupling effects. Moreover, the said method is based on measurement of S-parameters for the chip (requiring identical on-chip probe pads and on-chip flip-chip pads), which is too restrictive in practice. A time-domain package characterization till 65 GHz is reported in [3]; a spatial-resolution l_{min} (the minimum resolvable distance between two discontinuities) of 600 μm (effective dielectric constant $\epsilon_{eff} = 4$) has been achieved with an incident pulse rise-time T_{rise} of 8 ps. The TDR system

rise-time and ϵ_{eff} determine the spatial resolution of the measurement set-up and is given by $l_{min} = \frac{c_0 T_{rise}}{2\sqrt{\epsilon_{eff}}}$. Moreover, the overall rise time of the TDR measurement system depends on the TDR pulse rise-time, the sampler rise-time and the instrument time-base jitter. The expensive state-of-art Electro Optical Terahertz Pulse Reflectometry (EOTPR) measurement set-up has achieved an overall system rise-time of 5.7 ps [4].

An alternative to the afore-mentioned package characterization schemes is proposed in this paper. The methodology uses 'package-peeling' approach together with TDR (Time-Domain Reflectometry) for investigation of flip-chipped packages, using the commercially-available CST MWS tool. In comparison with S-parameter simulations, a more intuitive and direct look at the flip-chipped package build-up is made possible using the proposed approach. A fast incident pulse rise-time T_{rise} of 0.876 ps can be achieved corresponding to 1 THz frequency band, which is well-suited for evaluating the impedance profile along a TEM or similar structure. Although some pulse-spreading due to dispersion is encountered for flip-chip packages, the location and value of impedance discontinuity can be estimated. The determination of cause of impedance discontinuity using 'package-peeling' approach aids in improving the performance of the millimeter-wave flip-chipped packages.

Section II highlights the details and measurement results of a 60 GHz flip-chipped package prototype that will be used as a case-study for the proposed approach. An investigation of the possible causes of transmission losses for a measured 60 GHz flip-chipped package using the proposed methodology is described in Section III. Section IV presents the effect of conductive and dielectric losses on TDR/TDT (Time-Domain Reflectometry/Time-Domain Transmission) response. Finally, the conclusions are drawn in Section V.

II. 60 GHz FLIP-CHIPPED PACKAGE

The prototype embeds a power amplifier (PA) and a balanced-fed-aperture-coupled-patch (BFACP) antenna into one package with an anisotropic conductive adhesive (ACA) flip-chip interconnection scheme, as shown in Fig. 1a inset [5], [6]. A microscopic photograph of the cross-section of an anisotropic conductive adhesive (ACA) flip-chip interconnection is shown in Fig. 1b. The PA is realised in 65 nm CMOS technology and is initially characterized with RF probes that connect directly to the chip. The maximum gain of the PA is
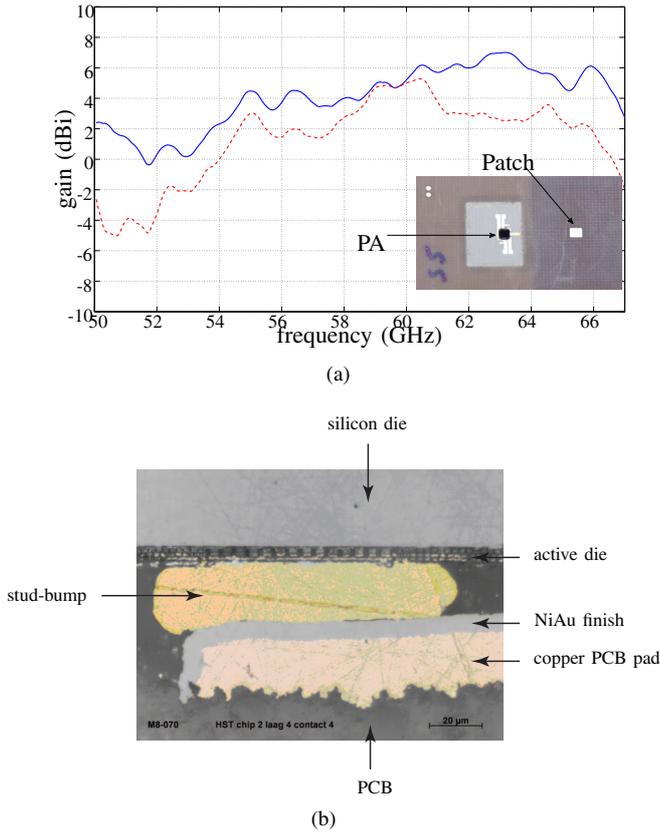
(a)

(b)

Fig. 1: (a) Measurement results of boresight gain of the packaged BFACP antenna with flip-chipped PA, including the power gain of the active PA (dashed-red), and without PA (solid-blue); [Inset] Photograph of flip-chipped PA and BFACP antenna package, (b) Microscopic photograph of the cross-section of a ACA flip-chip interconnection.

about 5-8 dB and the 3 dB gain bandwidth ranges from 54 to 66 GHz. A comparison of boresight gain of the packaged BFACP antenna with flip-chipped PA, including the power gain of the active PA, and without PA is made in Fig. 1a. It is observed that the gain of the former is 0-4 dB lower than the gain of the latter in the operating range of the antenna (57.7 - 65.0 GHz). This implies that the RF losses are equal or larger than the gain of the packaged PA.

III. EM-Tool Based TDR Analysis

This section presents 'package-peeling' approach to investigate the 60 GHz flip-chipped package using Time-Domain Reflectometry (TDR). The said methodology is applied to investigate and address the possible causes of transmission losses for the 60 GHz flip-chipped package. CST MWS tool is used for this analysis.

A. Setting-up 60 GHz flip-chipped package in CST MWS

In order to address the possible causes of transmission losses for the 60 GHz flip-chipped package, it is desirable to set-up a simulation which is not only close to real situation but also within the computational capability of the simulation
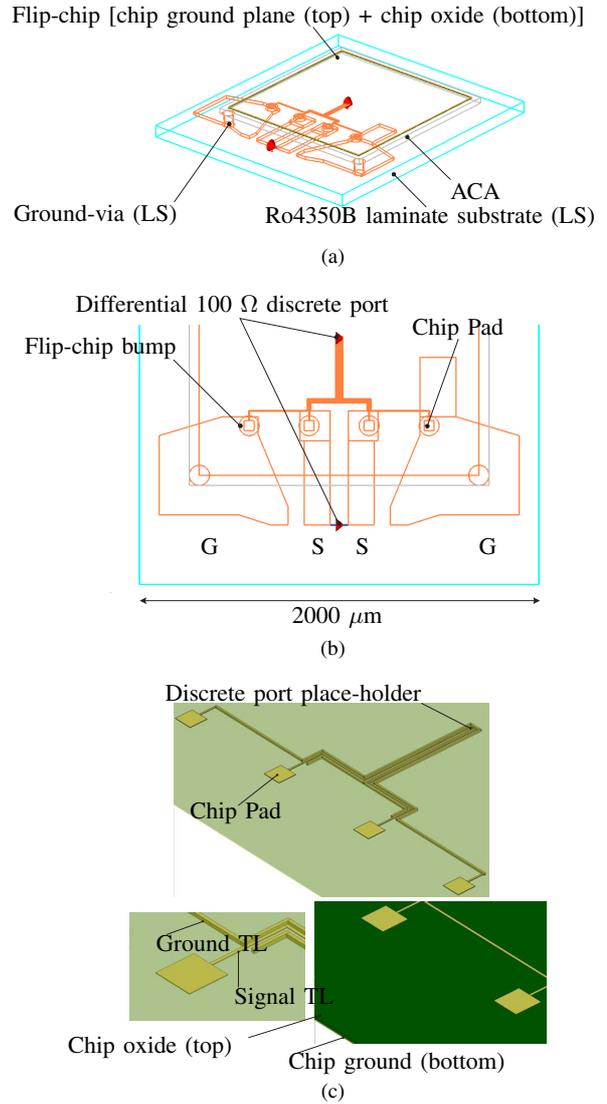

(a)

(b)

(c)

Fig. 2: CST model for TDR analysis of 60 GHz Flip-Chipped Package (a) 3D view, (b) Top view, (c) CST model of un-flipped CMOS IC.

software. The necessary and sufficient information required for simulation of the package (laminate, chip-mount and flip-chip interconnect etc.) is available from Fig. 1 and [5], [6]. Moreover, the details of the 100 Ω differential coplanar transmission line in a ground-signal-ground-signal-ground (GSGSG) configuration for CMOS PA are reported in [7], [8]. The transmission line has a measured differential impedance of 100 Ω and a relative dielectric constant of around 3.8-4. Following are the worth-mentioning points concerning the simulation set-up:

- The simulation uses PEC for metallized structures and does not incorporate the dielectric losses.
- The layout of the simulated flip-chipped package is delineated in Fig. 2. The details of the chip are shown in Fig. 2c, highlighting the connection scheme of on-chip GSGSG transmission lines and GSSG chip pads. The

TABLE I: CST simulated model of 60 GHz flip-chipped package (L = Length, W = Width, H = Height)

Components	Material	Dimensions [μm]
Ro4350B Laminate substrate	[ε_r] 3.74	[H]102
Ground-Via diameter	PEC	100
Metallization thickness	PEC	25
Flip-Chip Interconnection		
Bump diameter	PEC	100/25
Bump height	PEC	25/200
ACA	[ε_r] 3.3	[H]50
CMOS chip		
Chip ground plane thickness	PEC	2
Chip Oxide (SiO_2)	[ε_r] 4	[H]4.8
Chip Pad Dimensions	PEC	50×50×0.9
		[$L \times W \times H$]
Ground (G)/Signal(S) transmission line	PEC	[W] 4

TABLE II: 'Package-peeling' approach for TDR analysis of 60 GHz flip-chipped package

Cases	Description
A	Extended 100 Ω diff. line on Ro4350B substrate
B	**A** + Laminate ground-vias + ACA + Chip Oxide (SiO_2)
C	**B** + Chip ground plane
D	**C** + Flip-Chip bumps [diameter: 100 μm, height: 25 μm]
E	Fig. 2 package with Extended transmission line
F	**E** with Flip-Chip bumps [diameter: 25 μm, height: 200 μm]

input (RF probe to IC) side of the flip-chipped package is simulated with the assumption of similar behaviour on the output side (IC to antenna). The two 100 Ω differential impedance discrete ports, one on the laminate substrate and the other on-chip, are used for the simulation set-up. Table I tabulates the details of the simulated package.

B. TDR Simulation of 60 GHz Flip-Chipped Package

Following are the highlighting points concerning the TDR simulation of 60 GHz flip-chipped package using CST MWS.

- CST MWS with its transient solver is ideally suited for this task, since TDR pulses have to be short in time (to be able to resolve discontinuities in space) and thus extremely broadband. When using a gaussian pulse, the TDR is calculated from the time integral of the pulse, which again is the well-known (smooth) step function. The rise time T_{rise} in this case correlates to the upper limit of the frequency band. The frequency range should be adjusted to $f_{min} = 0$, $f_{max} = 0.876/T_{rise}$. The rise time is the 10 % to 90 % rising time of a corresponding step signal, which is the result of an integrated gaussian pulse. The TDR simulation set-up uses f_{max} = 1 THz, giving rise time T_{rise} of 0.876 ps.

- The spatial distance l of the discontinuity from the source can be estimated, if the effective dielectric constant ϵ_{eff} or dielectric constant ϵ_r of the medium is known [3]:

$$l = \frac{c_0 t}{\sqrt{\epsilon_{eff}}} \approx \frac{c_0 t}{\sqrt{\frac{\epsilon_r+1}{2}}}, \tag{1}$$

where t means the time the signal takes to reach the discontinuity. As a rule of thumb [3], two discontinuities
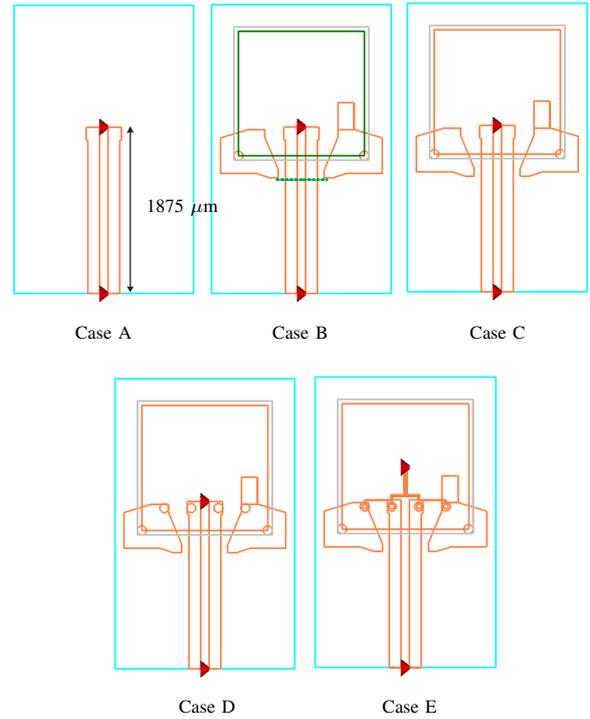

Fig. 3: 'Package-peeling' of 60 GHz flip-chipped package

can be resolved, if they are separated at least

$$l_{min} = \frac{c_0 T_{rise}}{2\sqrt{\epsilon_{eff}}} \tag{2}$$

from each other. Thus, the rise time T_{rise} of the step should be as short as possible. Assuming a dielectric constant ϵ_r of 4 for the material of the flip-chipped package, a sub-millimeter spatial resolution of almost 85 μm is obtained for flip-chipped package characterization, using T_{rise} = 0.876 ps.

- The use of waveguide port for the high frequency range of 1 THz is quite difficult because a lot of unwanted higher order modes are generated which has to be taken into account in the simulation; the discrete ports have been used instead. However, at this high frequency, the inductance of the discrete port becomes visible as well which will produce some over shoots in the TDR curve. Nevertheless, impedance discontinuities can still be seen and the overshoot can be decoupled from the package by using extended transmission line. Moreover, it is also important to see the behaviour of the propagating pulse in the package, to correctly interpret TDR impedance profile results.

- The 'package-peeling' approach uses different cases for TDR analysis, starting from a simple transmission line to the full 60 GHz flip-chipped package, as described and delineated in Table II and Fig. 3, respectively. The said approach aims to provide a more intuitive look into the flip-chipped package, in terms of impedance discontinuities.

Material	tan δ
Ro4350B Laminate substrate	0.004
Anisotropic Conductive Adhesive (ACA)	0.03
Chip Oxide (SiO_2)	0.01

from S_{11}-parameter needs to perform the inverse fourier transformation in the first step to reconstruct the TDR profile.

- Fig. 4a shows the impedance variations as the TDR pulse travels along the package for cases A to F. The impedance profile between the two discrete ports is analyzed; the region-of-interest is approximately from 5 to 22 ps after decoupling inductance overshoot of discrete ports. The time (location) of the impedance discontinuities for a non-dispersive medium is approximately twice $t = (l/c_0)\sqrt{\epsilon_{eff}}$, since the return distance is included in the TDR profile. However, a small pulse spreading due to dispersion can be seen in the impedance profiles of Fig. 4a. As can be seen, the impedance magnitude degrades from 97 Ω (case A) to 25 Ω (case E). Fig. 4b also shows the performance degradation of $|S_{21}|$ in the frequency domain for cases A to E. It is clear from the graphs that the close proximity of the chip ground plane is the main reason for the large impedance discontinuity, thereby degrading the transmission coefficient at 60 GHz, due to large mismatch. Assuming a similar behaviour on the output side (IC to antenna), the simulated losses for the both sides of the flip-chipped package are estimated, which are in-line with the observed losses during measurements of the said 60 GHz flip-chipped package (Fig. 1a). In order to validate the impedance values for cases A, B and C, the respective stacks have been simulated in another simulation set-up having waveguide ports. The E-field lines and the calculated line impedances for 60 GHz frequency are shown in Fig. 5. The close proximity of the chip ground plane gives rise to an unwanted mode for case C, thereby degrading the impedance.

- In order to decrease the proximity effect of the chip, the diameter and height of the flip-chip bumps were modified for case F. The simulation results in terms of TDR impedance profile and S parameters are shown in Fig. 4. Almost 3.5 dB improvement in the transmission coefficient is observed due to much better impedance match for case F.
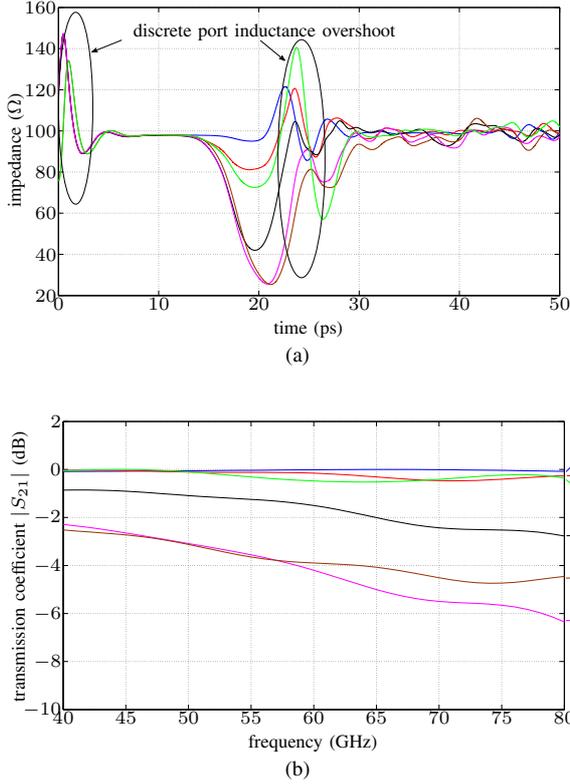

Fig. 4: CST-based TDR analysis for cases A [solid (blue)], B [solid (red)], C [solid (black)], D [solid (magenta)], E [solid (brown)] and F [solid (green)] (a) TDR impedance profile [region of interest: approx. 5-22 ps], (b) transmission coefficient $|S_{21}|$.
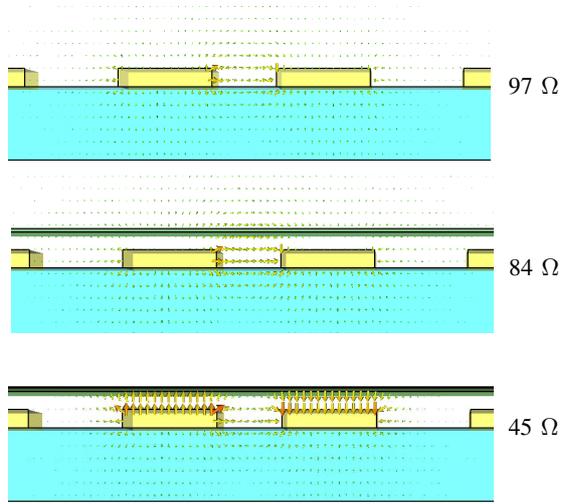

Fig. 5: E-field lines with line impedances at 60 GHz frequency for cases A, B and C, respectively

IV. EFFECT OF CONDUCTIVE AND DIELECTRIC LOSSES ON TDR/TDT RESPONSE

The application of TDR/TDT (Time Domain Reflectometry/Time Domain Transmission) method in distinguishing between the main causes of transmission losses, i.e., losses due to reflection, dissipation (conductive + dielectric losses) and radiation losses is investigated in this section. Since CST MWS determines the TDR impedance profile using input

- The TDR impedance profile can be determined from the time signals as well as S_{11}-parameter; both approaches give identical results. The TDR profile from the time signal approach directly takes the time integral of the input gaussian pulse and the reflected signal. The TDR
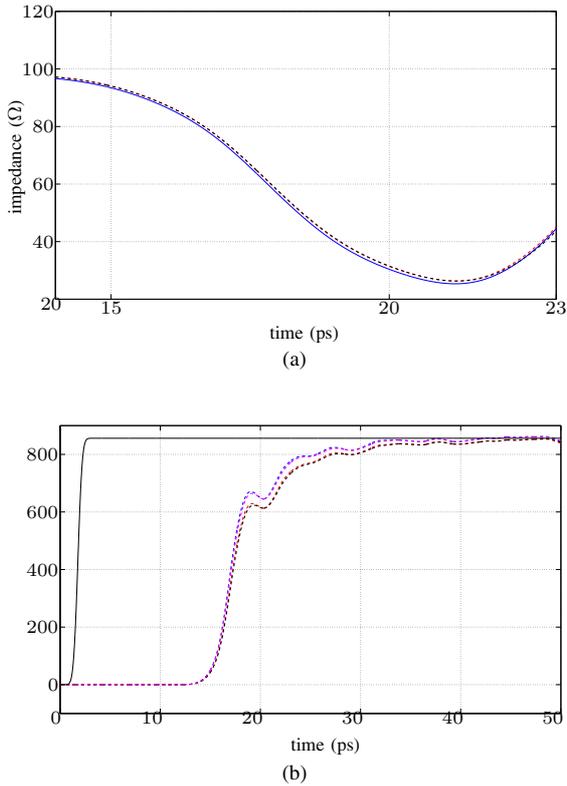
Fig. 6: (a) TDR impedance profiles for sub-cases of package **E**; E0 [solid (blue)], E2 [dash (red)] and E3 [dash (black)], (b) TDT profiles; integrated gaussian pulse [solid (black)], Transmitted pulses E0 [dash (blue)], E1 [dash (magenta)], E2 [dash (red)], E3[dash (black)].

and reflected signals of the flip-chipped package, the afore-mentioned effects can be incorporated by proper simulation settings. In the previous section, the TDR impedance profile has been generated using PEC material for metallized structures and no dielectric losses have been taken into account. Moreover, open boundary conditions are included which takes into account the radiation losses as well.

In order to investigate conductive and dielectric loss mechanisms using TDR/TDT approach, the following simulations are set-up for Case **E** (flip-chipped package having flip-chip bumps diameter: 100 μm, height: 25 μm):

- PEC for metallized structures with no dielectric losses [E0]
- PEC for metallized structures with dielectric losses [E1]
- Lossy Gold for metallized structures with no dielectric losses [E2]
- Lossy Gold for metallized structures with dielectric losses [E3]

Table III tabulates the loss tangent (tan δ) values used in the simulations. The TDR impedance profiles generated for the itemized sub-cases of package **E** are delineated in Fig. 6a (the impedance profile is shown from 15-23 ps for clarity). A variation of 1-1.5 ohms is observed in TDR impedance profile, when losses are included. As expected, the effect of dissipation losses on TDR impedance profile is small and

the influence of the reflection due to the geometrical profile is dominating. The total dissipative losses are found to be around 1 dB, as determined from $|S_{21}|$-parameter. The Time-Domain Transmission (TDT) profiles for sub-cases of package **E** are plotted in Fig. 6b to investigate the effect of dissipative losses on the transmitted pulse. As observed from the plots, the conductive losses play a dominant role in degradation of the transmitted pulse rise-time.

V. CONCLUSION

A 'package-peeling' approach using EM-tool based Time-Domain Reflectometry (TDR) is presented to investigate and address the cause of transmission losses for the 60 GHz flip-chipped package. It has been observed from the proposed approach that the close proximity of the chip ground plane is introducing a large dip in impedance profile, thereby degrading the transmission coefficient at 60 GHz, due to large mismatch. The estimated simulated losses for the both sides of the flip-chipped package are in-line with the observed losses during measurements of the 60 GHz flip-chipped package. The proposed technique provides a more intuitive and direct look at the package characteristics and aids in improving the performance of the millimeter-wave flip-chipped packages.

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