TOPICS: a new hierarchical design tool using an an expert system and interval analysis

TOPICS: A NEW HIERARCHICAL DESIGN TOOL USING AN EXPERT SYSTEM AND INTERVAL ANALYSIS

D.M.W. Leenaerts
Department of Electrical Engineering
Eindhoven University of Technology
5600 MB Eindhoven, the Netherlands

Abstract

A TOP-down Integrated Circuit Synthesis expert system (TOPICS) which is able to design *CMOS operational amplifiers (op-amps) is under development. The synthesis is* based on a *hierarchical design methodology and due to the fact that interval analysis is* used and all *solutions will be found the partitioning and mapping of the design constraints* on a normal *operating range of a collection of subblocks will always yield a solution.*

I. Introduction

In recent years many research was done to automate the design of analog circuits, aiming to reduce design time and cost. In order to reduce the design effort, standard cell libraries could be used. However, the disadvantages are the non optimal solution with respect to several design parameters (area, power dissipation etc.) and the rapid obsoletion due to technology evolution and changing design rules.

To overcome these disadvantages, one is starting to apply expert systems, software programs in which human expert knowledge is collected, often by using artificial intelligence techniques, in which this knowledge interacts with parameterized circuits. A few design systems in which the design of op-amps is done automatically have been developed, i.e. OASYS, BLADES, OPASYN, IDAC etc. [1,2].

In general these expert systems solve a set of non-linear equations together with design parameter values at each level in the hierarchical top-down design process. Due to the design constraints for normal circuit operation, some or all of these unknowns may only be chosen within specific domains. The problem is then to solve the equations in such a way that a solution exists when the design process goes a level down in the hierarchy, leaving a maximum amount of freedom for the set of design parameters (see fig. 1a). This problem is propagated through all the design levels until the solutions for all levels are found. This top-down parameter instantation may fail at a certain level due to an unrealizable circuit. The process has to be restarted a number of times, before a realizable partition can be produced. To avoid that this process has to be restarted several times, interval analysis can be used [3].

II. Interval analysis as part of the solution strategy

In interval analysis, each parameter is valid within a certain range, i.e. an interval. One can think for instance of the minimum and/or maximum allowable power dissipation and transistor sizes. Next, at each level the description of the domains of the parameters must be used to find the solution for matching the set of equations with these domains. The solution space actually yields new parameter domains (see fig. 1b). Advantages of this technique are that the solution space at each level is consistent with the solution spaces at higher levels and that all solutions will be found.
When at the lowest level the solution space is determined and nonempty, the solution space at higher levels is assembled using a bottom-up strategy from the solution at the lower levels. At the top design level, actual values can be chosen within the produced solution space. This automatically results in valid parameter values at the lower levels, in agreement with the design constraints at all levels of the hierarchy.

III. The expert system TOPICS

The above outlined technique is the kernel of the expert system TOPICS, a synthesis tool to design op-amps. TOPICS is built from three parts, an inference engine, a knowledge/rule base and a simulator (fig. 2). The used interval technique can be seen as a shell in TOPICS, which can be accessed by the three parts.

Controlling the design flow is done by the inference engine. The design starts, after reading the desired specifications of the op-amp, with the partitioning of the design constraints together with a corresponding partitioning of the circuit into smaller blocks. This partitioning takes place in the same way human design experts decompose the circuit into subblocks which can be designed almost independently of each other. Information on how to decompose the circuit can be found in the knowledge/rule base.
In contrast to many other systems, TOPICS is able to construct the topology of the circuit by itself. The topology and building blocks will be chosen during the design process, based on the solution space and the rules in the database.

At each level the design equations will be solved, using the interval analysis technique. When a solution space at a certain level becomes empty, meaning that for such a circuit configuration with corresponding design parameter domains there *never* exists a solution, even by any other method, the knowledge/rule base can be consulted for options (topology and subcircuits) to restart the design process. This is in contrast to other systems which try to restart the process with the same configuration but at an other starting point, not aware of the fact that a solution never exists.
When this top-down process is finished and all the transistors are sized the circuit can be analyzed by a simulator, integrated in TOPICS.

The hierarchical structure of the synthesis process, producing more detail at lower levels, demands the simulator to be able to link and use model descriptions in these stages. This requires a mixed-level simulator which option is supplied by a Piecewise Linear (PL) simulator. The use of such a simulator has another advantage: to find all solutions of sets of underconstrained non-linear equations, where the variables are eventually bound, can be done when the non-linear equations are approximated by piecewise linear equations [4]. Therefore the methodology to solve the equations, where interval analysis is used to restrict the parameter values for normal circuit operating ranges, is fully integrated in the simulator.

TOPICS is programmed in the C language and runs on a Apollo DM 3000 workstation. Detailed information about the piecewise linear simulator can be found in [5]. The next sections deal with the other main parts of the expert system.

IV. The knowledge/rule base

To deal with a broad scope of op-amp circuits the topology of these circuits is constructed by the system itself. For that reason, the system deals with an adequate set of basic building blocks, currently only blocks for designing one- and two-stage CMOS op-amps (fig. 3). The rules, describing the electrical behaviour of these subblocks are stored in the knowledge base. This database contains for instance simple rules of thumb for the amplification of or the noise in these subcircuits. Also interconnection properties such as impedance, voltage levels and node connections can be described by these rules.

Another class of rules gives information about when to use these subblocks, for instance the first stage or its building blocks, in comparison with other subblocks. Such rules are stored in a so called rule base together with the process technology parameters, in this case for a CMOS 2.4μm n-well process.

V. The inference engine

To produce an op-amp realizing the desired performance the inference engine activates the synthesis process to solve this problem. The inference engine uses a strategy as explained in section III and can be seen as a loop, containing six steps:

1) partition the design constraints
2) partition the circuit topology
3) solve the matching of both partitions
4) simulation
5) comparing simulation results with desired performance
6) goto step 1 at a lower level

The first three steps make use of the interval analysis technique as explained in section II. Due to the fact that at each level the same problem occurs upto the lowest level the iteration of step 6) is implemented. A stop criterium is needed when the desired circuit is obtained.

VI. An example

To show the advantage of the interval analysis in a synthesis environment, suppose the following desired performance of an op-amp is offered to TOPICS:

$V_{dd} = -V_{ss}$	= 5 V	UGBW	≥ 2 MHz
C_{load}	= 10 pF	ϕ_m	≥ 60°
A_o	≥ 80 dB	output swing	≥ ±2 V
SR	≥ 2 V/μs	eq. input noise	≤ 20 μV_{rms}
		P_{diss}	≤ 2 mW

Based on the rules collected in the rule base and the desired performance TOPICS takes the decision to use a one-stage approach. Now, at level one TOPICS tries to obtain the solution space of the parameters of the set of equations predicting the performance of the A_o, UGBW and the SR and the domains of these parameters. This convex solution space can be described by a linear combination of vectors (see fig. 4). Considering the solution space of level 1 TOPICS tries to design a general form of a folded OTA structure. Now, more design parameters will be used, i.e. ϕ_m, P_{diss} and the noise. After solving the set of equations, it seems that there only exist a solution when a folded cascode circuit topology will be used. At the end of this level the solution space for some parameters of a driver, load and cascode building block are obtained (fig. 4 level 2). At level 3 the rule base instructs TOPICS to use the simple load and the simple cascode option. A final solution space is obtained when the solutions at higher levels are assembled with the solution obtained for this level. After searching a smooth solution point in this space, the building blocks can be substituted and the transistors can be sized. At the lowest level in TOPICS a final simulation is done to compare the simulated performance of the design with the desired performance. These simulations are done by the PL simulator.

SPICE simulations are performed to compare the quality of the design equations, used by TOPICS and its PL simulator and show its correctness (fig. 4, level 4).

VII. Conclusion

The use of interval analysis within a hierarchical design environment leads to advantages. Due to the fact that the parameters are valid within intervals and all solutions will be obtained, if they exist, the synthesis will always yield a solution leaving the maximum amount of freedom in the selection of the parameters. A main advantage is that the solutions at each level are in accordance with solutions found previously in the synthesis process.

Literature

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[2] F.M. El-Turky,'BLADES: an expert system for analog circuit design' proc. ISCAS, pp.552-555, 1986.

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[4] D.M.W. Leenaerts, J.A. Hegt,'Finding all solutions of piecewise linear functions and the application to circuit design' Int. Journal on Circuit Theory and Applications, vol 19, march 1991.

[5] W.M.G. v Bokhoven,'Piecewise linear analysis and simulation' in: A.E. Ruehli (editor), Circuit analysis, simulation and design, Amsterdam, North-Holland chapter 9 1986.

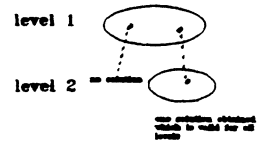


figure 1a: points

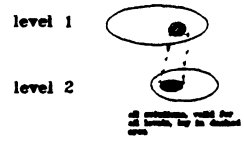


figure 1b: spaces

figure 1: solution points and spaces (ellipse denotes solution space valid for that level)

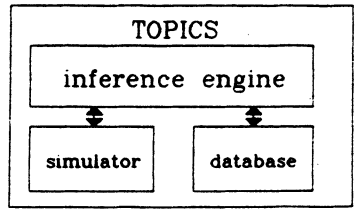


figure 2: organization of TOPICS

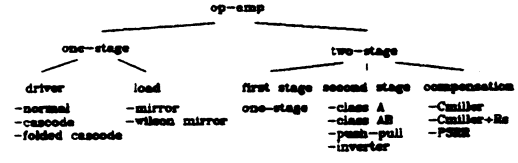
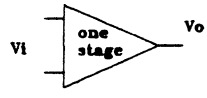


figure 3: building blocks

level 1 synthesis



parameters: gm, Ro, Io

rule base

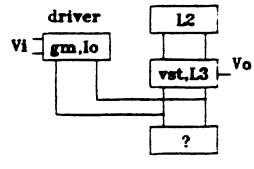
gm (uS) ∈ [1, 500]
Ro (MΩ) ∈ [1, 100]
Io (uA) ∈ [1, 50]

solution space

$(Ao,UGBW,SR,gm,Ro,Io)^T = \sum_{i=1}^{n=6} p_i \underline{a}_i$

$\forall_i p_i \geq 0$

level 2 synthesis



rule base

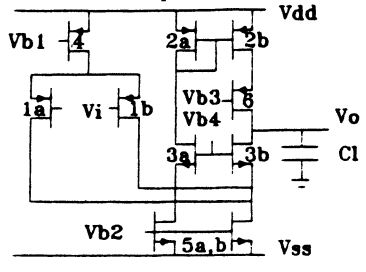
vst (V) ∈ [0.2, 0.5]
L2 (um) ∈ [2.4, 40]
L3 (um) ∈ [2.4, 10]

solution space

$(vst,L2,L3)^T = \sum_{j=1}^{m=3} q_j \underline{b}_j$

$\forall_j q_j \geq 0$

level 3 optimalization in space $(Ao,UGBW,SR,noise,Pdiss,....,gm,Io,L2,L3,vst,.....)^T = \sum_{i=1}^{max=7} r_i \underline{c}_i \quad \forall_i r_i \geq 0$



size of transistors (um)

W1/L1 = 199/2.4
W2/L2 = 80/2.4
W3/L3 = 59/2.4
W4/L4 = 63/2.4
W5/L5 = 47/2.4
W6/L6 = 196/2.4

voltage sources (V)

Vb1 = 3.6
Vb2 = -3.6
Vb3 = 2.87
Vb4 = -2.87
Vdd = 5
Vss = -5

level 4 final simulation and comparison with SPICE

specification	TOPICS	SPICE
Ao (dB)	80	79.8
UGBW (MHz)	4.47	4.7
SR (V/us)	5.6	5.3
φ_m	89.6	84
noise (uVrms)	13	-
Voff (mV)	0.28	0.018
swing (V)	3.8	4
Pdiss (mW)	1.1	1.1

figure 4: final results at each design level of TOPICS