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A Multiphase Series-Resonant Converter with a New Topology and a Reduced Number of Thyristors

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Abstract—Multiphase series-resonant (SR) power converters provide a flexible way to transform power between a utility grid and a multiphase load or source. The current implementations all suffer from a high component count, which makes the use of these converters unattractive from an economical point of view.

A new topology for multiphase SR converters has been proposed in the literature in a simulation context. This topology uses half the number of power semiconductors compared to the existing multiphase SR converters.

The present paper addresses the implementation of the new topology in a prototype converter. The old and new topologies are presented. The operation of the new topology is explained. In the new topology the resonant circuit is grounded at one side, which compared to the old topology imposes a restriction on the operation.

The paper shows both simulation data and measured waveforms. It is explained that the economical gain due to the reduction in component count is offset by a lower power rating. The paper finishes with conclusions and acknowledgments.

Index Terms—Power electronics; control systems; invertors; series resonant converters; three-phase; AC-to-AC power converter; reversible power flow; thyristors; reactive power generation.

I. INTRODUCTION

SERIES-RESONANT (SR) techniques have been used for a long time to attain low switching losses in dc–dc power converters. The low switching losses facilitate using high switching frequencies while keeping, at the same time, the conversion efficiency high.

During the last decades the use of SR techniques has spread out into the field of multiphase applications. The transition from SR dc–dc to SR multiphase converters has been made in three steps: first multiphase to dc, then dc to multiphase, and finally multiphase to multiphase.

The first step was made in [1], where the traditional three-phase input rectifier was replaced by a controlled thyristor bridge, which was part of the resonant structure. In this setup, the input currents of the three-phase to dc converter would still have rectangular shapes. However, contrary to the “classic” thyristor bridge/dc–dc converter combination the power factor at the input could be kept high (0.955) under all operating conditions.

A further step was made in [2], [3], where a flexible modulation process was introduced to generate essentially sinewave

currents at the output of a dc to three-phase converter. It was shown that control of the state of the resonant circuit was of paramount importance, and to that effect the V_{cpeak} -predictor circuit was introduced. A related problem lies in the field of High Frequency (HF) power distribution in space vessels. The decomposition of an HF carrier into waveforms for several Low Frequency ac or dc loads has been treated in [4]–[6].

For an SR multiphase to multiphase converter a major control problem lies in the generation of the input currents. As the converter itself has a negligible capability for energy storage, input and output power need to be precisely matched under all operating conditions. At the same time, the power factor at the input of the converter needs to be maximized, and therefore tight constraints on the shape of the multiple input currents need to be maintained. This problem was first addressed in [7], [8], and treated in more detail in [9].

The multiphase SR converters which have been presented in the literature feature several interesting properties, including

- Smooth input- and output voltages and -currents.
- Adjustable power factor at the input of the converter, including unity.
- Absence of low-frequency filters, thus reducing weight.
- Common grounds for inputs and outputs, thus reducing high-frequency interference, and facilitating “clean” measurements.
- Easy parallel operation (phase-staggering) of multiple modules.
- Expandability to any number of inputs or outputs.

In these applications one resonant L - C tank is time-shared between the input- and output terminals of the converter. A common topology of the power circuit makes it necessary to connect both sides of the resonant tank to the terminals of the converter. For ac operation, current flow in two directions is necessary, and therefore the number of semiconductor switches needed for multiphase ac applications equals four times the total number of terminals. For a three-phase to three-phase converter 24 switches would be needed. Clearly, this number compares badly to the number of active devices which is needed to build a PWM voltage source inverter bridge.

In this paper a modified multiphase SR converter topology is presented, in which only one side of the resonant circuit can, by means of a switch matrix, be connected to the input- and output terminals of the converter. The other side of the resonant tank is connected to a common neutral. The number of active semiconductors (SCR thyristors in our case) in this topology reduces to 12, which clearly is an advantage as compared to the 24-thyristor alternative.

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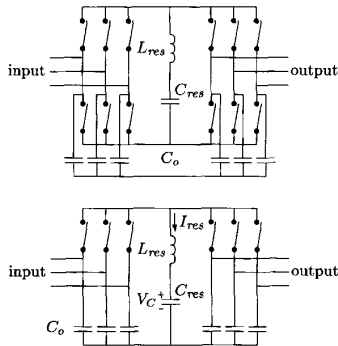


Fig. 1. Topologies of two power circuits. (a) (upper) The old circuit. (b) (lower) The new circuit.

II. CIRCUIT TOPOLOGIES

The “classic,” 24-thyristor topology is shown in Fig. 1(a). The circuit is composed of two three-phase switch matrices connected in parallel to an SR tank composed of L_{res} and C_{res} . Both inputs and outputs are connected to capacitive filters, which are referenced to a common neutral.

In Fig. 1 every switch represents the combination of two antiparallel thyristors and their snubber circuits. The operation of the circuit is based on the selective redirection of the current in the resonant tank to the input- and output terminals. For detailed information concerning the operation of the circuit in Fig. 1(a) the reader is referred to [8], [9], [7].

The new topology is depicted in Fig. 1(b). In this circuit one side of the resonant tank is connected to the neutral which is common to inputs and outputs. Compared to Fig. 1(a) the number of semiconductor switches is reduced to half.

III. OPERATION DURING ONE RESONANT PULSE

A. State-Plane Description

For the analysis of the circuit in Fig. 1(b) all voltages will be referred to the “starpoint,” i.e., the common of the filter capacitors (C_o).

The operation of the power circuit of Fig. 1(b) is most easily demonstrated starting from the situation where the voltage across the resonant capacitor (V_C) is at its maximum value. If the magnitude of this peak capacitor voltage is larger than any of the input- or output voltages, the direction of current flow will be dictated by its polarity. Furthermore we will assume that the value of the filter capacitors (C_o) is much larger than the value of C_{res} , which implies that the source and load of the converter can be modeled as ideal voltage sources.

Current flow in the circuit starts with the closing of one of the six switches. With the assumptions mentioned before, the direction of the resonant current is dictated by the sign of V_C , i.e., I_{res} will become positive if V_C was negative and vice versa. For simplicity, only the case of a negative initial value for V_C will be considered in the following. The case for positive V_C can be treated in a completely analogous way.

Without further intervention, the resonant current I_{res} will develop as a positive sine wave. At the moment this current

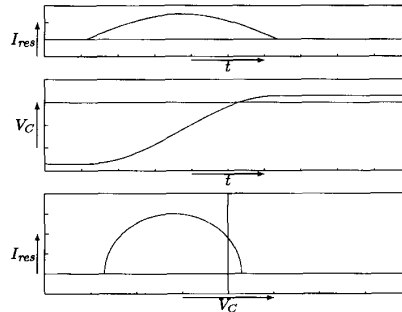


Fig. 2. Signal shapes for one resonant sine wave. (a) (upper) I_{res} : Current through L_{res} . (b) (middle) V_C : Voltage across C_{res} . (c) (lower) I_{res} versus V_C .

becomes zero again, the thyristor switch will turn off, and V_C will have been mirrored in the voltage of the terminal whose switch had been closed.

Figs. 2(a) and (b) show the shape of the resonant current (I_{res}) and capacitor voltage (V_C). When these two variables are plotted against each other in the so-called state-plane [10] the trajectory shows up as an ellipse, or, with proper scaling, as a circle. This circle has been depicted in Fig. 2(c). The center of this circle is located at $(V_{LC}, 0)$, where V_{LC} indicates the voltage applied to the resonant circuit. Geometrically the “mirroring” of the capacitor voltage in V_{LC} is quite obvious.

B. Energy Considerations

It has been argued in [9] and [11] that continuous operation of a multiphase resonant converter is possible subject to the following conditions:

- V_C should be large enough to overcome any opposing terminal voltage. Depending on the switching pattern, the magnitude of V_C should either exceed the largest difference between any two terminal voltages, or exceed the largest terminal voltage. The former is the case in the old topology, the latter applies to the new topology.
- V_C should be exactly inverted after every resonant half cycle. In this way it is guaranteed that the initial conditions for the next resonant half cycle are (apart from a trivial inversion) identical to those of the cycle which has just been finished.

If the capacitor voltage is exactly inverted after every resonant half cycle, the net energy supplied to the resonant circuit needs to be zero. This implies that two voltages of opposite polarity need to be applied in sequence to the resonant circuit. The reader may want to compare this need to the situation in the well-known buck-boost converter, where two voltage polarities are used to constrain the energy in the main inductance.

A proper choice of the moment of turnover (t_1) from the “first” to the “second” terminal voltage permits precise control of the final value of V_C . If the two terminal voltages involved satisfy some auxiliary constraints, the reachable range for V_C at $I_{res} = 0$ includes the inverse of the initial value of V_C . Fig. 3 shows the influence of a varying moment of turnover from the first to the second current segment on the shape of the resonant current [Fig. 3(a)] and on the capacitor voltage [Fig.

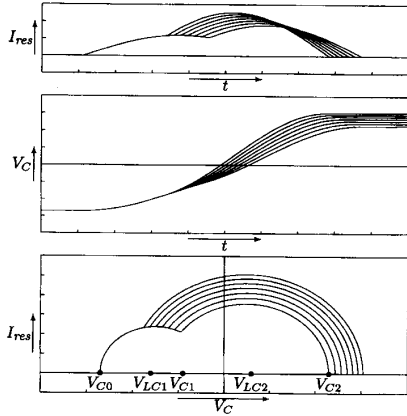


Fig. 3. Signal shapes for a resonant sine wave composed of two current segments for varying turnover time t_1 . (a) (upper) I_{res} : Current through L_{res} . (b) (middle) V_C : Voltage across C_{res} . (c) (lower) I_{res} versus V_C .

3(b)]. The state-plane portrait of the operation of the converter for this case has been drawn in Fig. 3(c).

In Fig. 3(c) the following important voltages are identified:

- V_{C0} The initial voltage across the resonant capacitor.
- V_{LC1} The voltage applied to the resonant circuit during the first current interval.
- V_{C1} The voltage across the resonant capacitor at the instant of turnover from the first to the second current interval.
- V_{LC2} The voltage applied to the resonant circuit during the second current interval.
- V_{C2} The voltage across the resonant capacitor after current flow has terminated.

The trajectories in Fig. 3(c) are each composed of two circular segments. The first circle is centered around V_{LC1} , and the second segment is centered around V_{LC2} . If the values for V_{C0} , V_{C2} , V_{LC1} , and V_{LC2} are supplied, the construction of the trajectory is straightforward. Clearly, the proper moment for turnover is indicated by the intersection of the two circles.

C. Predictor Circuit

For the real-time control of the peak capacitor voltage (V_{C2}), the instant in time where the two circles of the state plane trajectory intersect needs to be determined. Several techniques can be used for this purpose. In [2] and [12] the instant for turnover is determined by computation of the distance of the first part of the trajectory in Fig. 3(c) to the center of the second part. The condition which is tested with this method can be expressed as

$$(Z_{res}I_{res})^2 + (V_C - V_{LC2})^2 \leq (V_{C2} - V_{LC2})^2 \quad (1)$$

where

$$Z_{res} = \sqrt{\frac{L_{res}}{C_{res}}} \quad (2)$$

At the first instant that (1) holds, turnover to the second current segment is initiated.

In the converter under consideration a different method was used, which can be analyzed as follows.

The value of the capacitor voltage at the instant of turnover (V_{C1}) can be derived analytically from the equations describing the circuit behavior. Skipping the derivation, which can be found in [9] this value is given by

$$V_{C1} = \frac{V_{C2}(V_{C2} - 2V_{LC2}) - V_{C0}(V_{C0} - 2V_{LC1})}{2(V_{LC1} - V_{LC2})} \quad (3)$$

where V_{C0} equals the initial value of the capacitor voltage, V_{C2} is the intended peak value of the capacitor voltage, and V_{LC1} and V_{LC2} indicate the voltages applied to the resonant circuit during the first and second current segment, respectively. Note that if no disturbances are present, then

$$V_{C0} + V_{C2} = 0 \quad (4)$$

which simplifies (3) somewhat. However, simulation experiments indicated that (3) shows better robustness against disturbances than (4). Therefore the complete expression (3) was used for the control setup. The condition to test for with this method can now be expressed as

$$V_C \geq V_{C1} \quad (5)$$

Inspection of the right-hand part of (3) and comparison with (1) shows two special properties:

- Equation (3) uses only values which can be measured *before* the initiation of current flow. The only error which is made in this way is that the influence of ripple on the terminal voltages V_{LC1} and V_{LC2} is disregarded. Consequently, the right-hand side of (3) needs to be evaluated only once for every current pulse. This shows a sharp contrast to (1), which needs to be evaluated continuously during the first current segment.
- In (3) only measured voltages are used. Consequently, the scaling with Z_{res} , which can be influenced by production tolerances and aging of the components of the resonant tank, is not needed.

For the actual computation of V_{C1} both analog (multiplier) and digital (DSP) methods can be used. Which method is preferred, depends more on economical than on technical considerations.

D. State Plane Presentation of the Control Law

Fig. 4 depicts the trajectories of (V_C , I_{res}) plotted in the state-plane (left) and vs. time (right). The scaling in the state-plane has been adjusted such that $Z_{res}I_{res} \equiv V_C$, therefore the trajectories show up as as circle segments.

In the state plane, our proposed control method shows a superficial similarity to capacitor-voltage control (see [13], [12]). As in that method, the actual capacitor voltage V_C is compared against a preset value (V_{C1} in our case). However, contrary to plain capacitor-voltage control, in our method the voltage V_{C1} is adjusted to the actual operating conditions for every individual resonant half wave. The adjustment is given mathematically by (3). The net result is that the transient response of the converter equals the response under optimal-trajectory [12] or V_{Cpeak} [9] control.

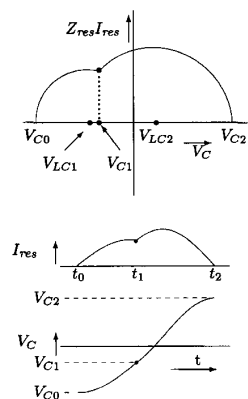


Fig. 4. Trajectories of (V_C, I_{res}) and control law in the state plane for one resonant half cycle.

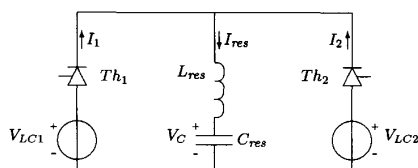


Fig. 5. The part of the power circuit of Fig. 1(b) which is active during one resonant half cycle.

E. Commutation

For the duration of one positive resonant half cycle, the active part of the circuit of Fig. 1(b) can be drawn as in Fig. 5. For convenience, in Fig. 5 the first voltage (V_{LC1}) applied to the resonant circuit has been drawn at the left, and the second voltage (V_{LC2}) at the right. However, these voltages can correspond to *any* of the terminals (input or output) in Fig. 1(b).

If SCR thyristors are used for the power semiconductors, the sequence of voltages applied to the resonant circuit is subject to the laws which govern the commutation of current from one thyristor (Th_1 in Fig. 5) to the other (Th_2). Inspection of the circuit shows that if I_{res} is positive, V_{LC2} needs to be more positive than V_{LC1} , in order to be able to turn off Th_1 .

An example of the currents in the circuit branches of Fig. 5 has been depicted in Fig. 6.

The currents in the two voltage sources show infinitely steep transients at the instant of turnover. For physical thyristors, these steep current slopes would lead to high turn-on and turn-off losses. Also, high levels of EMI (electromagnetic interference) may be expected. Therefore, in the real circuit commutation inductances (L_c) are placed in series with the thyristors in order to smooth the current transients.

During current flow, the commutation inductances act in series with the main inductance. The size of L_c relative to the total resonant inductance is subject to the following considerations:

- For $L_c = 0$ the analysis of the circuit operation leads to explicit equations, which in their turn can be used to design a predictor circuit according to (3). However, small

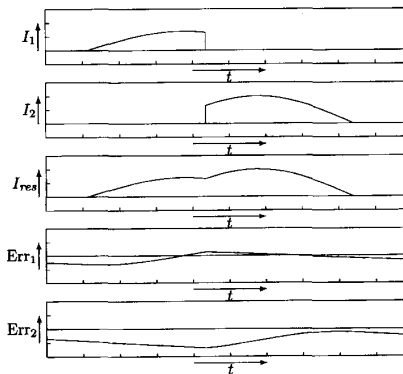


Fig. 6. Currents in the branches of Fig. 5, and signals in the current control system I_1, I_2, I_{res} : currents in the branches of Fig. 5, Err_1, Err_2 : The corresponding ASDTIC-signals according to (6).

values for L_c will lead to high values for the di/dt of the semiconductors. In any case, L_c needs to be high enough to assure that device ratings for di/dt are not exceeded.

- A very large value of L_c , i.e., L_{res} approaching zero, leads to very smooth waveforms for the semiconductors. However, tight control with a predictor circuit becomes awkward, to say the least. This problem is discussed more fully in [9]. The operation of the circuit in the limit case ($L_{res} = 0$) has been discussed in a simulation context in [14].
- It has been shown in [15] that an intermediate value for L_c , ca. 25% of L_{res} , leads to minimum power losses in the snubber circuits.

An optimal choice for L_c depends on the weighing of design parameters like cost, efficiency, and complexity of the control system. For the prototype considered here, priority was given to the latter. The control system used is based on a circuit model without the L_c present. Therefore the value of L_c was chosen only slightly larger than the value for which the di/dt rating of the devices would be exceeded.

F. Current control

Fig. 6 shows that a finite amount of charge has been transported to two out of the six terminals of the converter. For the next current pulse other terminals can be chosen, which implies that in time every terminal can be supplied with the desired amount of charge. A control loop is needed to adjust the charge transfer process in order to arrive at the desired current flow in every terminal.

The control system which was used consists of a modified ASDTIC controller [3], [16] for every terminal of the power circuit. In this controller, every terminal is associated with an ASDTIC error signal which is defined as follows:

$$Err = \int (i - i_{ref}) dt. \quad (6)$$

The ASDTIC error signal for a voltage-controlled terminal is defined in an analogous way (see [8]). The sum of the rectified ASDTIC errors, which can be interpreted as an overall error signal, is used to trigger the generation of a new current pulse.

The error signals in the modified ASDTIC control system have been shown in the lower two traces of Fig. 6. Fig. 6 shows that due to the displaced charge of the current pulse the two ASDTIC signals are restored to a position closer to zero.

IV. SELECTION OF TERMINALS

The flow of current in the resonant circuit is initiated when the overall error signal, composed from the individual terminal error signals, crosses a certain bound. However, in *which* terminals the current is going to flow is still to be decided.

From the previous discussion two items are of special importance here:

- 1) The currents in both terminals which will be serviced during this particular resonant current pulse will flow in the same direction as I_{res} . Clearly, during the next resonant half cycle I_{res} will flow in the opposite direction. This implies that at least two (other) terminals should be available which can handle this direction of current flow.
- 2) In order to be able to keep the peak capacitor voltage at a predictable level, the voltages on the two selected terminals need to oppose each other.

Of course, the charge transported by a resonant current pulse needs to be used to lower the overall error signal. Therefore a selection of terminals according to the sign and magnitude of their individual error signals is appropriate.

A. Strict Polarity Check

The first selection method depends on a strict check of the polarities of error signals and voltages.

If this polarity criterion would be strictly adhered to, the minimum number of terminals for a converter would appear to be 4. Two out of these terminals would operate with positive current flow, and be serviced during the positive resonant half cycles, and the other two would be serviced during the negative half cycles.

Closer inspection of the circuit operation would indicate that proper operation of a 4-terminal converter would hardly be feasible. Due to the exact inversion of the capacitor voltage the net energy consumption of the converter over a resonant half cycle is zero. Therefore both the two "positive" and the two "negative" terminals are subject to an energy constraint. If I_{p1} is used to denote the current in the first "positive" terminal, I_{m1} for the first "negative" terminal, and similarly for the voltages, the energy constraint for the "positive" pair can be formulated as follows:

$$I_{p1}U_{p1} + I_{p2}U_{p2} = 0 \quad (7)$$

and similarly for the "negative" pair.

Furthermore, due to Kirchhoff's current law the sum of the currents flowing into the converter over one complete resonant cycle needs to be zero. Consequently, this also applies to the average current over any time span:

$$I_{p1} + I_{p2} + I_{m1} + I_{m2} = 0. \quad (8)$$

Three constraints applied to four currents implies that only one current can be chosen freely in this situation: the other three can then be found using the constraining equations.

In the (more interesting) case of a three-phase to three-phase converter, a similar approach would lead to three degrees of freedom (six terminals—three constraints). These three degrees can be used to select the wave shapes of the three output currents, the input currents would then be defined by the constraints. It follows that in this situation it is not possible to select the shape of the input currents: the system has too many constraints to achieve this. This conclusion was confirmed by a simulation of this system: although the output currents conformed reasonably well to their prescribed (sine) wave shapes, the input currents showed a ragged appearance. A similar result has been reported in [14].

B. Loose Polarity Check

Inspection of the operation of the simulated converter with strict polarity check revealed that the control system spends a large percentage of time waiting for one of the terminal voltages or error signals to pass through zero. This undesirable behavior is caused by the strict interpretation of the polarities involved. For example, the control system could allow a current pulse to be generated if a certain signal would be at +1 mV, but stall the operation if the same signal would lie at -1 mV. However, a human observer would interpret both values to be "close to zero," and treat both situations equally.

Trying to mimic this behavior in the control system, it was decided to loosen the polarity check. For example, for a positive half wave of the resonant current, first the terminal with the most negative or least positive error signal would be selected. Then, on the remaining terminals with opposite polarity of the voltage, a similar selection could for example lead to positive current flow in a terminal with an already positive error signal, thus in fact worsening the situation for this individual terminal. However, for the complete converter system the total error is still lowered. Contrary to the setup with a strict polarity check, the operation of the complete system does not stall any more because for example only one terminal with positive current flow was available. Simulation of this setup showed superior performance. It was even shown to be possible to operate a three-terminal converter in this way.

C. Algorithm

The implementation of the terminal selection uses, similarly to the system which has been discussed in [9], a sequential two-pass selection circuit. During a *first pass*, the terminal with the most positive (least negative) or most negative (least positive) error signal, depending on the direction of the resonant current (polarity of V_C), is selected. The *second pass* is used to select a *second terminal* from the remaining terminals with an opposing voltage. An example of the selection will be given in Section V.

After the selection process, the thyristor which is going to conduct during the first current segment can be fired. Turnover to the second current segment is initiated when the V_{cpeak} -predictor circuit indicates that the cross-over point between the two trajectories of Fig. 3 has been reached. The second current segment is terminated when the resonant current again

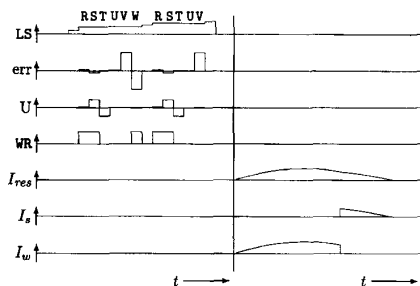


Fig. 7. Simulated operation of the terminal selector and start of current flow.

reaches zero. After an appropriate turn-off time, the circuit is ready for the next current pulse.

V. SIMULATION

In order to test the intended operation of the power circuit and its control, a simulation needed to be set up. Due to the similarity of the new circuit to its old counterpart, it was possible to reuse the software which had already been written for that circuit [9]. It was found that only minor modifications were needed in the analog sections of the simulation. However, the new selection algorithm made it necessary to reprogram the digital part of the simulation.

Fig. 7 shows the operation of the algorithm for the terminal selection. For clarity, the left-hand part is plotted with an expanded time scale. During a first pass, indicated by the second step on the staircase-like signal LS , all six terminals (R, S, T, U, V, W) are checked sequentially (indicated by the lettering above trace LS) in order to find the one with the worst error (signal err). The signal WR indicates whether a terminal has been temporarily selected. The last terminal for which signal WR is high, is included in the final selection. In Fig. 7, this is terminal W , which clearly corresponds to the largest negative error signal (see trace err). Also, during the first pass, the sign of the voltage on the selected terminal (signal U) is stored for use during the second pass. In this case, the voltage on terminal W is (slightly) negative.

In the second pass, indicated by the fourth step on signal LS , the remaining five terminals (R, S, T, U, V) are checked for the proper polarity of their voltages. In this case, due to the fact that the first selected terminal (W) carries a negative voltage, we need a terminal with a positive voltage. If more candidates are available, the one with (again) the worst error signal is taken. Fig. 7 shows that finally terminal S remains selected in this pass.

The right-hand part of Fig. 7 shows the development in time of the currents in the resonant circuit and in two of the six terminals of the power circuit on a much longer time scale. The current flow is initiated in terminal W , because during the first current segment energy needs to be transported out of the converter.

On a much larger time scale, the operation of the circuit starting at zero initial conditions has been depicted in Fig. 8.

In Fig. 8, the converter is configured as a three-phase reactive current compensator, i.e., only the left-hand part of the circuit in Fig. 1(b) is used. The upper traces show the current

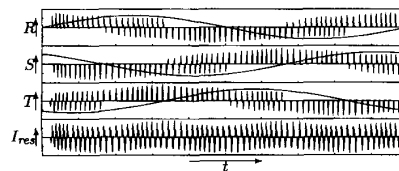


Fig. 8. Simulation of the operation of the new circuit configured as a reactive current compensator. Upper traces: unfiltered current and voltage in terminal R, S , and T , respectively. Lower trace: current in the resonant tank. The simulated time span is 20 ms.

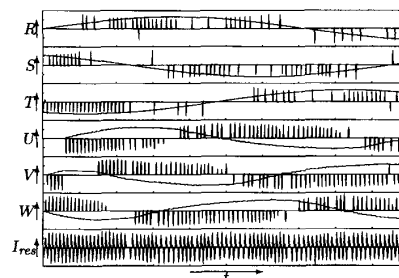


Fig. 9. Simulation of the operation of the new circuit configured as a three-phase ac to three-phase ac converter. Upper traces: unfiltered current and voltage in terminals R, S , and T , (inputs) and U, V , and W (outputs), respectively. Lower trace: current in the resonant tank. The simulated time span is 20 ms.

pulses flowing in the three input terminals and the associated voltages. The average of the current pulses shows a typical 90 degrees phase shift when compared to the corresponding voltage.

Fig. 8 shows that around the maximum value of a terminal voltage the associated current is composed of alternating positive and negative pulses, which implies that the average current in this interval lies close to zero. This kind of behavior would not be compatible with a strict polarity check.

Fig. 9 shows the operation of the system configured as a three-phase to three-phase converter. The simulated input frequency is 35 Hz, the frequency of the output voltages is 50 Hz. The traces in Fig. 9 show the division of resonant current pulses over the input (R, S, T) and output (U, V, W) terminals. Due to the larger number of degrees of freedom, the alternating pulse pattern which was shown in Fig. 8 is practically absent here.

In the simulation, the converter is loaded with three resistors of 75Ω in a star configuration. Simulation experiments showed that this is approximately the maximum resistive load which can be powered for this configuration. At a rated line voltage of 380 V (rms), this corresponds to an output power P of

$$P = \frac{380^2}{75} = 1925 \text{ W.} \quad (9)$$

It is interesting to note that the old power circuit configuration [see Fig. 1(a)] was able to power a threefold load (25Ω in star, see [9]). The reduction in output power is rooted in three facts:

- 1) In the new power circuit only one side of the resonant tank is used to supply current to the terminals. Therefore the current rating of the new converter is reduced by at least 50%, compared to the old topology.

TABLE I
RMS CURRENTS IN THE INPUT AND OUTPUT THYRISTORS OF THE TWO TOPOLOGIES

	old topology	new topology
Input thyristors	2.65 [A]	4.12 [A]
Output thyristors	4.35 [A]	6.68 [A]

TABLE II
PARAMETERS OF THE PROTOTYPE CIRCUIT

L_{res}	148 μ H
C_{res}	2 μ F
C_o	90 μ F
L_c	20 μ H
thyristors	SKFT60/12DT

- 2) The handling of reactive output power is much less effective here. The old power circuit was able to transfer power between two terminals and supply current to the third in one resonant half cycle. The new circuit needs a complete resonant cycle to accomplish the same.
- 3) With the lower output current rating, and the same output voltage and frequency, a larger percentage of the output current is consumed by the (unchanged) filter capacitors.

Clearly, the latter two mechanisms only show up under ac operation.

Simulations were also used to compare the current stresses on the individual thyristors in the old and new topologies. Both topologies were resistively loaded with 75 Ω in Y configuration. The results for the RMS currents are reported in Table I.

Table I shows that the thyristors in the new topology have to endure over 50% larger current stresses for the same load. A similar result was found for the rms current in the resonant circuit.

VI. MEASUREMENTS

For the experimental verification of the new concept, a prototype converter needed to be constructed. The primary goal of the experiments being to show the operation of the new control method on real hardware, it was decided to recuperate an existing circuit. Therefore the converter hardware shown here probably is not optimal for the new topology. For the verification which we present here this is not a serious drawback.

Table II lists the most important parameters of the prototype circuit.

As has been discussed in Section III-E, commutation inductances (L_c) were placed in series with the thyristors in order to limit the di/dt values applied to these components. A more thorough description of the power circuit can be found in [9].

In order to convert the old into the new topology, two major changes were called for:

- 1) The two lower rails in Fig. 1(a) needed to be connected together, and
- 2) the lower row of switches needed to be deactivated.

The digital part of the control electronics was implemented using programmable logic devices (EPLD's), which made the

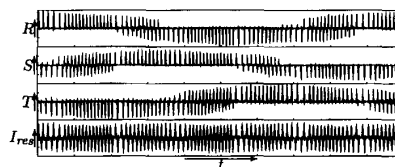


Fig. 10. Currents measured in the prototype of the new circuit operated as a reactive current compensator. Upper trace: current in the resonant tank. Lower traces: unfiltered currents in terminal T , S , and R , respectively. The full range of every trace is -52.4 to 52.4 A. The time scale covers 20 ms.

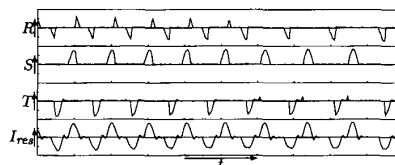


Fig. 11. Traces as in Fig. 10. The time scale covers 2 ms.

latter change rather straightforward. With these, and some minor changes in the analog control electronics, a configuration according to the topology of Fig. 1(b) was obtained.

A. Three-Phase Operation

Fig. 10 shows the operation of the prototype converter configured as a three-phase reactive current compensator.

The measured signals in Fig. 10(a) show good agreement to the simulation results in Fig. 8. Differences lie mainly in fast transient effects, which were not modeled in the simulation.

Fig. 11 shows the the same configuration as in Fig. 10(a) on a smaller time scale. The currents in Fig. 11 show the gradual takeover of alternating current pulses from phase R to phase T . On this stretched time scale, the presence of reverse recovery spikes, which were not included in the simulation model, is visible. Furthermore the traces in Fig. 11 show that, due to the commutation inductances, the slope of the current pulses is limited.

B. Three-Phase to Three-Phase Operation

Fig. 12 depicts the system operating as a three-phase ac to ac converter. The input frequency is 50 Hz, the converter generates an output waveform at 23 Hz. The three-phase input voltage is supplied by a variable transformer with a relatively high impedance. As a consequence, the stability of the input circuit is rather low, which shows up as distortion of the input voltage.

Fig. 12 shows the division of the individual current pulses over the input- and output terminals. It shows that a relatively smooth output wave form is generated in spite of the distorted input voltage.

VII. CONCLUSION

The operation of a multiphase SR power converter with a new topology has been presented both in simulation and as a prototype. This new topology uses a relatively small number of power semiconductors. The topology can be used for a

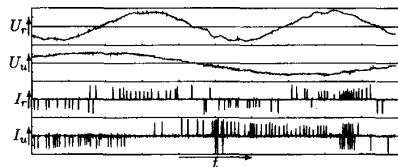


Fig. 12. The prototype of the new circuit operated as a three-phase ac to ac converter. Traces (from high to low): U_r : voltage on input terminal R , U_u : voltage on output terminal U , I_r : current through input terminal R (unfiltered), I_u : current in output terminal U (unfiltered). The full range of the voltage traces is -240 to 240 V, the current traces range from -52.4 to 52.4 A. The time scale covers 40 ms.

converter with three or more terminals, be it input, output, or mixes thereof.

The state of the resonant circuit is controlled between tight margins through the application of a modified V_{cpeak} controller.

The converter is capable of step-up and step-down operation, both for dc and ac waveforms, between two grids connected to a common neutral. Furthermore the power factors at both input and output can be controlled independently.

Compared to the old topology, the current handling capability of the new converter will be at least 50% lower for dc operation. The reduction will be even larger for ac inputs or outputs. The effective pulse repetition frequency shows a similar reduction.

The converter is a promising candidate especially for active power factor correction. In this configuration only six thyristors are used.

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