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Abstract: In this paper, we present a study of integrated optical delay lines (DLs) for application in optical time-division multiplexers. The investigated DLs are formed by spirally folded waveguides. The components were designed in a generic approach and fabricated in multi-project wafer runs on an InP-based platform. The design process and rules, together with characterization results of test structures, are discussed. Static and dynamic measurements were performed for verification of the DLs’ performance in the wavelength and time domain. Additionally, a comparison between the simulation and characterization results is given, which confirms good agreement between measured and designed values.

Index Terms: Delay lines, optical time-division multiplexing (OTDM), photonic integration, indium phosphide.

1. Introduction

Delay lines (DLs) are important elements of various photonic devices and systems, specifically those dedicated to signal processing and/or transmission. They are typically deployed in optical beamformers for wireless communication [1], read-out units for Brillouin effect based sensors [2] and optical buffers [3]. Optical DLs are also an essential part of contemporary OTDM (optical time division multiplexing) systems which enable a significant increase of the capacity of a single fiber-optic communication link, while simultaneously keeping the driving electronics at relatively low speed. The result of OTDM is a serialized data stream with a bit-rate being a multiplication of the number of channels and the bit-rate in the individual input channel. The current record of the transmission rates reaches 1.28 Tb/s [4] for an on-off modulation scheme.

Multiplexing of parallel optical signals in the time domain can be realized by various methods. The simplest one is to use passive power combiners [5]–[7], but there are also techniques making use of optically active components and such phenomena as four wave mixing (FWM) [8], differential frequency generation (DFG) [9] and cross phase modulation (XPM) [10], which can be utilized to encode a signal carried in one wavelength channel onto another. Regardless of the multiplexing technique, the incoming parallel signals should be precisely aligned to ensure that the outcoming data stream is a sequence of pulses which do not overlap with each other. To do so, an accurately controlled delay has to be introduced to the input signals. This can be done either by adding an
extra propagation path or by decreasing the group velocity of the optical signal. It should be noted, however, that techniques of slowing light are still at an early stage of development and require sophisticated fabrication technology (photonic crystals [11]), specific operational conditions (low temperature [12]) or large dimensions (several km of optical fiber [13]), therefore are not commonly deployed.

By contrast, adding an extra propagation path is generally considered as a straightforward and very efficient way of introducing a time delay to the optical signals. Delay lines (DLs) can be fabricated as free space components making use of a set of mirrors. Another approach uses optical fibers differing in length so the signal in each branch travels along a different optical path. Unfortunately, such components are bulky and occupy much space, also the precision and stability of the delay is limited.

Following the common trend for miniaturization, it is also possible to fabricate delay lines in a form of photonic integrated circuits (PICs), using planar technology based either on dielectric or semiconductor materials. Photonic integrated circuits are playing a systematically increasing role in optical telecommunication networks and systems due to their significant advantages which they offer comparing to bulk components. These are compact size, low weight, low power consumption, suitability for high-speed operation (above 10 GHz) as well as a reduction of the number of interconnecting fibers. Furthermore, large scale production can significantly reduce the price of a single photonic circuit. Photonic integration technology allows fabrication of the delay lines as spirally folded waveguides [5], [14]–[17] or with the use of ring resonators [18], [19]. Both solutions are comparable in terms of size, but a serious drawback of the ring resonators is that long delays are obtainable only in the structures with a very high Q factor, which makes them extremely wavelength sensitive [18].

Spiral DLs have been already demonstrated using silica on silicon [14], [15], indium phosphide [16], [17] and silicon on insulator [5] based technologies. The first technology is characterized by the smallest group index, around 2.0, with silicon nitride as the waveguide core [15], while for the remaining two the group index takes values around 3.7 and 4.0, respectively. It makes these two technologies more efficient, as the same value of time delay may be obtained with the use of a shorter line. On the other hand, the silica on silicon waveguides are characterized by the lowest attenuation coefficient achieved so far, $\alpha = 0.01 \text{ dB/m}$ [14], using a very specific waveguide structure (light propagation is not supported in case of straight sections). However, both silicon-based platforms do not allow monolithic integration of the delay lines with optical amplifiers which are an important part of transceivers utilizing OTDM technique. By contrast, InP-based technology platforms enable integration of both active and passive elements. In this work we focus on optical delay lines fabricated as InP-based photonic integrated circuits, which are designed as composite building blocks for optical time division multiplexers [6], [7]. In the next sections the design procedures and rules are presented, followed by the simulation and characterization results.

2. General Design Rules

A delay line in a planar technology may be designed and fabricated as a looped-back Archimedean spiral, with continuously changing bending radius. The practical implementation may be significantly simplified, without loss of the quality, when it is constructed with discrete arcs. In the implementation presented here, the delay line starts with a series of half-circles going in one, e.g., clock-wise, direction. The radius of consecutive half-circles is gradually decreased by a specific number ($\Delta R$), thus forming a spiral. In the center of the structure there are two arcs, the radius of which is equal to the minimum value supported by the fabrication technology. These are used to go from the clock-wise (CW) to counter-clock-wise (CCW) orientation. Then the same set of half-circles as for the clock-wise direction follows. The spiral layout strongly reduces the space required for the component. Fig. 1 depicts the schematic of the delay line with annotated characteristic dimensions.

The total length of the line may be calculated using the equation:

$$l_t = 2\pi R_{\text{min}} + 2\pi \sum_{i=1}^{n} R_i$$  \hspace{1cm} (1)
where $R_{\text{min}}$ is the minimum bending radius allowed by the fabrication technology and $R_i$ denotes the radii of consecutive half-circles. The increment of the radii depends on the minimum separation between the adjacent waveguides $\Delta d$ and the waveguide width $w$:

$$\Delta R = \Delta d + w.$$  

The largest radius is

$$R_1 = 2R_{\text{min}} + \frac{\Delta R}{2} + (n - 1)\Delta R$$

where $n$ is the number of half-circles in one direction.

The waveguide junctions between (1) straight and curved sections (2) curved sections with different bending radius (3) curved sections with different direction of bending (CW and CCW) require a lateral offset in order to minimize the modal transition mismatch between the sections.

Typically there is a need for designing a delay line with a strictly specified and very accurate length. It can be controlled by means of various modifications of its parameters. The first step in the design process is determining of the number of half circles. As the total length grows discretely with the number of half-circles, it is necessary to choose the first possible number which gives the length larger than the targeted one. Then it can be tuned and controlled by changing the angle $\alpha_1$ of the first arc, the one with the largest radius. It results in a total length of

$$l_2 = 2\pi R_{\text{min}} + 2\pi \sum_{i=2}^{n} R_i + 2\alpha_1 R_1,$$

As the first and the last arcs do not have a common center, there will be a displacement of the input and output in the $x$ direction by

$$\Delta x = \Delta R \sin \alpha_1.$$

In principle the length can be designed with any chosen accuracy. However, in practice it will be limited by the capabilities and accuracy of the technology process, resulting in a slightly different group index than calculated.

The delay line occupies an area of approximately

$$S = \pi R_1^2.$$
where $R_1$ is the radius of the largest arcs. Some of the space in the center of the structure is sacrificed due to two half-circles used for looping-back the spiral. The amount of this space depends on the value of the minimum bending radius allowed by the technology.

Hereafter we will refer to the values specified by the generic integration technology process that is currently being trialed by Oclaro Ltd. (UK). The effective group index of the deeply-etched waveguide is $n_{\text{eff}} = 3.69$, at $\lambda = 1550$ nm for the TE mode and a waveguide width of $w = 1.5$ µm. The calculated minimum bending radius that prevents excess loss and polarization conversion is 80 µm.

The attenuation coefficient $L = 5$ dB/cm is determined by the scattering loss due to waveguide roughness (approximately 1–2 dB/cm) and by loss introduced by the dopants, which in this case has dominant character. The generic process supports both passive waveguides and electro-optic phase modulators. The dopants required for efficient operation of those modulators are present in all waveguide structures. The waveguide losses have been measured by the foundry using the Fabry–Perot technique. By comparing waveguides with and without p-doping the contributions from roughness and doping could each be quantified.

The maximum length of the delay lines is limited by the available chip area and, what is even more important, by optical loss in the long waveguide. For example, if we assume the maximum attenuation introduced by the component to be equal to 10 dB, the corresponding maximum line length will take the value of 2 cm, which in turn results in a time delay around 250 ps. Fig. 1 presents such a delay line, for which $R_1 = 315.25$ µm, $\alpha_1 = 29.32^\circ$ and the number of arcs in each direction is $n = 14$. The resulting structure has dimensions $620 \times 620$ µm$^2$.

3. Design and Fabrication

The delay lines presented in this paper were designed in an experimental generic integration technology based on indium phosphide (InP) and its compounds (InGaAsP). In such a generic technology, complex photonic ICs for a wide range of applications may be designed by using basic elements such as waveguides, phase modulators and semiconductor optical amplifiers. By combining basic building blocks, it is possible to construct composite building blocks that synthesize a higher-level function, which in turn can be used to build complicated circuits of various kinds. The application of the delay lines discussed here is an integrated optical time division multiplexer dedicated for use as a readout unit in a neutrino telescope experiment [6], [7].

To develop delay lines we used the deeply-etched straight and curved waveguides, provided by Oclaro Ltd., in the framework of the Dutch Memphis project [20] and the EU-project EuroPIC [21]. The waveguide core is formed by a multiple InGaAsP quantum well stack ($n = 3.38$) embedded between n-doped InP substrate ($n = 3.16$) and p-doped InP cladding ($n = 3.17$). The optimum values of the offsets between straight and curved sections have been calculated by maximizing the 2D modal field overlap integral of the fundamental modes in the straight and curved sections using the PhoeniX FieldDesigner software [22]. In the Fig. 2 the mask layout of the fabricated photonic integrated circuit is presented, containing test structures of example delay lines. These are labeled DLA, DLB, DLC, with a total length of 5.13 mm, 2.21 mm, and 1.26 mm, respectively. These DLs
have been used in the OTDM system described in our previous work [6], and their length was calculated to introduce 31.25 ps delay in a cascaded delay network of the 32 Gb/s multiplexer. For testing purposes they were placed in one arm of a Michelson interferometer, while the other arm was used as a reference. Additionally, to build the interferometer itself, we used 1 × 2 multi-mode interference (MMI) power splitters and MMI-based reflectors [23].

Fig. 2 presents the scheme of such test circuits. The chips have been fabricated in multi-project wafer runs and the facets have been anti-reflection (AR) coated.

4. Characterization

The schematic of the characterization setup for the test structures in Michelson configuration is shown in Fig. 3. As a light source we used either a tunable diode laser operating around \( \lambda = 1550 \) nm or a femtosecond-pulse laser with a pulse width of 150 fs, 80 MHz repetition rate and central wavelength \( \lambda_c = 1550 \) nm. The pulse duration of the laser will broaden to about 1 ps by the dispersion of the optical fibers and the on-chip delay lines. A polarization controller and a polarizing beam splitter were used to excite only the fundamental TE mode in the circuit. The optical signal was coupled to the chip with a polarization maintaining lensed fiber. The outgoing signal was measured with a power meter or a digital communication analyzer (DCA, a sampling oscilloscope).

First of all, we measured the frequency domain response of the test structures. The laser wavelength was tuned and the output power was continuously monitored. Fig. 4 presents the Fourier transform of the recorded spectra for three types of delay lines. The Fourier spectrum shows the lengths of the main cavities formed by the Michelson interferometer. Some additional peaks appear due to the non-zero reflection at the semiconductor-air interface. Even though the chip has been AR-coated, the power reflection coefficient \( R < -27 \) dB (as specified by the foundry) is still significant and the reflections define additional cavities between the facet of the chip and the two
reflectors. The length of the DLs has been determined using the group index of the waveguides $n = 3.69$, obtained from simulation, and this index was used to calculate the physical cavity lengths. The measurement results show a good agreement with the design values. The error of the length is smaller than 0.3% for all of the measured structures.

Fig. 5 presents the Fourier spectrum for three similar delay lines, this time placed in a Mach–Zehnder interferometer structure, so the cavity lengths are twice as short, since they are traversed only once. In this case the signal is much smoother and the extra peaks that were observed in the Michelson structures are absent. The influence of the reflection at the facet is significantly reduced. Previously there were parasitic cavities formed between the chip-air interface and the highly-reflective MMI reflector. On the contrary, in this case the Fabry–Perot cavities are formed by two AR-coated facets, each characterized by the power reflection coefficient of $R < -27$ dB.

Additional test structures have been designed in order to check whether and to what extend the performance of a spiral delay line differs from a straight waveguide section. The measurements, performed for the Michelson-type structures, showed that there are no significant differences. Fig. 6 presents the Fourier transform of the 2.21 mm DL. The shape of the main peak is the same for the
straight and the spiral structure. The position of other peaks, formed by the cavities between the facet and the MMI reflectors, are different due to a different distance between the facet and the input power splitter.

The measurement data has been used to verify the simulations performed with our photonic circuit simulator implemented in Agilent’s ADS [24]. The simulation model includes multiple internal reflections of the MMI-based power splitters and reflectors, reflections and losses at junctions between different waveguide sections, the facet reflection \( R = -27 \text{ dB} \), fiber-to-chip coupling and attenuation of the waveguides \( L = 5 \text{ dB/cm} \). Fig. 7 presents the comparison between results obtained in ADS and the measured data on the 2.21 mm DL. The position of the main peaks, formed by the Michelson cavity and the cavities originating from the facet and MMI reflectors, are in good agreement. Additionally, several peaks indicating the cavities created by internal reflections of the MMI-based components are observed both in simulation and measurement results.

Finally, to verify the time delay introduced by the delay lines a pulsed signal was coupled to the test structures. The output signal was measured by the DCA. Fig. 8 shows time traces for two of the structures with physical lengths of the lines of 5.13 mm and 2.21 mm, respectively. Due to the 30 GHz bandwidth of the DCA, the laser pulses are broadened, but the two peaks can be clearly resolved. The measured delays, 126.5 ps and 55 ps, are close to the design values, which were 126.3 ps (0.16% error) and 54.5 ps (0.9% error), respectively. However, a more exact determination of the time
difference is limited by the broadening of the laser pulses, which results in overlapping of the delayed and non-delayed pulse for the shorter line.

5. Conclusion
We presented the design process of compact optical delay lines for application as parameterized building blocks in photonic integrated circuits. Several test structures were designed and fabricated in a multi-project wafer in a generic InP-based technology. Characterizations in the wavelength domain and in the time domain were conducted to verify their performance and validate the simulation models.

For the technology process discussed here, the DLs can provide up to 250 ps of time delay, while occupying only 0.38 mm² of space and introducing 10 dB of losses, which are mainly caused by the waveguide doping. If necessary, the losses can be compensated by using monolithically integrated semiconductor optical amplifiers, however, at the cost of increased noise and utilized chip area.

There were no significant differences observed between the performance of a straight piece of waveguide and a spirally folded delay line. The measurements confirmed that application of the minimum bending radius of 80 μm, which was chosen as a result of performed simulations, does not introduce extra losses.

The characterization results of the components show very good consistency between simulated and measured values, with respect of both wavelength and time domain. Therefore, the simulation models applied here have been validated. This provides a designer a very good control over the output physical parameters of the structures, especially in terms of the introduced time delay. Furthermore, accurate simulation of parasitic effects such as spurious reflections of MMI-based components, gives insight how a delay line will perform in more complicated photonic integrated circuits.

The main advantages of the demonstrated delay lines are compact size, achievable time delay and precise control over the parameters. Even though they suffer from significant losses, this problem can be overcome by using amplifiers. Altogether, they can be applied in any photonic integrated circuit that requires an accurate time delay.

References


