New patterning paradigm? : selective deposition may be the way forward to the far reaches of device scaling after 7nm.

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New Patterning Paradigm?

Selective deposition may be the way forward to the far reaches of device scaling after 7nm.

APRIL 16TH, 2015 - BY: **MARK LAPEDUS (HTTP://SEMIENGINEERING.COM/AUTHOR/MARK-LAPEDUS/)**

Chip scaling is becoming more difficult at each process node, but the industry continues to find new and innovative ways to solve the problems at every turn. And so chipmakers continue to march down the various process nodes. But the question is for how much longer? In fact, at 16nm/14nm and beyond, chipmakers are finding new and different challenges, which, in turn, could slow IC scaling or bring it to a sudden halt one day.

To prevent those occurrences, chipmakers are working on a multitude of technologies. But one in particular is gaining steam in the lab—selective deposition. Some call the technology ALD-enabled nano-patterning.

At least in theory, selective deposition is a paradigm shift in chip manufacturing that could help extend IC scaling. But researchers still have some issues to solve to make this technology viable. And even then, it is not expected to appear until 7nm or 5nm.

For decades, chipmakers have used deposition, which is a process that deposits a blanket of thin material on a surface. In contrast, combining novel chemistries with atomic layer deposition (ALD) or molecular layer deposition (MLD) tools, selective deposition involves a process of depositing materials and films in exact places. Selective deposition can be used to deposit metals on metals and dielectrics on a device.

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The technology could replace some, if not many, of today's traditional patterning steps. In one possible futuristic flow, a tool selectivity deposits a self-assembled monolayer chemistry on a surface. This, in turn, forms a tiny mask or template on the surface at or near perfect alignment.

Others are working on a different approach called direct-write ALD. Using e-beam and multi-beam tools, the technology patterns the surface from the ground up.

"Patterning requires lithography, which is complicated in terms of resists, patterning the resists and etching," said Gregory Parsons, a professor in the College of Engineering at North Carolina State University. "What selective deposition could do, in principal, is reduce some of the steps in the fabrication of the device."

So, **Intel (http://semiengineering.com/kc/entity.php?eid=22846)** and others are taking a hard look at the technology. "That's why the patterning people are interested," said James Engstrom, a professor in the School of Chemical and Biomolecular Engineering at Cornell University. "They are getting very nervous as the feature sizes continue to shrink. Doing lithography, as traditionally defined, gets quite tricky."

Still, the questions are clear. Can selective deposition move from the lab to the fab? And if selective deposition works, how do chipmakers intend to use it?

Continuing Moore's Law

Meanwhile, according to the International Technology Roadmap for Semiconductors (ITRS), logic is supposed to scale to the 1.8nm node in the 2025 timeframe. It's debatable if logic will extend that far, but some are working on it. "My target is to approach 1.5nm," said E.S. Jung, executive vice president of the semiconductor R&D center at **Samsung (http://semiengineering.com/kc/entity.php?eid=22865)**, at a recent event. "How can we make it happen? We need tools, materials and open innovation."

To reach the near-term nodes, chipmakers are taking the conventional lithographic route. For example, they plan to extend optical lithography to at least 7nm. By then, IC makers hope that extreme ultraviolet (**EUV (http://semiengineering.com/kc/technology.php?tid=31045)**) **lithography (http://semiengineering.com/kc/knowledge_center.php?kcid=80)** is ready.

In either case, chipmakers require some form of **multi-patterning (http://semiengineering.com/kc/knowledge_center.php?kcid=196)**. Multi-patterning requires good overlay between the various masks. But overlay errors will likely increase as the industry moves from **double patterning (http://semiengineering.com/kc/knowledge_center.php?kcid=197)** and beyond. "Edge placement error control with pitch division becomes more difficult due to (the) non-scaling nature of overlay errors," said Yan Borodovsky, a senior fellow and director of advanced lithography at Intel.

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Borodovsky contends that multiple patterning doesn't threaten **Moore's Law (http://semiengineering.com/kc/knowledge_center.php?kcid=74)**, but rather edge placement error (EPE) is the real problem. EPE is measured as the difference between the intended and printed features in a layout.

"Edge placement error and overlay are clearly going to be challenging," said Uday Mitra, vice president and chief technology officer for the Etch Business Unit at **Applied Materials (http://semiengineering.com/kc/entity.php?eid=22817)**. "In pitch division, you can do it 32 times. But getting the patterns exactly where you want them to be is the fundamental challenge. At 5nm, it becomes very, very big."

In the distant future, the various next-generation lithography (NGL) technologies may not solve the EPE issue. So, the industry is looking at novel techniques like selective deposition to solve some of the problems.

To some degree, selective deposition already exists. For example, **Lam Research (http://semiengineering.com/kc/entity.php?eid=22820)** has offered an electroless deposition tool, which is used to deposit cobalt capping layers in dual damascene structures. "People are also looking at selective dielectric deposition," said Dave Hemker, senior vice president and chief technology officer at Lam Research. "In that, there is a bunch of opportunities there. I don't know if there are any good solutions yet. But that's why we are doing R&D."

What is selective deposition?

In the lab, researchers are developing selective deposition processes using ALD and MLD. Used in today's chip manufacturing, ALD deposits material layer-by-layer at the atomic level.

In selective deposition, ALD is used to selectively deposit inorganic compounds. MLD and ALD are similar, but MLD deals with organic materials. "The basic concept is that you have a substrate, where there are multiple materials present on the surface," Cornell's Engstrom said. "Perhaps they have been patterned in some way in some previous step. You might have some areas that might be a metal. Other areas might be a dielectric. Maybe another area is a semiconductor. So the idea is that you want to add material and you want to only deposit on those areas that you wish to deposit on."

In the future, though, selective deposition could evolve into what some researchers call ALD-enabled nano-patterning. According to the Eindhoven University of Technology, there are three basic approaches in ALD-enabled nano-patterning—lift-off; area-selective ALD by area-activation; and area-selective ALD by area-deactivation.

In the lift-off approach, a resist is applied to the surface, except for the area of the desired structure. Then, a film is deposited on the entire surface using ALD. The film and resist are dissolved, which results in the final structure.

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The Eindhoven University of Technology, for one, is working on another approach—direct-write ALD. This is based on an area-selective ALD by an area-activation technique. This makes use of electron-beam induced deposition (EBID) or ion-beam induced deposition (IBID). "We combine the advantages of electron-beam patterning with the advantages of ALD," said Erwin Kessels, a professor at the Eindhoven University of Technology. "The patterning by the e-beam can take place in a SEM system, but it can also be done in a multi -electron beam system."

For example, Mapper Lithography's multi-beam e-beam tool could be used in direct-write ALD, Kessels said. All told, direct -write ALD is a bottoms-up patterning process, which does not require a photoresist or an etch step.

"In this method, we first pattern the surface with an ultra-thin seed layer using electron-beam induced deposition at a thickness of <1nm," Kessels said. "Subsequently, we increase the thickness of this pattern by selective-area ALD. The ALD growth takes place only in the pattern."

In the lab, the technology has enabled the development of several structures, including platinum (Pt) nanowires at about 10nm. "The method is most promising for the selective deposition of metal nano-contacts. For example, it could be used for contacts in carbon nanotube transistors or graphene devices," he said.

"There is still a long way to go for bringing this method from lab to fab. The repeatability and reliability of the method still needs to be addressed. It is also not yet clear whether the technique has a sufficient yield and is economical," he said. "Another big challenge is the extension of the technique to other materials. The technique works well for Pt nano-contacts, and we have also promising results for other Pt-group metals, such as Pd (palladium) and Ru (ruthenium), as well. The challenge will be to deposit materials, such as oxides and nitrides by direct-write ALD as well. This will require clever chemistries, including new ALD processes as well as the screening and development of ALD precursors."

For some time, meanwhile, researchers have been working on the third approach—area-selective ALD by area-deactivation. This technology makes use of self-assembled monolayer (SAM) chemistries, which are based on long organic molecules.

In the basic flow, a SAM-based chemistry is applied on a surface, forming a mask on the surface. Then, a material using ALD is applied to the surface. The ALD growth appears in the places not covered by the mask. "Instead of a physical mask to align, you would want to use the chemistry of the surface to do the alignment," said Parsons of North Carolina State University. "In principal, we get perfect alignment or something close to perfect alignment."

Still, there are challenges with selective deposition in general. "The main challenge is basically to understand and control thin-film nucleation," Parsons said. "We need to

understand what the first reactions are that lead to deposition. And how do we either enhance that step or avoid that step."

It's too soon to say if selective deposition will work. It will require more funding and support to bring the technology from the lab to the fab. But is the industry willing to take a gamble and fund the technology? And are there enough R&D dollars to go around?

Today, the industry continues to pour money into EUV. To a lesser extent, it is also investing in DSA, multi-beam and nano-imprint. In addition, the industry needs more funding for next-generation inspection and metrology. And that's just the tip of the iceberg.

Commenting on the future of lithography in general, Aki Fujimura, chief executive at **D2S (http://semiengineering.com/kc/entity.php?eid=22864)**, said: "Different types of applications may require different things. So at 7nm and 5nm, different people are going to have different strategies. That's not necessarily good for the industry, because the investments get divided."

It also leaves the industry facing big challenges of triple and quadruple patterning at 10nm, which will be significantly more difficult to master than double patterning at 16nm/14nm because the current tools can't account for all of the different colors and possible unknowns.

"At 10nm and below, the challenges will be in the tools, the process and the complexity," said David Abercrombie, advanced physical verification methodology program manager at **Mentor Graphics (http://semiengineering.com/kc/entity.php?eid=22017)**. "We're seeing more differences between foundries as we move forward, too. At 20nm and 16/14nm, it was the same basic layers and simple double patterning. At 10nm, there is more diversity in how they approach multi-patterning. There is still double patterning there, but depending on the layer and the foundry, it might be a completely different experience."

At a macro level, what changes is that the tools, the process and the design flow become much more interdependent, so a change in any one of those affects the other two. And considering that new processes, tools and flows are all in flux at 10nm and beyond, it may take even longer to sort out than usual."

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