

A 5.3 GHz 16b 1.75 GS/S wideband RF mixing-DAC achieving IMD

Citation for published version (APA):

Bechthum, E., Radulov, G. I., Briaire, J., Geelen, B., & Roermund, van, A. H. M. (2015). A 5.3 GHz 16b 1.75 GS/S wideband RF mixing-DAC achieving IMD. In *2015 IEEE International Solid-State Circuits Conference (ISSCC), 22-26 Februar 2015, San Francisco* (pp. 1-3). Institute of Electrical and Electronics Engineers. <https://doi.org/10.1109/ISSCC.2015.7062980>

DOI:

[10.1109/ISSCC.2015.7062980](https://doi.org/10.1109/ISSCC.2015.7062980)

Document status and date:

Published: 01/01/2015

Document Version:

Publisher's PDF, also known as Version of Record (includes final page, issue and volume numbers)

Please check the document version of this publication:

- A submitted manuscript is the version of the article upon submission and before peer-review. There can be important differences between the submitted version and the official published version of record. People interested in the research are advised to contact the author for the final version of the publication, or visit the DOI to the publisher's website.
- The final author version and the galley proof are versions of the publication after peer review.
- The final published version features the final layout of the paper including the volume, issue and page numbers.

[Link to publication](#)

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
- You may freely distribute the URL identifying the publication in the public portal.

If the publication is distributed under the terms of Article 25fa of the Dutch Copyright Act, indicated by the "Taverne" license above, please follow below link for the End User Agreement:

www.tue.nl/taverne

Take down policy

If you believe that this document breaches copyright please contact us at:

openaccess@tue.nl

providing details and we will investigate your claim.

9.6 A 5.3GHz 16b 1.75GS/s Wideband RF Mixing-DAC Achieving IMD<-82dBc up to 1.9GHz

Elbert Bechthum¹, Georgi Radulov¹, J. Briaire², Govert Geelen², Arthur van Roermund¹

¹Eindhoven University of Technology, Eindhoven, The Netherlands

²Integrated Device Technology, Eindhoven, The Netherlands

Cellular multicarrier transmitters for communication infrastructure require both high linearity and large bandwidth (BW) at GHz frequencies. The combination of multicarrier GSM, WCDMA and LTE typically requires IMD<-80dBc and SFDR>80dBc in a large transmit bandwidth of 300MHz and at an output frequency of up to 3.5GHz and beyond. Current-Steering (CS) Nyquist DACs have large BW, but their linearity drops for increasing output frequencies [1]. A separate mixer is therefore needed to generate an RF signal with high linearity. A Mixing-DAC integrates the function of the mixer and DAC together. Using a Mixing-DAC can result in different architecture trade-offs which potentially enable a reduction of the cost and power consumption, while improving the linearity at high frequencies. The state-of-the-art Mixing-DACs attain linearity by means of $\Delta\Sigma$ modulation [2,3] or low sample rate [4], but this results in a limited BW and does not result in a linearity better than IMD=-71dBc. Even a GaAs implementation [5] only achieves IMD=-70dBc while consuming 1.2W.

This paper proposes a CS Mixing-DAC architecture that provides both high linearity and large BW at an output frequency of up to 5.3GHz. This is enabled by using the architecture depicted in Fig. 9.6.1. The key properties of this architecture are: local mixing per current cell, multilevel cascoding with double bleeding currents and elevated bulk voltage, supply-isolated LO driver, and sort-and-combine calibration [1].

The 16b converter is segmented into a 6b unary part and a 10b binary part. The 10 binary current cells are accurately scaled versions of the unary current cell. A current cell contains a cascoded current source (M_0, M_1), data switches (M_2, M_3), mixer switches (M_4, M_7) and output cascodes (M_6, M_5). The measurement probes (M_{8m}, M_{9m}) for the error measurement can individually connect each current cell to the measurement circuit during calibration. The digital baseband signal is supplied to the Data switches while the LO signal up-converts it to the RF output frequency. The switching signals for the data and mixer switches are generated using CML buffers. This prevents signal-dependency in the supply current consumption and enables control of the cross-over point of the switching signals. Coupling of the LO signal to the output is minimized by careful layout.

To maintain high linearity at RF frequencies this Mixing-DAC uses local mixing per current cell, a balanced LO distribution tree and a global LO driver. Local mixing means that the mixing is implemented locally in each current cell, as opposed to using one global mixer at the output. Local mixing offers the highest linearity, since it essentially is an inherently linear 1-bit system, as theoretically argued in [6]. Tight control over the mismatch between the mixers in the array of current cells is required [7]. The timing errors in the mixer function can originate from both the LO signal and the mixer switches. The single global LO driver and the carefully designed distribution tree eliminates timing mismatch between the distributed LO signals. Since the mixer is fully differential, mismatch in the mixer switches causes mainly duty-cycle timing errors and almost no delay timing errors [7]. These duty-cycle errors generate predominantly out of band distortion, which can easily be filtered out. Other important mismatches between the current cells are: static mismatch of the current sources and timing mismatch of the data switches. These are calibrated using the sort-and-combine method [1]. Note that its use in Mixing-DACs is novel, maintaining the calibration advantages even at RF frequencies.

The multilevel cascoding strategy ensures that each function of the current cell is isolated from the other functions. This implies that every transistor, apart from its main function, also acts as a cascode. The main functions are: reference current generation (M_0), data switching (M_2, M_3) and mixing (M_4, M_7). Some state-of-the-art Mixing-DACs combine multiple functions in one transistor, e.g. use the current source transistor also as a mixer [3], which hampers the independent optimization for each function. The separate transistor level per function of the proposed architecture enables the precise optimization for each function. The cascoding transistors (M_1, M_6, M_5) and double bleeding currents for the mixer and the output cascode ($I_{bleed,oc}$ and $I_{bleed,mix}$) are used to protect the most sensitive nodes and to increase the output impedance. The mixer operates at the LO frequency and hence driving its gate capacitance is critical. Therefore, the mixer is implemented using 1.2V thin-oxide devices. To provide an optimal

voltage range of 1.8V for the 4 cascoded thin-oxide transistors, the operating voltages of the mixer are shifted using a triple-well technology. This improves the Mixing-DAC performance without compromising reliability. The required elevated bulk voltage is generated on-chip.

The required elevated supply voltage for the LO driver is generated from the 3.3V power supply using an internal regulator. The regulator also ensures that the local supply voltage remains clean.

The proposed architecture is implemented using a triple-well 65nm CMOS technology with 1.2V and 3.3V supplies. A micrograph of the die of the dual-Mixing-DAC with two Mixing-DAC cores and the digital front-end is shown in Fig. 9.6.7. The area of one Mixing-DAC core is 1.6mm². The nominal full-scale output current is 20mA in a differential 50 Ω load. To synchronize the switching activities of the mixer and data switches, f_{LO} is an integer multiple of F_S , and the phase between the two signals is optimally set. The typical configuration is: $F_S=1.75GS/s$, $f_{LO}=1.75GHz$ and $f_{in}=155MHz$. The power consumption is 710mW with two Mixing-DAC cores and 380mW with only one Mixing-DAC core enabled. The nominal output power of a single-tone signal in the high Nyquist band at $f_{LO}+f_{in}\approx 1.9GHz$ is -8.0dBm. Due to losses in the measurement setup, the signal power at the spectrum analyzer is -14.9dBm. In the remaining part of this paper, the measurement results are not corrected for this loss. The output spectrum of a dual-tone signal is shown in Fig. 9.6.2, where the largest odd-order IMD is IMD₅= -83.9dBc. In a radio transmitter, a transmit filter attenuates spurious emissions at typically >150MHz from the carrier. Therefore, the SFDR in a Reduced Bandwidth (RB) of 300MHz is relevant. The single-tone SFDR_{RB} is 75.1dBc. The SFDR in the full Nyquist band is 66.3dBc, which is limited by HD₂. The measured thermal noise power, including the measurement setup, is -168dBm/Hz at 10MHz from the output frequency.

The results of IMD and SFDR measurements for various values of f_{in} are shown in Fig. 9.6.3, where $F_S=f_{LO}=1.5GHz$. Both the high and low Nyquist band are shown. Figure 9.6.4 shows the measurement results for $f_{LO}=1.3$ to 5.1GHz, $f_{LO}=n\cdot F_S$ and $f_{in}=155MHz$. Since most publications measure with a small RB interval of 20MHz or less, the RB interval of each SFDR_{RB} data point is indicated in Fig. 9.6.4 with black interval bars. The linearity up to 1.5GHz is almost constant and is limited by the baseband-frequency part of the converter. Above 1.5GHz, cell-dependent timing errors in the mixer cause the linearity to degrade for increasing output frequency. However, the presented chip outperforms [2-5] in terms of IMD and SFDR_{RB}, while measuring in the largest RB.

A 13-tone signal at 2.0GHz is shown in the top of Fig. 9.6.5, which ultimately demonstrates that the proposed Mixing-DAC architecture realizes the RF digital-to-analog conversion with 81dBc linearity in 300MHz BW. The excellent noise and distortion performance is further demonstrated using a 4-channel LTE signal at 2.0 GHz, shown in Fig. 9.6.5 bottom. A performance summary for $f_{out}\leq 1.9GHz$ and $f_{out}=4.1GHz$ is given in Fig. 9.6.6. Also a comparison with previously reported work is given.

The reported measurement results (IMD<-82dBc, SFDR_{RB300MHz}>75dBc for $f_{out}\leq 1.9GHz$) validate that the proposed architecture can simultaneously provide high linearity and large bandwidth.

Acknowledgements:

The authors are grateful to the engineers of the high-speed data converter team of IDT and of the MsM group of the TU/e for their support and advice.

References:

- [1] H. van de Vel et al., "A 240mW 16b 3.2GS/s DAC in 65nm CMOS with <-80dBc IM3 up to 600MHz," *ISSCC Dig. Tech. Papers*, pp. 206-207, Feb. 2014.
- [2] A. Jerng, Sodini, C.G., "A Wideband $\Delta\Sigma$ Digital-RF Modulator for High Data Rate Transmitters," *IEEE J. Solid-State Circuits*, vol.42, pp. 1710-1722, Aug. 2007.
- [3] S. Luschas et al., "Radio frequency digital-to-analog converter," *IEEE J. Solid-State Circuits*, vol.39, pp.1462-1567, Sept. 2004.
- [4] P. Elooranta et al., "A WCDMA Transmitter in 0.13 μ m CMOS Using Direct-Digital RF Modulator," *ISSCC Dig. Tech. Papers*, pp. 340-341, Feb. 2007.
- [5] M. Choe et al., "A 1.6GS/s 12b Return-To-Zero Gaas RF DAC for Multiple Nyquist Operation," *ISSCC Dig. Tech. Papers*, pp.112-113, Feb. 2005.
- [6] E. Bechthum et al., "Systematic analysis of the impact of mixing locality on Mixing-DAC linearity for multicarrier GSM," *IEEE International Symp. Circuits and Systems*, pp. 241-244, 2012.
- [7] E. Bechthum et al., "A novel timing-error based approach for high speed highly linear Mixing-DAC architectures," *IEEE International Symp. Circuits and Systems*, pp. 942-945, 2014.

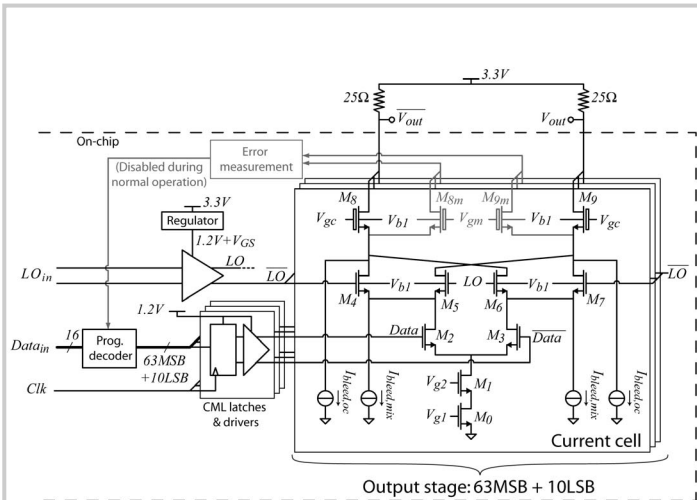


Figure 9.6.1: Schematic of the Mixing-DAC architecture.

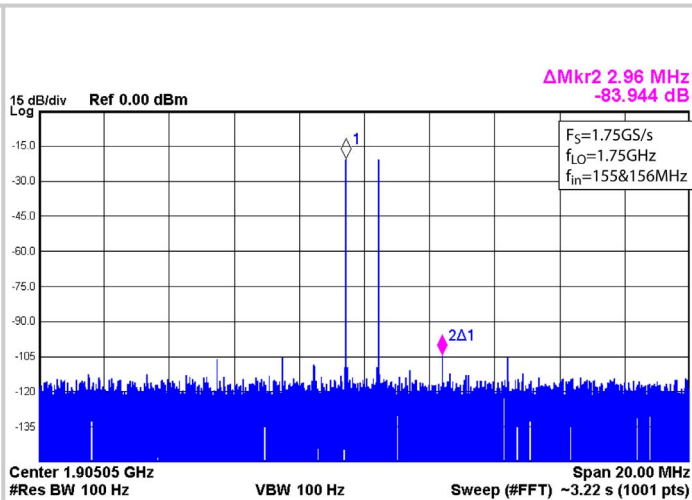


Figure 9.6.2: IMD=-83.9dBc at an output frequency of 1.9GHz.

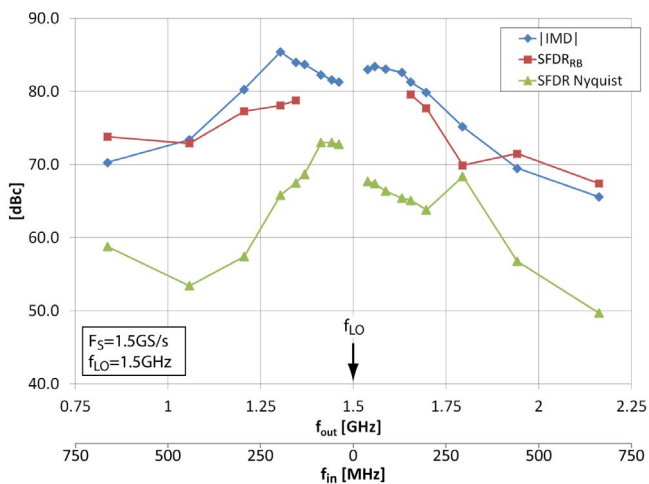


Figure 9.6.3: Two-tone IMD and single-tone SFDR (RB=300MHz) for various values of f_{in} .

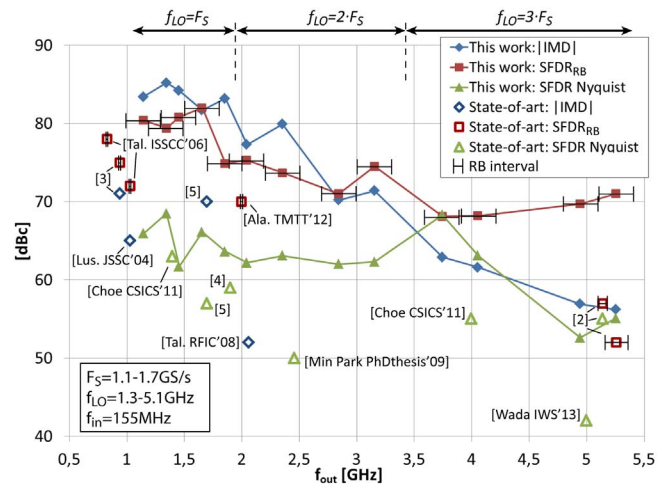


Figure 9.6.4: Two-tone IMD and single-tone SFDR (RB=300MHz) as a function of the output frequency.

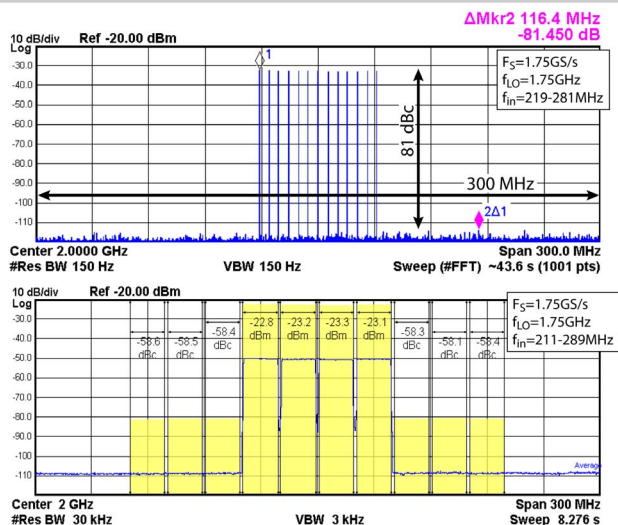


Figure 9.6.5: Multi-tone and modulated output signals result in a large clean bandwidth.

| | This work | [5] | [4] | [2] | [3] |
|---------------------------------|---------------------|---------------------|-------------------|--------------------------|--------------------------|
| Technology | 65nm CMOS | 80GHz f_T GaAs | 130nm CMOS | 130nm CMOS | 180nm CMOS |
| Core area | 1.6 mm ² | 3.2 mm ² | 1 mm ² | 0.7 mm ² | - |
| Resolution | 16 bit | 12 bit | 10 bit | 3 bit ($\Delta\Delta$) | 3 bit ($\Delta\Delta$) |
| Max. sample rate | 1.75GS/s | 1.6 GS/s | 0.15 GS/s | 2.63 GS/s | 0.51 GS/s |
| Max. effective signal bandwidth | 875 MHz | 800 MHz | 75 MHz | ~300 MHz | ~30 MHz |
| Max. LO frequency | 5.1 GHz | 1.6 GHz | 1.9 GHz | 5.25 GHz | 1.03 GHz |
| Max. output freq. | 5.26 GHz | 2.4 GHz | 1.92 GHz | 5.26 GHz | 0.94 GHz |
| f_{out} | ≤ 1.9 GHz | 4.1 GHz | 1.7 GHz | 1.92 GHz | 5.26 GHz |
| Core power consumption | 380 mW | 380 mW | 1200 mW | 92mW | 187mW |
| IMD | < -82 dBc | -62 dBc | -70 dBc | - | -71 dBc |
| SFDR Nyquist | > 62 dBc | 63 dBc | 57 dBc | 50 dBc | 52 dBc |
| SFDR _{RB} | > 75 dBc | 68 dBc | - | 52 dBc | 75 dBc |
| @ RB | 300 MHz | 300 MHz | - | 200 MHz | 17.5 MHz |
| NSD | < -165 dBm/Hz | -167 dBm/Hz | - | -146 dBm/Hz | - |
| 1-ch. ACLR: LTE | < -69 dBc | -73 dBc | - | - | - |
| 1-ch. ACLR: WCDMA | < -74 dBc | -77 dBc | - | -58 dBc | - |

Figure 9.6.6: Performance summary and comparison.

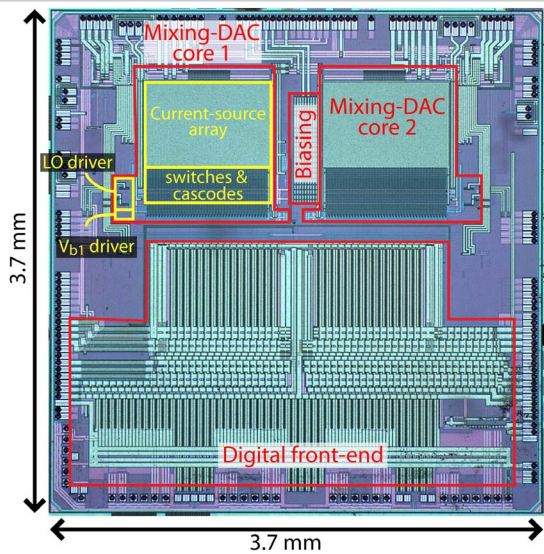


Figure 9.6.7: Die micrograph with bond wires removed.