A novel timing-error based approach for high speed highly linear Mixing-DAC architectures

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***Abstract*—In current steering Mixing-DACs with local mixing, timing errors between the current cells is a major concern. This paper considers two types of random timing errors: delay and duty-cycle. Analysis shows that the Mixing-DAC is sensitive to delay errors, but much less sensitive to duty-cycle errors. For the required high spectral purity of future 4GHz multicarrier GSM ($SFDR_{RBW}$=85dBc), the delay spread $\sigma(delay)$ should be <36fs. Therefore, only mixing in the output stage with a single LO driver can achieve the desired linearity.**

The presented analysis shows that the timing of the binary cells in the segmented converter is very important, especially in a back-off scenario. Simulations confirm that accurate capacitance scaling at the high-frequency nodes of the binary current cells is crucial. A new, back-off aware segmentation trade-off is proposed, which shows the impact of the $SFDR_{RBW}$ and back-off requirements on the segmentation choice.

The proposed methods result in an optimal Mixing-DAC architecture, implemented in 65nm CMOS, with a simulated performance of $SFDR_{RBW}$=86dBc at 4GHz output frequency and -16dB$_{FS}$/tone output power (10dB back-off).

I. Introduction

Highly linear wideband transmitters are needed for the transmission of multicarrier GSM signals[1]. Using a transmitter with Mixing-DAC[2] offers many advantages[3]. Fig. 1 shows such a transmitter. The required linearity of a Mixing-DAC in a multicarrier GSM transmitter is very high: $SFDR_{RBW}$>85dBc (Spurious Free Dynamic Range in a Reduced BandWidth).

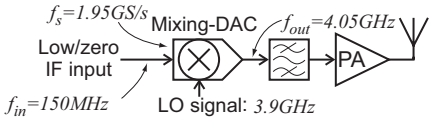


Fig. 1. RF transmitter based on a Mixing-DAC

A Current Steering (CS) Mixing-DAC with local mixing[3] can be very linear if the responses of all 1-bit switched current sources (current cells) are uncorrelated and identical, or ideally scaled for binary current cells. For high linearity at high frequency, both timing and amplitude of the 1-bit cells should be considered. The amplitude matching in CS (Mixing-)DACs has been thoroughly researched, and many intrinsic and correction methods exist[4]. However, the synthesis of a Mixing-DAC architecture with the focus on timing errors is not discussed in open literature, while this is critical for achieving high linearity at high frequency.

This paper focuses on local mixing (mixing inside DAC current cells) since that results in a better linearity than global mixing (separate mixing after DAC) [3]. With local mixing, the timing synchronization between the current cells is important, since timing errors degrade the linearity.

Current steering Mixing-DACs predominantly use a segmented implementation, with a unary scaled MSB part and a binary scaled LSB part. Without loss of generality, the analysis in this paper assumes a 16 bit Mixing-DAC with a segmentation of 6bit unary MSB and 10 bit binary LSB, implemented in 65nm CMOS. The presented analysis is also applicable to other segmentations. The used signal frequencies are as given in Fig. 1.

Timing errors in the unary (MSB) part are only randomly distributed. No systematic timing errors are present since each cell is identical. The random timing errors dictate the most optimal Mixing-DAC architecture, which is discussed in section II. For multicarrier transmitters, the power of a single carrier is much lower than the total full scale output power. This significantly increases the importance of timing errors in the binary (LSB) current cells. In the binary part, systematic timing errors are dominant over random timing errors. The systematic binary timing errors are discussed in section III.

II. Timing errors

Random timing errors predominantly can occur in three signals in the Mixing-DAC unit cells: $Data$ input, LO input and the $Mixed$ signal (see Fig. 3(a) for $Data$ and LO, and Fig. 3(b) for $Mixed$). Only timing error *differences* between the current cells are relevant since they lead to non-linear distortion. The timing errors are assumed to be Gaussion distributed with zero mean.

Two types of timing errors are considered: the delay and duty cycle. An ideal periodic square waveform and the same waveform with timing errors are shown at the left of Fig. 2. The difference between the base waveform and the waveforms with timing errors, and the spectra of these differences, are also shown. For all practical values of the timing errors, the error spectrum of the Δ-waveform with a delay timing error only contains odd harmonics of the base frequency, and the duty-cycle error spectrum only contains even harmonics of the base waveform. This spectral difference is important for the Mixing-DAC architecture analysis.

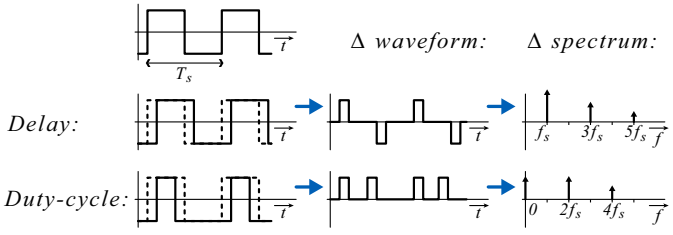


Fig. 2. Time domain and spectral characteristics of timing errors

For all practical segmentations and for a full-scale signal, the response of the MSB unary current cells determines the performance. In this section the binary current cells are thus assumed to be ideal. The next subsections discuss possible Mixing-DAC architectures and the impact of timing errors at three nodes in a Mixing-DAC: LO, $Data$ and $Mixed$ signal. The value of the $SFDR_{RBW}$ in a a 200MHz band around $f_{out} = F_{LO} + f_{in}$ is used as a measure of the spectral purity.

A. *Architecture options*

The sensitivity to timing errors highly depends on the Mixing-DAC architecture. The mixing operation can be done in the output stage (see Fig. 3(a)) or earlier in the signal chain, e.g. in the driver using a mixing-driver (see Fig. 3(b)). Another degree of freedom is the locality of the LO driver, which can be local or global. Mixing-DAC architectures with mixing in the output stage, and with global and local LO driver, are shown in Fig. 3(a) and Fig. 3(c) respectively. For the mixing-driver architecture, the choice of a local or global driver does not influence the results of the timing error analysis.

In this paper, intrinsic timing error sensitivity is compared. Numerous timing error calibration techniques for CS DACs exist [5]–[7] but they are not considered since it is assumed that they are equally applicable to all proposed architectures.

B. Data *input timing*

Timing errors in the $Data$ input signal are extensively discussed in publications regarding CS DAC timing errors[5]–[9]. The same conclusions and calibration techniques apply to all proposed Mixing-DAC architectures, which is verified with simulations. Therefore, $Data$ timing errors have no influence on the architecture comparison.

C. LO *input timing*

Sensitivity to LO timing errors is specific for Mixing-DACs. Fig. 4(a) shows the results of transistor level simulations of the circuit of Fig. 3(a) at F_{LO}=3.9GHz, where the two types of timing errors are deliberately introduced in the LO input. Each current cell has its own independent random timing error, which is fixed for one trial of the Monte Carlo simulation. To isolate the nonlinear distortion due to timing errors, other error sources are eliminated: $R_L \approx 0$ (to reduce output related effects[3]) and ideal drivers and ideal current sources are used.

A 99% yield $SFDR_{RBW}$ of 85dBc at F_{LO}=3.9GHz requires $\sigma(delay)$<36fs and $\sigma(duty\text{-}cycle)$<0.85ps. Hence, the Mixing-DAC is very sensitive to delay errors, but at least 20 times less sensitive to duty-cycle errors. The cause for the difference in sensitivity to the two types of timing errors can be seen in Fig. 5, where two output spectra with added delay and duty-cycle timing errors in the LO signal are shown. The delay timing errors cause spurs around F_{LO} (which is close to the output band) while the duty-cycle timing errors create spurs around $2{\cdot}F_{LO}$. This can be expected, see Fig. 2, since the delay error spectrum contains energy at the fundamental frequency (i.e. F_{LO}), while the duty-cycle error spectrum contains energy at double this frequency (i.e. $2 \cdot F_{LO}$).

With a single common LO signal (i.e. a single global LO driver, see Fig. 3(a)) and output stage mixing, predominantly

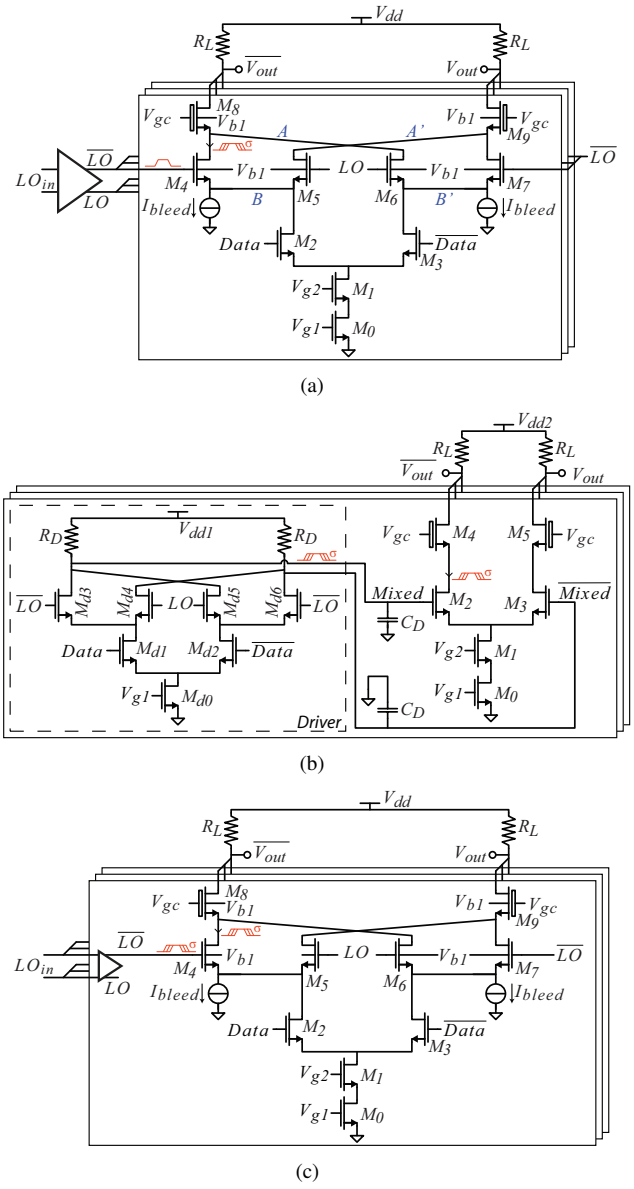
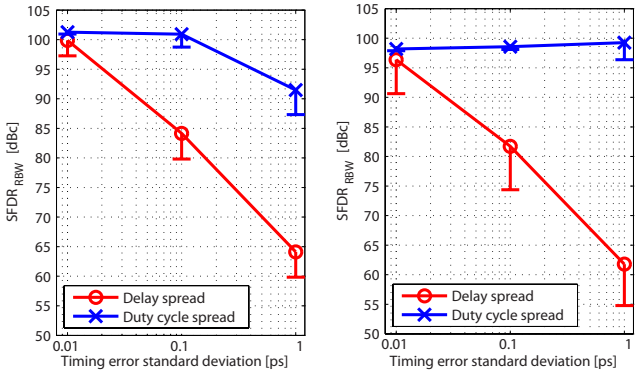


Fig. 3. Three local Mixing-DAC architectures with annotated timing errors: (a), output stage mixing with a single global LO driver [3]; (b), proposed example of mixing in the digital domain with mixing-driver; (c), proposed mixing in the output stage with local LO driver



(a) LO timing errors in Fig. 3(a) (b) $Mixed$ timing errors in Fig. 3(b)

Fig. 4. Resulting $SFDR_{RBW}$ of timing errors (error bar=90%, #trials=20)

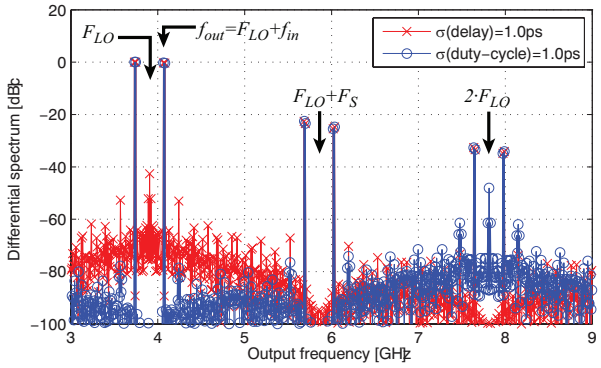


Fig. 5. Schematic level simulation, comparing the spectral impact of delay and duty cycle timing errors

duty-cycle timing errors occur. The duty-cycle timing errors mainly originate from threshold mismatch and gain mismatch in the mixing transistors, M_4-M_7 in Fig. 3(a). This can be verified in the results of Monte Carlo mismatch simulations for the architecture of Fig. 3(a), which is shown in Fig. 6, where only the mixing transistors have mismatch. The mismatch-induced timing errors are almost exclusively duty-cycle timing errors, and the standard deviation of both timing error types are less than the values required for $SFDR_{RBW}$<85dBc.

A significant delay error can only originate from imperfect layout of the LO distribution or output recombination structure. Careful layout of the corresponding tree structures can reduce the expected delay error to less than ±5fs.

A local LO driver, as proposed in Fig. 3(c), introduces additional duty-cycle timing errors *and* delay timing errors, which can easily exceed 200fs, while <36fs is required.

D. Mixed *signal timing*

Fig. 4(b) shows the results of a Monte Carlo transistor level simulation of the Mixing-DAC architecture with mixing-driver of Fig. 3(b), where $R_L \approx 0$, and with ideal current sources, and ideal $Data$ and LO drivers. In each current cell with mixing-driver, a random timing error is deliberately introduced in the $Mixed$ signal (i.e. output of mixing-driver). Again, the performance is very sensitive to delay timing errors: $\sigma(delay)$<16fs for $SFDR_{RBW}$>85dBc.

Mismatch in the mixing-driver, e.g. in the current source (M_{d0} in Fig. 3(b)), load resistor value (R_D) or (parasitic) load capacitance (C_D) of the CML driver, can generate large timing errors. Schematic level simulations show that a mismatch of σ=3% in the R_DC_D time-constant results in a delay timing error of $\sigma(delay)$=0.26ps, while $\sigma(delay)$<16fs is required.

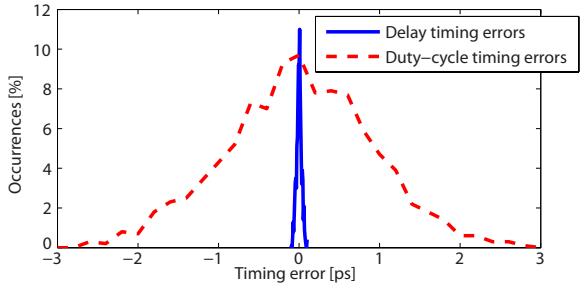


Fig. 6. Simulated LO timing errors due to mixer mismatch

E. Architecture choice

The linearity of a Mixing-DAC architecture is very sensitive to delay timing errors in the LO and $Mixed$ signal. A local LO driver or mixing in the driver using a mixing-driver is expected to lead to large delay timing errors. However, local mixing in the output stage with a single global LO driver (Fig. 3(a)) does not exhibit delay timing errors in the sensitive signals. Therefore, the latter architecture is preferable for high linearity at high frequency.

III. Binary Optimization

Current multicarrier transmitters use output power back-off, which increases the importance of the binary current cell matching and alters the segmentation trade-off.

A. Output power back-off

One of the characteristics of a multicarrier transmitter is that the power of each single carrier is lower than the full scale signal, i.e. back-off (typically -16dB$_{FS}$/tone). In such a transmitter, the signal of one tone only uses a small subset of the unary current cells, effectively changing the segmentation of the Mixing-DAC. Hence, the binary part of a segmented Mixing-DAC becomes increasingly important. Fig. 7 shows the spectra of a full-scale dual-tone signal at -6dB$_{FS}$/tone, and a signal at -16dB$_{FS}$/tone (10dB back-off). While the difference in signal power is 10dB, the spur-floor is at the same absolute level, reducing the $SFDR$. The cause of this high spur-floor is systematic timing errors between the binary current cells.

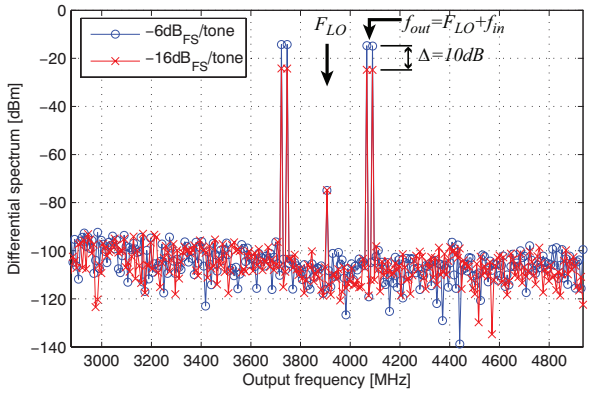


Fig. 7. Spectral compariston between full-scale output and back-off

B. Binary matching

In a traditional DAC output stage, only one critical high-speed node should be rigorously optimized for binary scaling: the source of the output cascodes. In the chosen Mixing-DAC architecture of Fig. 3(a), two sets of high-speed nodes need precise optimization: the source of the output cascodes (nodes A and A') and the source of the mixer (nodes B and B'). The response of these nodes should be exactly scaled with respect to the unary current cell. To guarantee this binary matching, the capacitance values and the gain of the transistors at these nodes should scale exactly with the binary current cell scaling.

To illustrate the sensitivity of the performance to capacitance deviations in the binary current cells, Fig. 8 shows the $SFDR_{RBW}$ as a function of the parasitic capacitance at the source of the output cascodes (A and A') of the three most

significant binary cells (B9, B8 and B7) in the LSB part of the exemplary Mixing-DAC. The pre-annotated capacitance in the schematic model of the current cells is altered. The x-axis is in % deviation of the ideally scaled value to ease the comparison between the various binary cells. The ideal value at 0% is the exactly binary scaled capacitance: the 6fF in the unary cell results in 3fF for B9, 1.5fF for B8, etc.

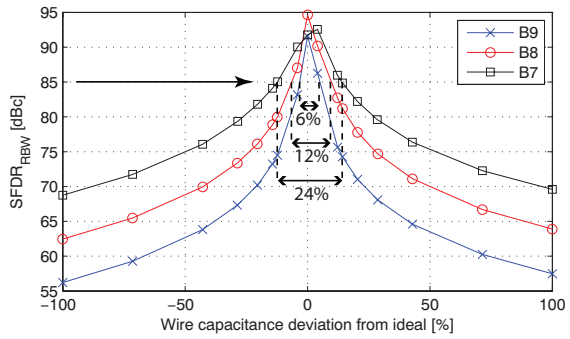


Fig. 8. SFDR dependence on the parasitic capacitance at the output cascode source node of B9, B8 and B7

Fig. 8 clearly demonstrates the low robustness of the spectral purity to the capacitance value. A change of 4% in the capacitance value in B9 results is a $SFDR_{RBW}$ degradation of 9dB to 83dBc, which is worse than the required 85dBc.

Fig. 8 also shows a relationship between the capacitance robustness and the binary cell index. The B9 cell has the lowest robustness: $\pm 3\%$ for 85dBc. The subsequent binary cells have a doubled robustness for each index decrement: B8=$\pm 6\%$, B7=$\pm 12\%$. Even though the actual robustness numbers may only be valid for the exemplary Mixing-DAC implementation, the robustness trend is valid for all CS (Mixing-)DACs. The robustness of an implementation is limited, which also limits the maximum $SFDR_{RBW}$ when the segmentation is fixed.

C. Segmentation

A novel, back-off aware segmentation trade-off is proposed in Fig. 9(a), in analogy to the segmentation trade-off figures in [10]. A larger unary MSB part improves the $SFDR_{RBW}$, but a lower output power reduces the $SFDR_{RBW}$. The segmentation trade-off of the exemplary Mixing-DAC is shown in Fig. 9(b). The proposed segmentation (6b unary, 10b binary) is design point α, where $SFDR_{RBW}$=86dBc at -16dB$_{FS}$/tone. If the back-off requirement increases to -22dB$_{FS}$/tone, the $SFDR_{RBW}$=80dBc (design point β). If the $SFDR_{RBW}$ of 86dBc value should be maintained at -22dB$_{FS}$/tone back-off, the segmentation should be changed to one more unary bit, which is design point γ. This illustrates the trade-off between $SFDR_{RBW}$, segmentation and output power back-off. Naturally, changing the segmentation has numerous other implication, e.g. on layout area or maximum signal frequency.

The simulated performance of the exemplary Mixing-DAC segmentation at -16dB$_{FS}$/tone (10dB back-off) of $SFDR_{RBW}$=86dBc is sufficient for the required 85dBc, hence the chosen segmentation is optimal.

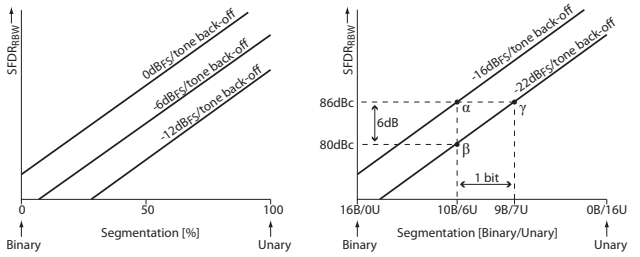


Fig. 9. Segmentation trade-off based on $SFDR_{RBW}$ and back-off, both trend (a) and exemplary Mixing-DAC (b)

IV. Conclusion

Timing errors are a main concern in high speed highly linear Mixing-DAC architectures. Simulations reveal tight constraints on the delay errors in the unary part of the segmented Mixing-DAC. For the multicarrier GSM requirement of $SFDR_{RBW}$=85dBc at 4GHz, $\sigma(delay)$ <36fs is required. The Mixing-DAC architecture with the highest linearity uses local mixing in the output stage with a single global LO driver.

For multicarrier transmitters, output power back-off is often used. With back-off, the matching of parasitic capacitances at the high-speed nodes in the binary current cells is crucial for achieving a high $SFDR_{RBW}$. The proposed segmentation trade-off shows that for every 6dB of additionally required back-off, one extra unary bit is needed.

The proposed methods lead to a Mixing-DAC architecture tailored toward the high linearity and high frequency requirements of multicarrier GSM transmitters. The simulated performance of this architecture, implemented in 65nm CMOS, is: $SFDR_{RBW}$=86dBc at f_{out}=4GHz and -16dB$_{FS}$/tone output power (10dB back-off).

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