Advances in High Precision Amplifiers - The Extra L Opposed Current Converter

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Abstract—In existing half/full-bridge high precision amplifiers output distortion is present due to the required switch blanking time. The OCC topology does not require this blanking time but has a much higher total inductor volume compared to the half-bridge. In this paper a patented new topology is introduced that has the advantages of the OCC but with a much lower total inductor volume. The basic operation and properties of the ELOCC topology are explained including an extended optimization of the total inductor volume and an average model for control design. A prototype ELOCC current amplifier has been developed. The behavior of this prototype is in good agreement with the obtained simulation results. Even though the prototype is not fully optimized the linearity compared to a full-bridge is already impressive.

Index Terms—DBI, dual buck inverter, ELOCC, high precision, OCC, opposed current converter.

I. INTRODUCTION

THE half-bridge (HB) with output filter, is a basic electronic building block used in high frequency switching power converters and amplifiers. This topology however has some inherent problems that limit the performance, efficiency and reliability. Consequently, the usability is reduced in high reliability and high precision amplifiers. This problem becomes more prone at higher operating voltages, as higher voltage switches have worse switching characteristics.

Because two stacked switches are connected across the bus voltage, a blanking time (dead time) is required between switching off a transistor and switching on the other transistor. The dead time must be sufficiently large to ensure that there is no overlap in conduction of both switches. During the dead time the parallel diode of one of the two transistors is conducting and carries the filter inductor current. This results in a current dependent switching node voltage during the dead time, which in turn introduces a zero crossing distortion and significantly increases the total harmonic distortion of the output current.

In the case of MOSFETs the parasitic body diode has poor switching characteristics, resulting in high reverse recovery losses and increased electromagnetic interference (EMI).

Another problem of the half-bridge is the sensitivity to cosmic radiation. This is mainly a problem in converters with a high bus voltage where MOSFETs are more sensitive to cosmic particle turn-on [1]. In case of a half-bridge converter in operation, for the majority of the time, one of the MOSFETs is switched on. If the opposite MOSFET is triggered by a cosmic particles, the bus voltage is shorted and both switches are typically destroyed. This sensitivity to cosmic radiation has a high impact on reliability.

There exists a topology that does not exhibit these downsides. This power converter topology is the opposed current converter (OCC) [2], [3] or dual buck inverter (DBI) [4], shown in Fig. 1 (a). The OCC or DBI topology is gaining popularity in grid connected applications [5], [6] and for non-dissipative voltage balancing in multi-level converter applications [7].

In the OCC the bidirectional half-bridge is replaced by two parallel-complementary unidirectional switching legs. Unfortunately the resulting converter has a much higher magnetic volume and therefore higher cost of implementation, with respect to it’s conventional equivalent. Methods have been
proposed to reduce the volume by coupling of inductors [8], [9] or using a split-wound inductor [10].

In this paper a patented new topology is proposed that leads to a lower total inductor volume without applying coupled inductors. The new topology is named extra L opposed current converter, or ELOCC, and is an evolution of the existing OCC. The ELOCC, shown in Fig. 1 (b), has no dead time distortion, resulting in a high linearity compared to a half/full-bridge amplifier. Moreover, the diode can be optimized with respect to MOSFET parasitic diode resulting in reduced EMI.

II. EXTRA L OPOSED CURRENT CONVERTER

The ELOCC topology is based on the existing OCC topology in which two parallel-complementary unidirectional switching legs together can provide bidirectional output current flow. In the OCC, in case the output current $i_{\text{out}}$ is positive, the positive leg and filter inductor $L_{f1}$ carries the output current. In case of negative output current, the negative leg and filter inductor $L_{f2}$ carry the output current. Therefore, both filter inductors should be capable of conducting the full output current.

As proposed in [11], in order to avoid distortion on the output, a bias current should be added, flowing from the positive leg to the negative leg to keep both legs in continuous conduction mode (CCM).

In the ELOCC an extra inductor $L_b$ is added between the two unidirectional legs. The goal of this extra inductor is to balance the current through $L_{f1}$ and $L_{f2}$ such that each filter inductor conducts only half the output current. To balance the filter inductor currents the average current through $L_b$ should be controlled such that in the ideal case

$$
\langle i_{L_b} \rangle = \begin{cases} 
\frac{1}{2}i_{\text{out}} + i_{\text{offset}} & \text{for } i_{\text{out}} \geq 0 \\
-\frac{1}{2}i_{\text{out}} + i_{\text{offset}} & \text{for } i_{\text{out}} < 0
\end{cases}
$$

(1)

which can be simplified to

$$
\langle i_{L_b} \rangle = \frac{1}{2}|i_{\text{out}}| + i_{\text{offset}}
$$

(2)

The brackets $\langle \rangle$ indicate the moving periodic average over a switching period. The term $i_{\text{offset}}$ is an additional current component flowing from the positive to the negative leg. Note that the current through $L_b$ is identical to the proposed modulated bias current in [11]. Since the current through $L_b$ is identical to the OCC bias current, inductor $L_b$ is also indicated as the bias inductor. Similar to the constant bias current in [11], the current through $L_b$ can also be set to a constant value.

The current ripple of each of the filter inductors is assumed to be fully absorbed by the filter capacitor and $\langle i_{C_f} \rangle$ is assumed zero for subsequent analysis.

A. Converter basics

The ELOCC switching cell contains two switches. These two switches give a total of four output states as given in Table I with the corresponding bias and average voltage. When a switch is off the complementary diode is assumed to be conducting. The average voltage $u_{\text{avg}}$ is defined as the average voltage of both switching nodes $u_{\text{sn1}}$ and $u_{\text{sn2}}$. The bias voltage $u_{\text{bias}}$ is defined as the voltage between $u_{\text{sn1}}$ and $u_{\text{sn2}}$.

A closer look at Table I reveals that in states $s_0$ and $s_3$ the bias voltage $u_{\text{bias}}$ can be set to $U_{\text{DC}}$ or $-U_{\text{DC}}$, while the average voltage $u_{\text{avg}}$ remains constant. In the states $s_1$ and $s_2$ the average voltage $u_{\text{avg}}$ can be set to $0V$ or $U_{\text{DC}}$, while $u_{\text{bias}}$ remains at $0V$. This means that $u_{\text{avg}}$ and $u_{\text{bias}}$ are decoupled. Therefore a similar decomposition as done in [11] can be applied for the ELOCC as

$$
\begin{align*}
\text{state} & \quad \text{switch} S_2 \quad \text{switch} S_1 \quad u_{\text{avg}} \quad u_{\text{bias}} \\
0 & \quad \text{off} \quad \text{off} \quad \frac{1}{2}U_{\text{DC}} \quad -U_{\text{DC}} \\
1 & \quad \text{off} \quad \text{on} \quad 0 \quad 0 \\
2 & \quad \text{on} \quad \text{off} \quad 0 \quad 0 \\
3 & \quad \text{on} \quad \text{on} \quad \frac{1}{2}U_{\text{DC}} \quad U_{\text{DC}}
\end{align*}
$$

In steady state the output voltage $u_{\text{out}}$ is equal to the average voltage $u_{\text{avg}}$, when neglecting losses.

Because $L_b$ is actually in parallel to the series connection of $L_{f1}$ and $L_{f2}$, a portion of $i_{\text{bias}}$ will also flow through the filter inductors, based on the impedance of the bias and filter inductors. Ideally the inductors are chosen such that the portion of the bias current through the filter inductors ($\frac{1}{2}(i_{L_{f1}} - i_{L_{f2}})$) is very small and can be neglected.

The filter inductors in the ELOCC are designed to allow a certain peak current ripple. When assuming the output capacitor is large and the converter is in steady state, the peak current ripple amplitude is found to be

$$
\Delta i_{L_{fk}} = \frac{U_{\text{DC}}}{8L_{fk}} T_{sw}
$$

(5)

where $k \in \{1, 2\}$. The peak current ripple is typically chosen between 10% and 40% of $i_{\text{out}}$. With the filter inductors fixed the filter capacitor $C_f$ is determined. The output filter cut-off frequency $f_o$ is defined by

$$
f_o = \frac{1}{\pi \sqrt{2LfC_f}}
$$

(6)

where $L_f = L_{f1} = L_{f2}$. The cut-off frequency of the output filter is typically chosen at $1/\sqrt{2}$ of the switching frequency.

To have an output filter performance equivalent to the conventional half-bridge, the filter capacitor can be kept identical to the half-bridge filter capacitor and the filter inductors should be chosen such that

$$
L_f = 2L_{\text{HB}}
$$

(7)
where $L_{HB}$ is the corresponding half-bridge filter inductor.

The choice for the bias inductor $L_b$ is described in section III. For now the inductance value of $L_b$ is considered much smaller than $L_f$.

B. Bias inductor current

The relation between the periodic average switching node voltage $\langle v_{snk} \rangle$ and switch duty cycle $\delta_{sn}$ of a unidirectional switching leg becomes linear when the switch resistances are matched and the leg is operated in continuous conduction mode, as shown in [12]. In the ELOCC switching cell, where two inductors are connected to a single leg, continuous conduction mode is not obvious. Therefore continuous conduction mode is defined for the total current out of leg 1, $i_1$, and the total current into leg 2, $i_2$. In order to operate each of the legs in continuous conduction mode the currents $i_1$ and $i_2$ must be positive. Resulting in the following bounds for the inductor currents

\[
\begin{align*}
  i_{L_f1} + i_{L_b} &> 0 & \text{(8a)} \\
  -i_{L_f2} + i_{L_b} &> 0 & \text{(8b)}
\end{align*}
\]

Due to the current ripple $\Delta i_{Lfk}$ in the filter inductors and $\Delta i_{Lb}$ in the bias inductor, the following requirements apply for CCM

\[
\begin{align*}
  \frac{1}{2}i_{out} - \Delta i_{Lf1} + \frac{1}{2}|i_{out}| + i_{offset} - \Delta i_{Lb} &> 0 & \text{(9a)} \\
  -\frac{1}{2}i_{out} - \Delta i_{Lf2} + \frac{1}{2}|i_{out}| + i_{offset} - \Delta i_{Lb} &> 0 & \text{(9b)}
\end{align*}
\]

To ensure that the converter is operated in CCM, $i_{offset}$ is chosen such that

\[i_{offset} \geq \Delta i_{Lf1} + \Delta i_{Lb} \quad \text{(10)}\]

Typically $i_{offset}$ is chosen larger than $\Delta i_{Lf1} + \Delta i_{Lb}$ to guarantee CCM during transients.

C. Switching waveforms

The steady state switching waveforms for positive output current of the ELOCC power stage are shown in Fig. 2. The MOSFETs and diodes are considered ideal, the output capacitor is assumed large and the bias inductor $L_b$ is assumed to have a series resistance.

1) Time interval $t_0$: The system is in output state $s_2$. The current in the filter inductors $L_{f1}$ and $L_{f2}$ decays with a rate of $\frac{u_{out}}{R_{\text{pk}}}$ and the current in the bias inductor $L_b$ decays exponentially due to the parasitic resistance of the inductor.

2) Time interval $t_1$: During time interval $t_1$ the system is in output state $s_3$. The current in the filter inductor $L_{f1}$ increases with a rate of $\frac{u_{PFC}-u_{out}}{L_{f1}}$, and the current in $L_{f2}$ decays with a rate of $\frac{u_{out}}{L_{f2}}$. The current in the bias inductor $L_b$ increases with a rate of $\frac{u_{PFC}}{L_b}$. In case a negative voltage across the bias inductor $L_b$ is required the system is in output state $s_0$. Then the current in filter inductor $L_{f1}$ decays with a rate of $\frac{u_{out}}{L_{f1}}$, and the current in $L_{f2}$ increases with a rate of $\frac{u_{PFC}-u_{out}}{L_{f2}}$. The current in the bias inductor $L_b$ then decreases with a rate of $\frac{u_{PFC}}{L_b}$.

III. Inductor volume optimization

In this section the total inductor volume for an ELOCC power stage is compared to a conventional HB. The inductor volume is expressed as function of $L_b$ and $R_{\text{Lb}}$. The estimation of the inductor volume is done using the area-product method [13].

To simplify calculations a few assumptions are made. The output current $i_{out}$ is assumed to be sinusoidal and in phase with the output voltage. The current through the filter inductors $i_{L_{f1}}$ and $i_{L_{f2}}$ is assumed to be sinusoidal with a triangular current ripple and the frequency of the output current is assumed much lower than the switching frequency. The bias current is set to a constant value and it is assumed that there is no ripple in the output current for both the ELOCC and HB case.

For a proper comparison between the ELOCC and HB the ELOCC filter inductors are chosen according to (7).

A. Area-product

The area-product $A_P$ is the product of the winding area $W_A$ and effective core area $A_C$, both indicated in Fig. 3. The
volume of the inductor is then given by $V_L = K_{vol} A_P^{0.75}$, where $K_{vol}$ is the geometrical constant of the core shape. Since the total inductor volume of the ELOCC power stage, relative to the inductor volume of the half-bridge is desired, the geometrical core constant $K_{vol}$ is assumed equal for all inductors. As $K_{vol}$ is assumed equal for the considered inductors it can be omitted. This gives

$$V_L \propto A_P^{0.75}$$

which is sufficient for determining the relative inductor volume.

When it is assumed that all energy is stored in the core material of the filter inductor, so there is no leakage flux, the area-product of the HB filter inductor is given by

$$A_{PHB} = \frac{L_{HB}}{B J K_u} \left| i_{LHB} \right| I_{LHB}$$

(12)

with $B$ being the peak magnetic flux density, $J$ the RMS current density and $K_u$ the window utilization factor. The currents $i_{LHB}$ and $I_{LHB}$ are the respective filter inductor peak and RMS currents. The currents are given by

$$|i_{LHB}| = |i_{out}| + \Delta i_{LHB}$$

(13a)

$$I_{LHB} = \sqrt{\frac{1}{2} i^2_{out} + \frac{1}{3} \Delta i^2_{LHB}}$$

(13b)

where the peak inductor ripple current $\Delta i_{LHB}$ can be expressed in terms of the peak output current $i_{out}$ as

$$\Delta i_{LHB} = 2 k_o \hat{i}_{out}$$

(14)

where $2 k_o$ is used because the ripple coefficient $k_r$ is defined for the ELOCC filter inductors (see (18a)).

Substituting (7), (13) and (14) into (12) gives

$$A_{PHB} = \frac{L_f}{2 B J K_u} \hat{i}_{out}^2 \left(1 + 2 k_r \right) \sqrt{\frac{1}{2} + \frac{1}{3} (2 k_o)^2}$$

(15)

In the ELOCC switching cell the total volume is determined by the volume of the three inductors together. Therefore the area-product must be calculated for each of the inductors separately. The total relative inductor volume of the ELOCC switching cell is

$$\frac{V_{LELOCC}}{V_{LHB}} = \frac{A_{PHB}^{0.75} + A_{PLF1}^{0.75} + A_{PLF2}^{0.75}}{A_{PHB}^{0.75}}$$

(16)

where due to symmetry the area-product $A_{PLF1} = A_{PLF2}$. The peak magnetic flux density $B$, current density $J$ and winding utilization factor $K_u$ are set equal for all considered inductors.
depends on \(m_{\text{bias}}\) only, where \(m_{\text{bias}}\) is the bias modulation index, defined such that
\[
\langle u_{\text{bias}} \rangle = m_{\text{bias}} U_{\text{DC}} \quad \text{for} \quad -1 < m_{\text{bias}} < 1 \tag{21}\]
The times \(t_0, t_2\) and \(t_4\) vary based on the output modulation index \(m_{\text{out}}\) resulting in a change in peak and RMS current. The output modulation index is defined as
\[
\langle u_{\text{avg}} \rangle = \frac{1}{2} m_{\text{out}} U_{\text{DC}} \\
\text{for} \quad -(1 - |m_{\text{bias}}|) \leq m_{\text{out}} \leq (1 - |m_{\text{bias}}|) \tag{22}\]
To simplify calculations an auxiliary modulation index is introduced for the output, being defined as
\[
m'_{\text{out}} = \frac{m_{\text{out}}} {1 - |m_{\text{bias}}|} \tag{23}\]
which spans the usable range of the output modulation index. Depending on \(m'_{\text{out}}\) the peak to valley current ripple in the bias inductor varies between \(2\Delta i_{L_b}\) and \(4\Delta i_{L_b}\). The resulting peak current in \(L_b\) is described by
\[
\hat{i}_{L_b} = [Q_{L_b} (\frac{1}{2} + k_o) + \Delta i_{L_b} (1 + |m'_{\text{out}}|)] i_{\text{out}} \tag{24}\]
where \(\Delta i_{L_b}\) can be expressed in terms of \(i_{\text{out}}\) as
\[
\Delta i_{L_b} = \frac{2m_{\text{bias}}|k_r|}{k_{Lb}} i_{\text{out}} \tag{25}\]
The factor \(k_{Lb}\) is the value of \(L_b\) relative to \(L_f\) as
\[
L_b = k_{Lb} L_f \tag{26}\]
The RMS current in the bias inductor is described by
\[
I_{L_b} = \hat{i}_{\text{out}} \sqrt{Q_{L_b}^2 (\frac{1}{2} + k_o)^2 + \frac{4}{3} \left(\frac{m_{\text{bias}} k_r}{k_{Lb}}\right)^2} M^2 \tag{27}\]
with \(M\) a function of \(m_{\text{out}}\) and \(m_{\text{bias}}\) given by
\[
M^2 = 1 + m'_{\text{out}}^2 (2|m_{\text{bias}}| + 2|m_{\text{out}}| + 1) \tag{28}\]
The area-product of the bias inductor, using (24), (25) and (27), is then given by
\[
A_{P_{Lb}} = \frac{L_f k_{Lb}^2}{BJK_o} \times \\
\left[Q_{L_b} (\frac{1}{2} + k_o) + \frac{2|m_{\text{bias}}| k_r}{k_{Lb}} (1 + |m'_{\text{out}}|)\right] \times \\
\sqrt{Q_{L_b}^2 (\frac{1}{2} + k_o)^2 + \frac{4}{3} \left(\frac{m_{\text{bias}} k_r}{k_{Lb}}\right)^2} M^2 \tag{29}\]

B. Current distribution

The distribution of the bias current depends on the impedance relation between the series connected filter inductors \((L_{f1} & L_{f2})\) and the bias inductor \(L_b\) as shown in Fig. 5.

For the DC part of the bias current the distribution is only dependent on the parasitic resistances of filter inductors and bias inductor. The distribution of the AC components does however also depend on the inductance of the components. The cut-off frequency of a typical inductor for \(L_b\) is well within the output frequency range, therefore the AC current distribution must also be taken into account.

As the AC and DC bias current distribution are independent, either can cause high peak and RMS currents in each of the inductors. Therefore the current distribution factors \(Q_{L_f}\) and \(Q_{L_b}\) are defined as follows
\[
Q_{L_f} = \max \left(\frac{R_{L_b}}{R_{L_f} + 2R_{L_b}}, \frac{L_b + 2L_f}{L_b + 2L_f}\right) \tag{30a}\]
\[
Q_{L_b} = \max \left(\frac{2R_L}{R_{L_f} + 2R_{L_b}}, \frac{2L_f}{L_b + 2L_f}\right) \tag{30b}\]
which is the maximum of both AC and DC current distribution between the filter inductors and the bias inductor.

C. Inductor volume

Using the current distribution factors from (30) the relative inductor volume of the ELOCC switching cell is determined. Typical values are chosen for the ripple and offset current coefficients and for the modulation indexes. The ripple current coefficient \(k_r = 0.1\), that is 10% of \(i_{\text{out}}\) and the offset current coefficient \(k_o = 0.2\). An average bias voltage of 5% of \(U_{\text{DC}}\) is reasonable for a practical system, therefore \(m_{\text{bias}} = 0.05\). The output modulation index varies sinusoidal with a maximum peak value of 0.95, for calculation a constant value of \(m_{\text{out}} = 0.95\) is used. This is slightly pessimistic for the RMS current but the difference is negligible for low values of \(m_{\text{bias}}\).

The total inductor volume of the ELOCC switching cell, relative to a half-bridge leg, is shown in Fig. 6.
Depending on the choice of \( L_b \) the total volume varies between a volume close to a HB leg to a volume of over a factor 4 larger. There is an optimal relation between the inductance and resistance of \( L_b \). This optimum is located in the valley of the graph in Fig. 6 for which holds

\[
\frac{L_b}{L_f} = \frac{R_{lb}}{R_{lf}}
\]  

(31)

or similar

\[
\frac{L_b}{R_{lb}} = \frac{L_f}{R_{lf}}
\]  

(32)

Therefore the time constant of the bias inductor \( L_b \) should be chosen equal to the time constant of the filter inductors \( L_f \).

Fig. 7 depicts the total inductor volume from Fig. 6 for (32).

When choosing \( L_b \) & \( L_{f,k} \) according to (32) with \( L_b/L_f \gg 1 \) the volume is obtained for a standard OCC switching cell with uncoupled inductors. When choosing the bias inductor equal to the filter inductors \( (L_b/L_f = 1) \) a volume reduction of already 35% is obtained with respect to a standard OCC. The lowest total inductor volume is obtained when at \( L_b/L_f = 0.016 \), with a total volume of 1.43 with respect to a half-bridge. For a smaller bias inductance the total inductor volume increases, this is due to the increasing ripple in the bias inductor resulting in a higher peak and RMS current. For larger values of \( m_{bias} \) the ripple also increases resulting in a higher optimal value for the bias inductor.

IV. AVERAGE MODEL

A high precision power amplifier generally requires control to generate output signals that have sufficient accuracy. For control design it is preferred to have a representative model of the system to ease design and simulations. In this section the average model of the ELOCC switching cell is derived.

As described in subsection II-A an ELOCC switching cell can be decomposed into two decoupled systems. The output transfer function is described by

\[
H_{out}(s) = \frac{i_{out}(s)}{u_{out}(s)}
\]  

(33)

and the bias transfer function is described by

\[
H_{bias}(s) = \frac{i_{bias}(s)}{u_{bias}(s)}
\]  

(34)

Fig. 8. ELOCC output system overview.

In both systems the target is to have a controlled current.

In case the switching frequency \( T_{sw}^{-1} \) of the legs is much higher than the cut-off frequency of the output filter \( f_o \), which should be the case in the ELOCC switching cell, each leg can be represented as an average voltage source \( \bar{u}_{snk} \). The average voltage is given by

\[
\bar{u}_{sn1} = U_{DC} \delta_{S1}
\]  

(35a)

\[
\bar{u}_{sn2} = U_{DC} (1 - \delta_{S2})
\]  

(35b)

when the switches and diodes are considered ideal and each of the legs is operating in CCM. Using the decoupling from (3) the linear bias transfer function is obtained as

\[
H_{bias}(s) = \frac{1}{2 (sL_f + R_{lf})} + \frac{1}{sL_b + R_{lb}}
\]  

(36)

When the bias inductor is chosen according to (32) and \( L_b/L_f \ll 1 \), the majority of the bias current flows through \( L_b \), therefore the left term in (36) can be neglected and \( H_{bias} \) simplifies to

\[
H_{bias}(s) = \frac{1}{sL_b + R_{lb}}
\]  

(37)

The output transfer function is mainly dependent on the load. The output voltage is decoupled from the bias voltage/current. Therefore the average model of the output system, in case of a full-bridge equivalent setup, simplifies to the circuit shown in Fig. 8.

The resulting output voltage is defined as

\[
u_{out}^* = u_{out,p}^* - u_{out,n}^*
\]  

(38)

where \( u_{out,p}^* \) and \( u_{out,n}^* \) are the output voltage set-points of the respective positive and negative switching cell. The transfer function (33) is found to be

\[
H_{out}(s) = \frac{s L_f + R_l}{\frac{1}{2} s^3 L_f L_1 C_f + \frac{1}{2} s^2 L_f R_l C_f + s \left( \frac{1}{2} L_f + L_1 \right) + R_l} \times \frac{1}{s L_1 + R_l}
\]  

(39)

which is identical to the transfer function of a full-bridge converter with \( L_{HIB} = \frac{1}{2} L_f \). Consequently the same output current controller can be used as in a full-bridge converter.

For frequencies well below the cut-off frequency \( f_o \ll f_o \) the output filter transfer function is approximately 1. Then the output transfer function simplifies to

\[
H_{out}(s) = \frac{1}{s L_1 + R_l}
\]  

(40)
TABLE II

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Value</th>
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</thead>
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<td>$i_{\text{out}}$</td>
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<td>$U_{\text{DC}}$</td>
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<tr>
<td>$f_{\text{sw}}$</td>
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<td>$L_1$</td>
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<td>$R_1$</td>
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<tr>
<td>Open loop bandwidth</td>
<td>&gt; 5kHz</td>
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V. EXPERIMENTAL PROTOTYPE

The performance and functionality of the ELOCC topology power stage is verified with a functional prototype. A full-bridge equivalent prototype is designed according to the specifications of an existing high precision full-bridge current amplifier. The application of this current amplifier is a high precision motor drive. The requirements for the prototype are given in Table II.

A. Power stage design

The prototype power stage is built with IXYS IXFH26N60P 26A 600V MOSFETs and Vishay VS-APH3006-F3 30A 600V diodes. The gate driver circuitry is completely re-used from an existing full-bridge current amplifier.

The filter inductors $L_f$ and $L_b$ are toroidal inductors, with 220μH inductance and 50mΩ DC resistance. The peak current ripple in the filter inductor $\Delta i_{L_f}$ is 1.09A.

The bias inductor $L_b$ is custom designed according to (32). In case we assume all bias current flows through the bias inductor, the peak current $i_{\text{bias}}$ is

$$i_{\text{bias}} = i_{\text{bias}} + \Delta i_{L_b} = \frac{1}{2} |i_{\text{out}}| + i_{\text{offset}} + \Delta i_{L_b}$$

where $i_{\text{out}} = 12.5A$, $i_{\text{offset}} \approx 3A$ and the target peak bias inductor ripple current is set at 0.5A. Therefore the inductor should be rated for $\geq 9.75A$ and have $\geq 30\mu H$ inductance. The bias inductor is constructed around a smaller toroidal core than the filter inductors. The constructed inductor has 33μH inductance and 8mΩ DC resistance. Fig. 9 shows the bias and filter inductor of the prototype. The obtained corrected relative inductor volume is approximately between 1.4 and 1.65 with respect to a HB. The expected value of 1.69 from Fig. 7 is higher but the average bias voltage in the prototype is lower than the 5% of $U_{\text{DC}}$ used in Fig. 7.

B. Control

In the prototype multiple controllers are implemented to control the ELOCC power stage. An overview of the control diagram in the prototype is shown in Fig. 10. Since the complete control scheme is implemented in an FPGA only discrete-time controllers are used.

The output current set-point $i_{\text{out}}$ is generated internally by the FPGA. A 32 bit sine-wave lookup table is implemented to create the set-point for the output current. The samples are addressed synchronous to the control frequency to have an optimal resolution. The frequencies that can be generated are multiples of 10Hz.

The performance and functionality of the ELOCC topology is verified with a functional prototype. A full-bridge equivalent prototype is designed according to the specifications of an existing high precision full-bridge current amplifier. The application of this current amplifier is a high precision motor drive. The requirements for the prototype are given in Table II.

A. Power stage design

The prototype power stage is built with IXYS IXFH26N60P 26A 600V MOSFETs and Vishay VS-APH3006-F3 30A 600V diodes. The gate driver circuitry is completely re-used from an existing full-bridge current amplifier.

The filter inductors $L_f$ and $L_b$ are toroidal inductors, with 220μH inductance and 50mΩ DC resistance. The peak current ripple in the filter inductor $\Delta i_{L_f}$ is 1.09A.

The bias inductor $L_b$ is custom designed according to (32). In case we assume all bias current flows through the bias inductor, the peak current $i_{\text{bias}}$ is

$$i_{\text{bias}} = i_{\text{bias}} + \Delta i_{L_b} = \frac{1}{2} |i_{\text{out}}| + i_{\text{offset}} + \Delta i_{L_b}$$

where $i_{\text{out}} = 12.5A$, $i_{\text{offset}} \approx 3A$ and the target peak bias inductor ripple current is set at 0.5A. Therefore the inductor should be rated for $\geq 9.75A$ and have $\geq 30\mu H$ inductance. The bias inductor is constructed around a smaller toroidal core than the filter inductors. The constructed inductor has 33μH inductance and 8mΩ DC resistance. Fig. 9 shows the bias and filter inductor of the prototype. The obtained corrected relative inductor volume is approximately between 1.4 and 1.65 with respect to a HB. The expected value of 1.69 from Fig. 7 is higher but the average bias voltage in the prototype is lower than the 5% of $U_{\text{DC}}$ used in Fig. 7.

The output current is controlled by $C_{\text{out}}$ based on the set-point $i_{\text{out}}$ received on the input. For the output controller a 2nd order continuous time controller is hand tuned. This continuous time controller is converted to a discrete time controller using the zero-order-hold transformation in MATLAB. A symmetric triangular carrier is used in the PWM modulator, therefore the output is updated twice per PWM period $T_{\text{sw}}$.

Based on the measured output current a set-point $i_{\text{bias}}^*$ is generated for the bias current in each of the legs. The set-point generator can be set to either constant or modulated bias current with a configurable offset current $i_{\text{offset}}$. The set-point for both bias current controllers is identical.

The bias current in each of the switching cells is controlled by a bias controller $C_{\text{bias}}$ based on the set-point received from the bias set-point generator. A 1st order lag-leading controller has sufficient performance for the bias controller, therefore a 1st order hand tuned controller is used. The pole of the controller is placed at 0.01Hz and the zero is placed at 10kHz. The gain is set to $10^{5}$. The continuous time controller $C_{\text{bias}}$ is converted to a discrete time controller using the zero-order-hold transformation in MATLAB.

C. Simulation results

The amplifier prototype is simulated using non-ideal components. In the simulation a 12.5A pk sinusoidal set-point is used with a frequency of 200Hz and an offset current of 3A. An overview of the inductor currents of the positive switching
Fig. 11. Simulated prototype waveforms with an output current set-point of 200Hz 12.5A pk.

Fig. 12. Simulated prototype switching waveforms, zoomed in on a single period with \( i_{\text{out}} = 12.5\text{A} \).

cell and output current is plotted in Fig. 11. A detailed image of the switching waveforms of the positive switching cell at the peak output current, is shown in Fig. 12.

As visible in Fig. 11 the current in the filter inductors is not identical. This is due to the fact that the inductance and resistance of \( L_b \) are not infinitesimal. With the selected bias and filter inductors in the prototype, the bias current through the filter inductors is about 8% of the current through \( L_b \).

D. Measurements

Measurements are performed on the prototype to verify the functionality and performance of the ELOCC power topology. The measurement set-up is shown in Fig. 13. The extra inductors can be spotted between the filter inductors.

The switching node voltages and filter inductor currents are shown in Fig. 14 (a). These measurements are taken with a 5A\text{DC} output current. There is a small overlap visible in the switching node voltage where both switches are on and thus a positive voltage is applied across the bias inductor. This is more clear when zooming in on the edges of the switching node voltage in Fig. 14 (b). The bias inductor current and output current are plotted in Fig. 15.

The low frequency behavior is shown in Fig. 16 where a 200Hz sinusoidal output current is generated with a peak value of 12.5A. The conditions in this measurements are equal to the conditions used in the simulation from Fig. 11. Comparing the simulation results in Fig. 11 to the measurement in Fig. 16 shows that the observed behaviour is in very good agreement.

E. Output linearity

The linearity of the converter is tested by measuring the distortion in the output current \( i_{\text{out}} \) with a 12.5A 160Hz sinusoidal output current set-point \( i_{\text{set}}^{\text{out}} \). The sinusoidal set-point is generated internally in the FPGA with a 32 bit lookup table. The output current is measured externally with a flux-gate current sensor. This sensor has a verified spurious free dynamic range of more than 90dB and a bandwidth well beyond the open loop bandwidth required for this prototype. The SR785 Dynamic Signal Analyser is used to analyze the harmonic content of the output current.

Measuring the distortion in an open loop configuration shows the distortion caused by the limited PWM resolution of 9 bit. Therefore all linearity tests are performed in closed loop configuration. The resulting spectrum of the output current is shown in Fig. 17 where a marker is placed on the highest harmonic. The amplitude of the 3\text{rd} harmonic is \(-76\text{dBc}\) (dB with respect to the first harmonic), the amplitude of the 5\text{th} harmonic is \(-89\text{dBc}\) and the amplitude of the 7\text{th} harmonic is \(-87\text{dBc}\). All other harmonics have an amplitude of \(-90\text{dBc}\) or less.
Fig. 14. Waveforms at 5A\(_{\text{DC}}\) output current; (a) overview and (b) zoomed in on \(u_{\text{sn1p}}\) rising edge. Voltage scaling at [200V/div], current scaling at [1A/div].

Fig. 15. Waveforms at 5A\(_{\text{DC}}\) output current. Voltage scaling at [200V/div], current scaling at [2A/div].

Fig. 16. Waveforms at 12.5A\(_{\text{pk}}\) 200Hz output current, current scaling is [5A/div].

Fig. 17. Measured spectrum of \(i_{\text{out}}\) with an output current of 12.5A\(_{\text{pk}}\) 160Hz.

For comparison the spurious free dynamic range is measured of a similar amplifier with a conventional full-bridge output stage. This amplifier is highly similar to the prototype, using the same components in the end-stage. Also the same closed loop current controller (\(C_{\text{out}}\)) and PWM modulator are used as in the prototype. Measuring the distortion in the output current under the same conditions, gives a spurious free dynamic range of 53dBc. This is a difference of 23dB.

Experiments show that the remaining amplitude of the harmonics in the output current of the ELOCC prototype, is not caused by a ripple on the bus voltage \(U_{\text{DC}}\). Improving the bus decoupling and reducing the 320Hz ripple present on the bus voltage does not yield to a lower distortion in the output current.

VI. CONCLUSION

In this paper a patented new high precision amplifier topology is introduced. The advantage of the ELOCC topology compared to an equivalent half/full-bridge circuit is that it has a much lower distortion. Also the parallel diode of the switches
is never conducting resulting in more design flexibility, as the switch and diode can be optimized separately. Moreover the total inductor volume of an ELOCC circuit is much lower than the volume of an equivalent OCC circuit. A theoretical volume reduction of up to 72% can be obtained.

A prototype is developed of an ELOCC full-bridge equivalent power stage. The developed prototype is fully functional and capable of supplying an output current of 12.5A_pik with an output voltage of 300V. The simulated behavior of the converter is in very good agreement with measured behavior of the prototype.

Without special optimization for low distortion, the spurious free dynamic range in the output current is already 53dB. A comparable fullbridge amplifier has a closed loop spurious free dynamic range of 55dB. The distortion in the ELOCC prototype is most probably caused by a mismatch in voltage drop across the different switches. A lower distortion might be obtained when using MOSFETs with a lower R_{DS(on)} or by using IGBTs. In the prototype the switches have a rather high resistance with a voltage drop of up to 10V.

**REFERENCES**


