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A 16-43 GHz Low-noise Amplifier with 2.5-4.0 dB Noise Figure

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Abstract—This paper presents an ultra-broadband low-noise amplifier (LNA) operating from 16 to 43 GHz in a 0.25 µm SiGe:C BiCMOS technology. Across this band, the LNA achieves simultaneous low-noise performance (2.5-4.0 dB) and power matching (S11 < -10 dB) using dual-LC tank matching. The measured minimal noise figure is 2.5 dB at 26 GHz with an average value of 3.25 (±0.75) dB from 16 to 44 GHz. The best average value of 3.25 (±0.75) dB from 16 to 44 GHz. The best matching (<1-dB compression point and input IP3 are better than –8.5 dBm and 43 GHz (90% fractional bandwidth). The measured input 1-dB compression point and input IP3 are better than –8.5 dBm and 1.8 dBm over the 16-43 GHz band, respectively, for a total power consumption of 24 mW.

Keywords—LNA; ultra-broadband; dual-LC tank; SiGe

I. INTRODUCTION

Broadband systems at millimeter-wave (mm-wave) frequencies have recently received a great deal of interest since their bandwidth is sufficient for high-data rate communication, such as the fifth generation (5G) wireless communication system [1] and typical K band (20-40 GHz) applications [2, 3]. With the development of silicon based technology, a high performance mm-wave front-end with complex system integration is feasible in SiGe BiCMOS technology [3]. However, it is still challenging for a mm-wave front-end system to cover the entire bandwidth from 20 to 40 GHz to support K band and 5G communication systems.

In such a broadband system, the low-noise amplifier (LNA) design is one of the biggest challenges, expected to provide significant low-noise (i.e. noise figure (NF) around 3 dB), sufficient power matching (S11 < -10 dB), and small gain variation (3-dB gain bandwidth, BW3dB > 20 GHz). Various wide band designs are proposed for broadband systems. For instance, the common-base (CB) structure could provide broadband input matching, but its noise performance is poorer than the common-emitter (CE) structure [4]. Shunt resistive feedback with inductive series-peaking is employed in [5] to provide large gain bandwidth, but both power matching and noise performance are limited. CE structure with inductive degeneration and inductor matching is used in [6] to achieve low-noise performance, however, it is limited by both power matching and gain bandwidth (26-31 GHz). An LC-ladder is used in [7] to achieve a wideband power matching (3-10 GHz) but the operating frequency is below 10 GHz. In this paper, an ultra-broadband LNA with 2.5-3.5 dB NF and S11 < -11 dB over the complete K band is presented. To achieve both broadband power matching and low-noise performance, a dual-LC tank matching method is proposed and employed in a cascode structure.

This paper is organized as follows. In section II, the proposed method of dual-LC tank matching is analyzed. The implemented LNA is presented in the Section III. The measurement results are provided in section IV. Conclusions are presented in Section V.

II. LNA CIRCUIT DESIGN

A. Dual-LC Tank Matching Network

The equivalent small-signal model of the dual-LC tank matching network is shown in Fig. 1, which consists of a shunt tank (L_s, C_s), a series (L_c, C_c) tank and an equivalent resistance (R_EQ). Both shunt and series tanks are resonant at the same frequency (ω_c). The input impedance, Z_IN, can be expressed as a function of frequency (ω) and R_EQ in (1).

\[ Z_{IN} = \frac{1}{j\omega L_2 \left(1 - \frac{\omega_c^2}{\omega^2}\right) + \frac{1}{R_{EQ}}} \]  

(1)

The Z_IN curves are plotted on the Smith chart in Fig. 1 with R_EQ from 30 to 70 Ω. The blue dashed circle indicates the region for return loss (S21) better than -10 dB, where Z_IN is defined in (2).

\[ S11 = 10\log|Z_{IN}|^2 = 10\log \left|\frac{Z_{IN} - Z_0}{Z_{IN} + Z_0}\right|^2 \]  

(2)

As shown in Fig. 1, the S11 bandwidth is extended when R_EQ is decreased. The bandwidth of S11 < -10 dB can be derived by solving ω from (1) under the condition that the imaginary part of Z_IN(ω) is zero. Equation (1) has three roots: ω_L at the central frequency, ω_c at a lower frequency and ω_H at a higher frequency with the relation ω_H/ω_L = ω_c^2. The real parts of Z_IN at these three frequencies are:

\[ R_{IN}(\omega) = \begin{cases} R_{EQ}, & \omega = \omega_L \\ \frac{L_1 L_2 \omega_c^2}{R_{EQ}}, & \omega = \omega_c \\ \omega = \omega_H \end{cases} \]  

(3)
Therefore, the $S_{11}$ is completely determined by $R_{EQ}(\omega)$ at these frequencies. Note that (3) also indicates $R_{IN}(\omega_0) = R_{IN}(\omega_0^*)$ (designated as $R_0$), which means $S_{11}$ has the same value at these frequencies. The boundary conditions of $R_{EQ}$ and $R_0$ is obtained by solving (2), which leads to $26 < R_{EQ} < R_1 < 96$. As a result, the $S_{11}$ bandwidth is given by (4).

$$\omega_H - \omega_L = \frac{R_1 R_{EQ} - R_2^2}{L_2}$$ (4)

### B. Dual-LC tank as Noise Matching

The Dual-LC tank can also be applied for broadband noise matching. The output impedance of the matching network ($Z_S$) is shown in Fig. 2, where $R_0$ is the source resistance. The minimal noise figure ($NF_{\text{MIN}}$) of a transistor is achieved under the noise matching condition of $Z_S = Z_{\text{OPT}}$ [6], where $Z_{\text{OPT}}$ is the optimal noise impedance of the transistor. If $Z_S = Z_{\text{OPT}} = Z_{IN}^*$, then the transistor achieves simultaneous noise and power matching [8]. For an inductively degenerated CE stage (Fig. 2), $Z_{\text{OPT}}$ and $Z_{IN}$ are expressed in (5) and (6), respectively.

$$Z_{\text{OPT}} \approx \frac{1}{\omega(C_{BE} + C_{BC})} \left[ \frac{g_m}{2}(R_E + R_B) + j \right]$$ (5)

$$Z_{IN} \approx \frac{g_m L_E}{C_{BE}} + \frac{1}{j\omega(C_{BE} + C_{BC})}$$ (6)

where $C_{BE}$ and $C_{BC}$ are the base-emitter and base-collector capacitance; $R_E$ and $R_B$ are emitter and base resistance; $g_m$ is the transconductance and $L_2$ is the degeneration inductance. $Z_S$, $Z_{IN}$, $Z_{IN}^*$ and $Z_{\text{OPT}}$ are plotted in the Smith chart from 10 to 50 GHz in Fig. 2. It can be shown that the rotation direction of $Z_{IN}$ in the Smith chart is similar to a series RC circuit, therefore $Z_{IN}$ and $Z_S$ constitute the dual-LC tank. By applying the dual-LC tank matching method, $Z_S$ and $Z_{IN}$ can be matched ($S_{11} < -10\ dB$ at $\omega_L, \omega_S$ and $\omega_{HI}$), which means $Z_S$ curve follows $Z_{IN}$ curve between $\omega_L$ and $\omega_{HI}$.

III. CIRCUIT IMPLEMENTATION

The schematic of the proposed LNA is shown in Fig. 3. The cascode structure ($Q_1$ and $Q_2$) is chosen to alleviate the Miller effect and improve the reverse isolation. The method of dual-LC tank matching network is implemented through $L_1, C_1, C_2$ and transistor $Q_1$. The pad capacitance $C_{PAD}$, the shunt inductor $L_1$ and the shunt capacitor $C_1$ form the first tank. The series inductor $L_2$, together with the input capacitance of transistor $Q_1$ ($C_{BE}$) and $L_1$ form the second tank. $L_3$ is a degeneration inductor to generate the required real part of the input impedance for power matching. The transistor $Q_1$ is biased at 3.5 mA/µm² current density for optimal noise performance.
The size of $Q_1$ and value of $L_3$ are selected to generate the required input impedance ($R_{IN} = 35 \Omega$) and noise matching ($R_{OPT} = 45 \Omega$) based on the dual-LC tank matching method at 30 GHz. The transistor $Q_2$ provides extra power gain and isolation and its size is selected to improve the noise matching between two transistors [6]. The inductor $L_4$ and transmission line $T_1$ provide a broadband inductive load to achieve the flat gain. Passive structures including inductors, transmission lines and bond pads are all simulated using electromagnetic (EM) software (Agilent Momentum).

IV. MEASUREMENT

The circuit is implemented in NXP’s 0.25μm SiGe:C BiCMOS technology with a peak $f_{T}/f_{MAX}$ of 177/216 GHz [6]. The measurement setup and the die photo are shown in Fig. 4 with a total die area of 0.7×0.6 mm².

The measured input return loss is less than -10 dB from 20 to 50 GHz and the reverse isolation is better than 25 dB at 40 GHz, as shown in Fig. 5. The gain and noise performance are shown in Fig. 6. The best $S_{21}$ is 10.5 dB at 26 GHz and the 3-dB gain bandwidth covers 16 GHz to 43 GHz, corresponding to a 90% fractional bandwidth. The measured minimal NF is 2.5 dB at 20 and 26 GHz and the average NF is 3.25 (± 0.75) dB from 16 to 44 GHz. The linearity performance is shown in Fig. 7 for input IP3 ($IP3$) and input 1-dB compression point ($ICP_{1dB}$) respectively. The group delay and phase of $S_{21}$ are shown in Fig. 8 for wideband applications. The LNA draws 10 mA from a 2.4-V power supply (24 mW in total).

Table I shows a benchmark with other silicon-based LNAs operating in the K band. The proposed work achieves the best performance in a combination of low average noise, wide gain bandwidth and sufficient $S_{11}$ bandwidth, covering the full K band from 20 to 40 GHz.
In this paper, the design of an ultra-broad band LNA with 90% fractional bandwidth is presented in a 0.25 µm SiGe:C technology. The input matching is the most crucial part to achieve a broadband noise and power matching. A dual-LC tank matching method is proposed and applied to the LNA design. The measured NF is 2.5-4.0 dB from 16 to 44 GHz. To our knowledge, this work achieves the best average noise performance for silicon based mm-wave broadband LNA designs (fractional bandwidth up to 90%). This LNA also enables a mm-wave front-end system integrated in a low cost silicon based technology for K band and future 5G communication systems.

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REFERENCES

TABLE I PERFORMANCE SUMMARY AND COMPARISON

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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3-dB Gain (dB)</td>
<td>10.5</td>
<td>25.3</td>
<td>12.4</td>
<td>12</td>
<td>13.8</td>
<td>14.2</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>2.5-4.0</td>
<td>2.5-3.2</td>
<td>1.8-2.2</td>
<td>4.5-6.3</td>
<td>3.8-6</td>
<td>2-3.3</td>
</tr>
<tr>
<td>S11&lt;10dB</td>
<td>17-50</td>
<td>N/A</td>
<td>29-33</td>
<td>20-35</td>
<td>29-50</td>
<td>29-43</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>1.8 to 5.9</td>
<td>-13.8@31GHz</td>
<td>-1.3@30GHz</td>
<td>-4.5 to -6.3</td>
<td>-1@37GHz</td>
<td>N/A</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>24</td>
<td>21</td>
<td>98</td>
<td>13</td>
<td>18</td>
<td>38</td>
</tr>
<tr>
<td>Technology</td>
<td>0.25 µm SiGe</td>
<td>0.25 µm SiGe</td>
<td>0.25 µm SiGe</td>
<td>0.18 µm Bi-CMOS</td>
<td>90 nm CMOS</td>
<td>0.15 µm InGaAs pHEMT</td>
</tr>
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*Calculated from Paper