A noise reconfigurable current-reuse resistive feedback amplifier with signal-dependent power consumption for fetal ECG monitoring

A Noise Reconfigurable Current-Reuse Resistive Feedback Amplifier with Signal Dependent Power Consumption for Fetal ECG Monitoring

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***Abstract*— This paper presents a noise-reconfigurable resistive feedback amplifier with current-reuse technique for fetal ECG monitoring. The proposed amplifier allows for both tuning of the noise level and changing the power consumption according to the signal properties, minimizing the total power consumption while satisfying all application requirements. The amplifier together with its amplitude detector and dynamical biasing circuit are implemented in a standard 0.18µm CMOS process. Measurements demonstrate that the proposed current-reuse resistive feedback topology improves the power efficiency of the conventional resistive feedback amplifier, achieving at the same time a good noise efficiency factor (NEF=2.8) and an input impedance of 20MOhm. The amplitude detector and dynamical biasing circuit, which tunes the current in the amplifier according to the signal amplitude, save up to 40% of the total power consumption. The amplifier achieves a measured noise level of 0.34µVrms in a 0.6 to 175Hz band, consuming 6.3µW power.**

***Index Terms*—electrocardiography, resistive feedback, current-reuse, signal dependent power, NEF.**

I. Introduction

High-risk pregnancies are becoming more prevalent because of the progressively higher age of pregnant women. Regular monitoring of fetal electrocardiogram (fECG) can reduce complications and mortality, but it would generate high costs with hospital-based systems. Currently available home-based fetal monitoring systems include a radio, an ADC and frontend amplifiers to be connected with cables to wet electrodes [1]. These systems consume a considerable amount of power, so that a bulky battery is required, making them unfit to ambulatory monitoring. Future fetal monitoring systems should therefore be low cost, highly integrated and low power, to enable miniature batteries and make possible continuous portable monitoring [2].

The front-end amplifiers and the radio are typically the most power-hungry parts in the signal acquisition chain of fetal monitoring systems. As a first step towards the implementation of an ultra-low power fetal monitoring system, a novel, power-efficient frontend amplifier is investigated in this paper.

The amplitude of the fECG strongly depends on gestational age, inter-electrode distance, and measurement orientation, while the required signal-to-noise ratio (SNR) for meaningful analysis of the fECG (e.g. determination of the fetal hart rate) is fixed [3]. Therefore a noise-reconfigurable frontend amplifier covering the required range of input-referred-noise levels with good noise efficiency factor (NEF) would offer better energy efficiency in the actual use than a point solution specified for worst-case SNR [4]. On top of battery size, another important factor to improve user comfort would be the possibility to avoid wet electrodes. This can be made possible by a frontend amplifier featuring high input impedance Z_{in}.

Resistive feedback amplifiers offer high Z_{in} and high CMRR, but suffer from relatively high NEF, mainly because the feedback resistors contribute to the total noise [5]. In this paper, a noise-reconfigurable current-reuse resistive feedback amplifier that achieves high power efficiency together with high input impedance is proposed and optimized in a standard 0.18µm CMOS technology. Several circuit techniques are employed to enhance power efficiency: current-reuse is applied to the amplifier core, a capacitive feedback is used to eliminate DC electrode offsets, and the bias current is made adaptive to the maximum signal amplitude to spare power in user scenarios characterized by small motion artifacts. Measurements show that the noise level of the frontend amplifier can be scaled from $30nV/\sqrt{Hz}$ to $200nV/\sqrt{Hz}$ while consuming 6.3µW to 0.9µW, thus achieving an NEF from 2.8 to 6.6. This level of power efficiency is achieved while providing an input impedance (Z_{in}) of about 20MΩ.

The paper is organized as the follows. In Section II the fECG signal is analyzed and the specifications for a fECG frontend amplifier are derived. In Section III the current-reuse resistive feedback topology is described and compared with the conventional resistive feedback topology. In section IV, the power consumption of the proposed amplifier is optimized employing two techniques: a capacitive DC servo-loop and a dynamic biasing circuit that allows signal dependent power consumption. In section V, the circuit implementation including noise scalability is discussed. Measurement results are presented in section VI, and conclusions are drawn in section VII.

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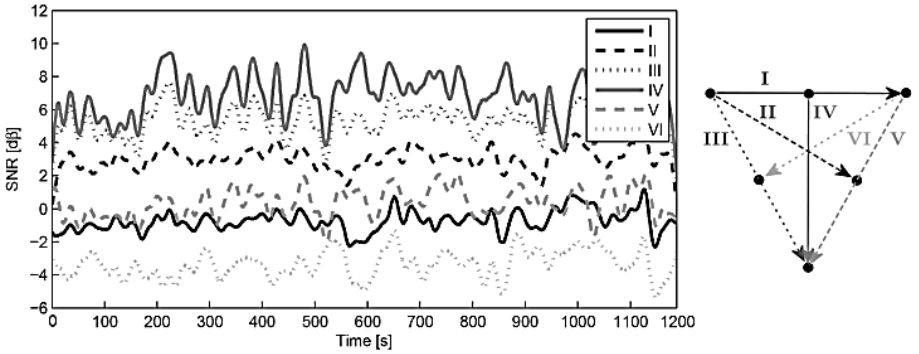

Fig. 1 SNR of the fECG in six bipolar directions as shown by the diagram on the right for a 20 minute segment [4]

II. Fetal ECG Signal and Monitoring System

A. fECG signal and interference sources

Various physiological signals play important roles in fetal health monitoring. The most important one is the fECG, which can be used to determine the fetal heart rate (fHR) and also allows for analysis of the fECG morphology. There are several interference sources in ambulatory abdominal measurements of fECG: the maternal ECG (mECG), the electrohysterogram (EHG) signal that originates from uterine muscle activity, and the motional artifacts (MAs). To enable reliable fECG detection, the influence of these interference sources can be reduced to a large extent with suitable algorithms implemented in a digital signal processor (DSP).

The fetal QRS-complex has detectable amplitude between 3μV and 20μV when measured on the abdomen. This amplitude strongly depends on gestational age, inter-electrode distance, and measurement orientation [3]. Fig.1 shows an example of the influence of the measurement direction on the SNR of an abdominal fECG. In this picture the position of the bipolar electrodes used for fECG measurement on the mother's abdomen is shown on the right by the dark markers, while the corresponding signals are shown in the panel on the left. The SNR for the six electrode pairs defined on the right side of the figure can differ significantly and change over a short time due to the movement of fetus. Therefore, a dynamic selection of the electrode pair with the best SNR during the measurement is essential to obtain reliable fECG detection.

To determine the SNR required for reliable R-peak detection in the fECG signal, we added increasing amounts of white noise to measured fECG signals showing negligible motion artifacts. In this way we could find out the detection error rate (DER) at various SNRs when using the R-peak detection algorithm described in [6]. According to the discussion in [4], for a DER lower than 5%, a minimum SNR of 9dB is required. Based on this specification, the changing fECG signal amplitude detected in our experiments allows for a dynamic adaption of the input-referred-noise level of the measurement system, which mainly depends on the frontend amplifier, while keeping the SNR constant.

Motional artifacts are the largest among all interferers, and their amplitude must be considered to set the gain of the frontend system. Therefore a study is carried out to quantify the amplitude of motion artifacts. Using the bipolar electrode layout shown in Fig. 1, a set of three recordings was made on a person performing tasks like walking, bending, and sitting-up. The maximum amplitude of the electrode motional artifacts was found to be 1mV. In prolonged ambulatory measurements, where the electrode could become less tightly connected to the skin, the amplitude of motional artifact can be as large as 10mV. This large value can be used as an indication of bad electrode connection.

B. Monitoring system and specification

A typical frontend for biomedical acquisition systems includes a frontend amplifier (IA) that defines the noise level of the system, and a second stage amplifier to further increase the gain. Usually the second stage amplifier applies capacitive feedback to define the gain with minimum additional noise.

Based on the discussion about the required SNR, the upper and lower bounds of the noise specification of the frontend system can be derived by the observed fetal QRS amplitude and the minimal SNR for reliable fetal R-peak detection. For a detectable fECG amplitude of 3 to 20 μV, the total in band integrated noise should range from $0.375\mu V_{rms}$ to $2.5\mu V_{rms}$, in case an SNR of 9dB is required. After taking an additional 20% margin for the lowest possible noise level, the input-referred voltage noise density of the frontend can be specified between $30nV/\sqrt{Hz}$ and $250nV/\sqrt{Hz}$ in the signal band of 0.5 to 200Hz.

According to the discussion on the amplitude of motional artifacts, and considering a typical supply voltage of 1.2V for our target IC technology, the gain of the frontend system can be defined as 300 or 30 for long-term use and short-term ambulatory use, respectively. These figures are calculated assuming that a maximum output swing of 0.3V will be needed to guarantee sufficient linearity. We shall suppose that the frontend amplifier must provide a fixed gain of 30 and the second stage amplifier can provide a gain of 10 when needed. The amplitude of the MA also has an impact on the power consumption of the proposed frontend amplifier. Indeed, it sets the optimization conditions for the amplifier, as will be discussed in section IV. Additionally, to enable the possibility of using dry electrodes for high user comfort, the input impedance of the IA should be high (>10MΩ) and the CMRR larger than 60dB.

III. Current-Reuse Resistive Feedback Topology

A. Resistive feedback vs. capacitive feedback

There are three commonly used topologies for chopper stabilized biomedical frontend amplifiers, as shown in Fig. 2(a)-(c). Topology (a) and (b) use capacitors in the feedback network (C_1 and C_2) since capacitors do not add noise to the circuit. In (a), the chopper is at the input of the frontend amplifier. The relation between the equivalent input-referred noise power density of the frontend amplifier and that of the

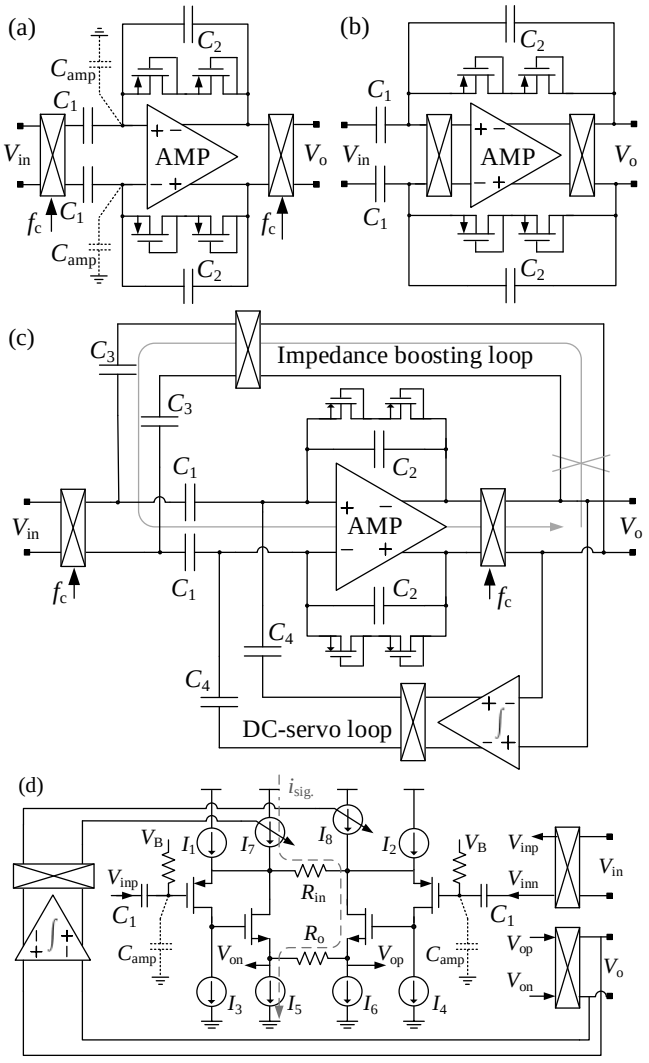

Fig. 2 Possible topologies of frontend amplifiers: (a) capacitive feedback with external chopper, (b) capacitive feedback with internal chopper, (c) external chopper with impedance boosting loop, (d) current feedback

core amplifier (AMP) can be expressed with Eq. (1), where C_{amp} is the input parasitic capacitance of the core amplifier [7]:

$$\overline{v_{in.noise}^2} = \left(\frac{C_1 + C_2 + C_{amp}}{C_1}\right)^2 \cdot \overline{v_{amp.noise}^2} \qquad (1)$$

In order to reduce the NEF of the AMP, the W/L ratio of the input transistors should be designed large enough to take advantage of the high g_m/I_D ratio in subthreshold region. On the other hand, L should be designed large enough to keep the corner frequency of the $1/f$ noise lower than the allowed chopping frequency (f_c), resulting in large C_{amp}. To keep noise and NEF low, C_1 (which sees a signal in the chopping band) should also be designed large, making Z_{in} low. In other words, there is a tradeoff between NEF and Z_{in}: this topology can achieve good NEF and high CMRR, but at the expense of low Z_{in}. Topology (b) has its choppers around the AMP. This topology can achieve higher Z_{in} than (a) since C_1 now works in the signal band. However this topology suffers from a limited CMRR, which depends on the matching of the capacitors C_1.

A positive feedback technique [9] as shown in Fig. 2(c) is often used to boost the input impedance of topology (a). With the capacitor C_3, some current from the amplifier output is supplied to the inputs, to provide part of the current needed by the capacitors C_1 and thus increase the effective input impedance. Assuming an input signal of V_1, the current needed for the capacitors C_1 equals to sC_1V_1. The current provided via C_3 to the input of C_1 equals to $sC_3V_1 \cdot (C_1/C_2 - 1)$. Thus the effective current needed from the amplifier input is $sC_1V_1 - sC_3V_1 \cdot (C_1/C_2 - 1)$. The relation between the boosted (Z_{inb}) and the original impedance ($Z_{in}=1/sC_1$) can be found in Eq. (2), where $A = C_1/C_2$ is the closed loop gain of the amplifier and $k = C_3/C_2$. For example, if k is chosen to be 1 then $Z_{inb} = Z_{in} \cdot A$. Assuming C_1=30pF, C_2=1pF to define a gain of 30, the original input impedance is then 1.3MΩ at 4kHz chopping frequency and the boosted impedance is 39MΩ.

$$Z_{inb} = Z_{in} \cdot \frac{A}{A - (A-1) \cdot k} \qquad (2)$$

Considering the stability, the feedback loop is shown by the arrow line, including the positive feedback loop (C_3) boosting the input impedance and the negative feedback loop (C_1, C_2) defining the gain of the amplifier. Assuming this loop is cut at the output of the amplifier as shown in Fig 3 (c), the open loop transfer function L can be obtained in Eq. (3) when AMP is considered to be an ideal amplifier. Then, the absolute value of L should be less than 1 (at -180 degree phase shift, stability criterion) and k (equals to C_3/C_2) in this equation should be less than $A/(A-1)$ in order to have enough gain margin as shown in Eq. (4).

$$L = \frac{-\frac{1}{sC_2}}{\frac{1}{s \cdot \left(\frac{C_1 C_3}{C_1 + C_3}\right)}} = \frac{-k \cdot C_1}{C_1 + k \cdot C_2} \qquad (3)$$

$$|L| = \frac{k \cdot C_1}{C_1 + k \cdot C_2} < 1 \rightarrow k < \frac{C_1}{C_1 - C_2} \approx \frac{A}{A-1} \qquad (4)$$

If Z_{inb} needs to be above 100MΩ, a k of 1.02 is needed, which leads to an absolute open loop gain $|L|$ of 0.99 (compared with 0.97 when k=1). In this setting, the value of k and $|L|$ further approaches the stability limit k=1.03, $|L|$ =1 that is calculated by Eq. (4) inserting A=30. Therefore with this technique, increasing input impedance can be achieved by increasing k at an increasing risk of instability since the parasitic of the AMP could add to C_3.

Topology (d) [4] applies a feedback with resistive components. In this circuit I_1=I_2, I_3=I_4 and I_5=I_6. The input voltage creates a signal current through R_{in}, which is copied to R_o and defines the output voltage. To obtain the high-pass corner frequency, a current-based DC servo loop is applied to null the DC current in presence of differential electrode offset (V_{DEO}) by tuning $I_{7,8}$. Since now Z_{in} is determined by C_{amp}, the value of C_1 can be made large to reduce the ratio C_{amp}/C_1 without compromising Z_{in}. This topology achieves high Z_{in} without need for positive feedback. It has high CMRR, as the capacitors C_1 are in the chopped domain, but also has relatively high NEF, mainly because of the additional noise contributed by the feedback resistors. In the following subsection, a novel resistive feedback topology is proposed to lower the NEF.

B. Current-reuse resistive feedback topology

The resistive feedback amplifier offers high Z_{in} and CMRR, as discussed. The current-reuse technique has been used to take advantage of the doubled g_m of complementary input devices driven together, and has been widely adopted in capacitive feedback amplifiers, as discussed in [9][10][11]. This current

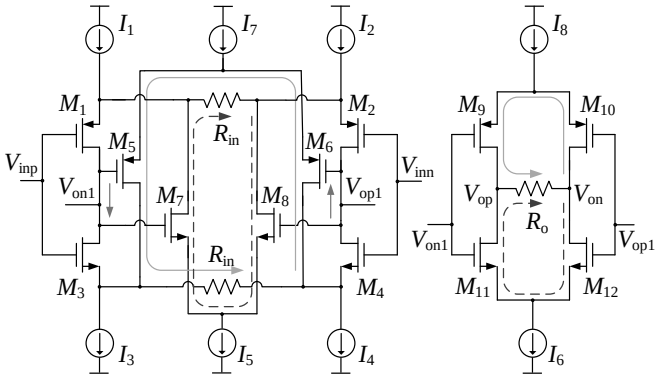

Fig. 3 Proposed current-reuse resistive feedback topology

-reuse approach can also be applied to a resistive-feedback frontend amplifier, as shown in Fig. 3. For simplicity, only the topology of amplifier core is shown here. The AC gain, the current consumption and the input noise of this topology will be analyzed.

- Analysis of the AC gain

The amplifier is built up of an input stage (Fig. 3, left side) and an output stage (the right side). In both stages, complementary input devices are driven together. The devices M_1 and M_2 of the first stage copy the differential input V_{in} = V_{inp}-V_{inn} on the resistor R_{in} (top one), creating a signal current V_{in}/R_{in}, which is shown with the dashed line. This signal current is absorbed by the differential pair M_7-M_8, creating an unbalance $V_{in}/g_{m78}R_{in}$ at its input (where g_{m78} is the transconductance of M_7-M_8). This unbalance contributes to the output voltage V_{op1}-V_{on1}. In the second stage (right side of Fig. 3), the output voltage V_{op1}-V_{on1} is applied to the devices M_{11}/M_{12}, which match the pair M_7-M_8. In this way the unbalance creates a differential output voltage V_o = V_{op}-V_{on}= R_o/R_{in}. In a similar way, the differential input V_{in} is also copied by transistors M_3/M_4 across resistor R_{in} (bottom one), creating a signal current V_{in}/R_{in} as shown in the input stage with a continuous line. This second signal current is absorbed by the differential pair M_5/M_6, creating an unbalance at its input $V_{in}/g_{m56}R_{in}$, which also contributes to the output voltage V_{op1}-V_{on1}. This unbalance is applied to the devices M_9/M_{10} in the second stage, which match the pair M_5/M_6. In this way the unbalance creates an additional differential output voltage V_o = V_{op}-V_{on}= R_o/R_{in}. Summarizing this analysis, both of the two signal paths in parallel contribute to the output voltage, resulting in:

$$A_0 = \frac{1}{g_{m\_in}R_{in}} \cdot \left(2g_{m_o}R_o\right) = \frac{2R_o}{R_{in}} \qquad (5)$$

In Eq. (5), g_{m_in} is equal to g_{m78} or g_{m56} in the input stage and g_{m_o} equals to g_{m1112} or g_{m910} in the output stage.

Considering the topology in Fig.2 (d), two current sources I_5 and I_6 are used to provide the output current, both of which have a minimum value of V_{oM}/R_o (V_{oM} is the maximum output amplitude). In this topology V_{oM}/R_o equals to V_{inM}/R_{in}, where V_{inM} is the maximum input amplitude. Similarly, in the input stage of Fig.3, the two current sources I_5 and I_7 are needed to create the small signal current in the top R_{in} and in the bottom R_{in}, respectively. The minimum value of these two current sources is thus $2{\cdot}V_{inM}/R_{in}$, because a differential pair can only generate a differential current on one input resistor with a maximum value of half of the tail current. For this reason, the current consumption in this part of the input stage (comprising two R_{in}, $M_{5\text{-}8}$ and $I_{5,7}$) is doubled because two differential pairs are deployed for the two input resistors.

It should be noticed that the bias currents in the output stage can be scaled down as I_6 (I_8) = $k_S{\cdot}I_5$ (I_7). The sizes of the pairs in the output stage must then be scaled accordingly as $(W/L)_{9,10}$ = $k_S{\cdot}(W/L)_{5,6}$ and $(W/L)_{11,12}$ = $k_S{\cdot}(W/L)_{7,8}$ and the value of R_o has to be scaled up to R_o / k_S. The value of k_S can be as low as 0.1, which allows saving current while keeping the gain unchanged as shown in Eq. (6).

$$A_{scaled} = \frac{1}{g_{m\_in}R_{in}} \cdot \left(2g_{m_o}k_s\right) \cdot \frac{R_o}{k_s} = \frac{2R_o}{R_{in}} = A_0 \qquad (6)$$

- Analysis of the current consumption

After applying this scaling, the total current consumption of the proposed current reuse resistive feedback amplifier is given by Eq. (7). In this equation two components appear: the first component $2nV_Tg_{M1}$ is the current through the input transistors, assuming weak inversion; the second component $4{\cdot}V_{inM}/R_{in}$ is the sum of the currents I_5 and I_7, each equal to $2{\cdot}V_{inM}/R_{in}$. Due to the k_S scaling the currents in the output stage are negligible.

$$I_{tot} = 2nV_Tg_{M1} + \frac{4V_{in}}{R_{in}} \qquad (7)$$

- Analysis of the input noise

Based on the analysis presented in [4], the input-referred-noise power density $\overline{v_{in.noise}^2}$ of the amplifier can be expressed as shown in Eq. (8). This equation comprises the noise contribution of input transistors $M_{1\sim4}$ and R_{in}. Because there are two small signal currents in parallel that are combined at the output nodes of the input stage, the input-referred noise power density is half of the one found in [4]. The noise contribution of the output stage can be omitted because the gain of the input stage is designed to be around 20dB, thus:

$$\overline{v_{in.noise}^2} = \frac{8kT}{3g_{M1}} + 2kTR_{in} \qquad (8)$$

It is worth noting that there is a trade-off between current consumption and input noise with respect to the selection of R_{in} and g_{M1}. By increasing the value of R_{in}, the second current consumption component in Eq. (7) can be reduced. However, since R_{in} contributes to the input noise, the first current consumption component should be increased to improve g_{M1} and thus reduce the noise contribution from the input devices, keeping the total noise constant.

C. Comparison to the conventional topology

The current consumption and input-referred voltage noise of the proposed amplifier (Fig. 3) and of a conventional resistive feedback amplifier (Fig 2 (d)) are compared in Table (1). In this table, I_0 is the current through the input device and I_R is the maximum small signal current through the input resistor(s): $I_R = V_{inM}/R_{in}$.

As can be seen from the table, the proposed current-reuse current-scaling topology consumes a similar current to the conventional current–feedback topology (provided that the I_R contribution is not dominant). However, it provides approximately half input-referred noise power because of the double effective g_m and halved effective value of the input resistor.

Table 1 Comparison of the proposed and conventional topologies

Parameters	Proposed topology (Fig. 3)	Conventional topology (Fig. 2(d))
Input device current	$2I_1-I_5=2I_0$	$2I_1-I_5=2I_0$
Resistor current	$2I_5=4I_R$	$2I_5=2I_R$
Second stage current	$I_6=k_s\cdot I_5=\cdot 2I_R$	0*
Total	$2I_0+2(1+k_s)I_R$	$2I_0+2I_R$
Input-referred noise	$(8kT/3g_m)+2kTR$	$(16kT/3g_m)+4kTR$
Gain	$2R_o/R_{in}$	R_o/R_{in}

*The conventional topology is single-stage [4]

IV. Power Optimization of the Current Reuse Resistive Feedback Amplifier

Based on the total current consumption in Eq. (7), and the input-referred-noise power density $\overline{v_{in.noise}^2}$ in Eq. (8), for a given noise level, R_{in} can be optimized for minimum current. Indeed, under the constraint of the specified $\overline{v_{in.noise}^2}$, I_{tot} in Eq. (7) can be minimized as a function of R_{in}. The obtained optimal values of R_{in} and I_{tot} are given by Eq. (9) and (10), respectively.

$$R_{in.opt}=\frac{\overline{v_{in.noise}^2}}{4kT}\cdot\alpha \tag{9}$$

$$I_{tot.opt}=\frac{16nV_TkT}{3\overline{v_{in.noise}^2}}\cdot\frac{1}{(1-\alpha)^2} \tag{10}$$

Where $\left(\alpha=\frac{\sqrt{2V_{inM}}}{\sqrt{2V_{inM}}+\sqrt{\frac{8nV_T}{3}}}\right)$

The input voltage V_{inM} includes both the AC component V_s, which has a maximum amplitude of 10mV and is dominated by motion artifact in ambulatory monitoring scenario, and the DC electrode offset V_{DEO} with a maximal value of 50mV. Thus $V_{inM}= V_s+ V_{DEO}$ is dominated by V_{DEO}. As can be observed in Eq. (9) (10), after applying the current-reuse technique and the optimization of the input resistor, a smaller input signal amplitude V_{in} can still provide a smaller $R_{in.opt}$ value, which would lead to less additional input noise and a lower total current consumption $I_{tot.opt}$.

Thus, in order to minimize the amplitude of V_{inM} at the gate of the input transistors and achieve a lower total current consumption, a capacitive DC-servo loop is used in our final implementation to cancel the V_{DEO}. Furthermore, the value of the input-resistor related current (the second component in Eq. (6)) can be made adaptive to the signal amplitude, which (after V_{DEO} cancellation) would be dominated by motion artifacts. A peak detector and dynamic biasing circuit can enable tuning of the input-amplitude related current I_R for motion artifacts in the range between 1mV and 10mV.

A. Capacitive DC servo loop

A capacitive DC servo loop, as shown on the bottom panel of Fig. 4, is used to cancel the electrode offset V_{DEO} at the gate of $M_{1,2}$. The DC servo loop consumes negligible additional current (0.15μA), and this current is independent of the signal amplitude. This approach makes possible to avoid the controlled current sources I_7 and I_8 in Fig. 2 (d), saving biasing current.

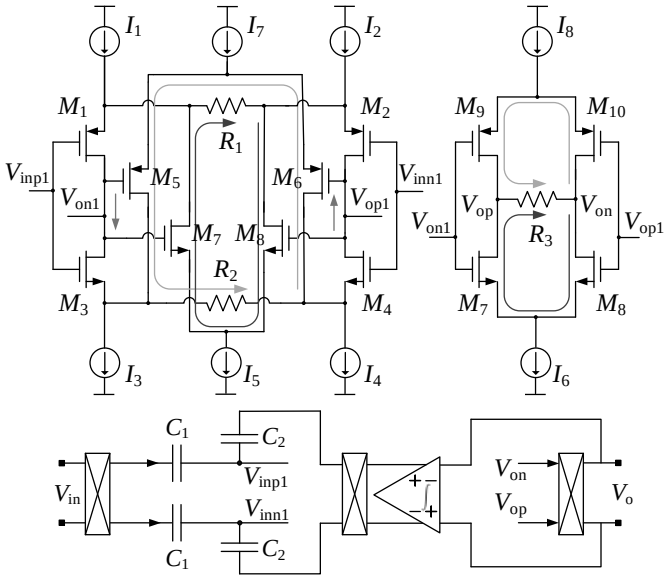

Fig. 4 The proposed topology with capacitive DC servo-loop

In steady-state the charge induced by V_{DEO} on the gate of $M_{1,2}$ should be delivered by the feedback C_2, thus $V_{int.}\cdot C_2 = V_{DEO}\cdot C_1$ where $V_{int.}$ is the output swing of the integrator. The V_{int} should be maximized to reduce the size of C_2 while still ensuring compensation of the 50mV V_{DEO}. A small C_2 minimizes the increment of the equivalent input noise due to capacitive loading of the input node. For a supply voltage of 1.2V, the ratio C_2/C_1 can be kept less than 1/20. It should also be noticed that C_2 reduces the input impedance, since it is in parallel with the parasitic capacitance at the input.

B. Signal dependent biasing

Dynamical/adaptive biasing techniques have been proposed before in literature, one example can be found in [12]. To our knowledge, here it is the first time that the dynamical biasing techniques are applied to the current feedback amplifier. To provide a dynamical biasing current for the input stage according to the input signal amplitude, an amplitude detector is designed. This circuit is implemented as shown in Fig. 5. It is based on a different slew rate for a rising signal and a falling signal. When there is a rising signal V_{in}, transistor M_4 will be turned on and charge the output capacitor, forcing the output node V_{peak} to follow the input voltage V_{in}. When there is a falling signal, transistor M_9 will be turned off and the charge on the capacitor will be discharged through a large resistor. In this way, the peak value of the amplitude is preserved for a certain period (the time constant RC is 1s, the R is implemented by active device). There are two detectors used, which share the same R and C. The input of each amplitude detector is connected to one of the two outputs of the proposed amplifier.

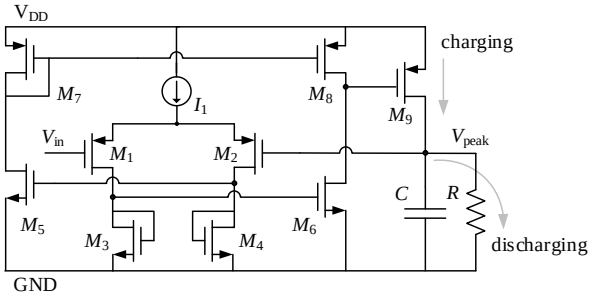

Fig. 5 Schematic of the amplitude detector

Table 2 Comparison of the current consumption of resistive feedback topologies with different servo-loops and biasing circuits

	Conventional with Current DC Servo-loop	Current-reuse with Capacitive DC servo-loop	With peak detector &dynamic biasing circuit	
			V_{inM}=10mV	V_{inM}=1mV
Input noise	32nV/Hz$^{1/2}$	32nV/Hz$^{1/2}$	32nV/Hz$^{1/2}$	31nV/Hz$^{1/2}$
Optimized R_{in}	12 kΩ	5.6kΩ	5.6kΩ	5.6kΩ
Input device bias	7.7 µA	2.2µA	2.2µA	2.2µA
Resistor related bias	2.4 µA	4.3µA	4.3µA	0.4µA
DC-servo bias	0.15µA	0.15µA	0.15µA	0.15µA
CMFB circuit bias	0.8 µA	0.65µA	0.65µA	0.65µA
PD & Biasing circuit	Not used	Not used	0.3µA	0.3 µA
Total bias current	11.05 µA	7.30µA	7.60µA	3.70 µA
NEF	4.1	3.3	3.4	2.3

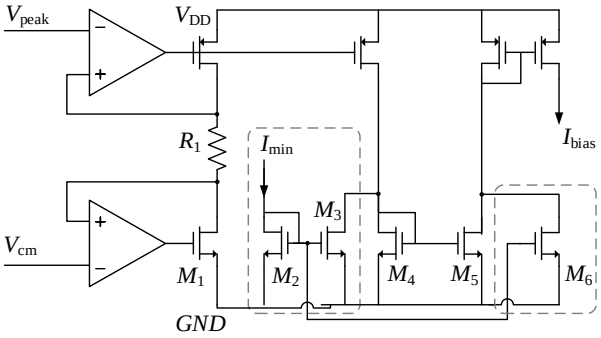

Fig. 6 Schematic of the dynamic biasing circuit

A dynamic biasing circuit (Fig. 6) is used to provide the biasing currents $I_{5\text{-}8}$, which are scaled with the signal amplitude detected by the circuit in Fig. 5. The two input amplifiers in Fig. 6 force the voltage at the two terminals of the resistor to be equal to the output of the peak detector, V_{peak} and the common mode output voltage V_{cm}, respectively. The resistor R_1 converts this maximum differential signal amplitude to a current with a proper value, which is set to 1.1 times the minimal current that is needed in the amplifier to generate the corresponding signal amplitude.

Besides, for reliability reasons, the minimum I_{min} sufficient for a 1mV input signal amplitude is supplied by M_2, M_3 and M_6. When an amplitude of <1mV is detected, transistors M_4 and M_5 are turned off, keeping $I_{bias}=I_{min}$. This prevents the biasing circuit to reduce the current to an undesirable low level. The amplitude detector and the dynamical biasing circuit consume 0.3µA and work with a motion artifact range between 1 to 10mV.

Table 2 shows a comparison of the simulated current consumption in the resistive feedback current-reuse amplifier with a current-based DC servo-loop topology, with a capacitive servo-loop topology and with the dynamic control of the biasing current at different motion artifact amplitudes. All the topologies are optimized for an input noise level of 32nV/$\sqrt{\text{Hz}}$ and have a supply voltage of 1.2V. The simulation results show that the current-reuse technique together with the capacitive DC servo loop saves 30% of the current in a conventional resistive feedback amplifier achieving the same input noise. Applying dynamic biasing according to the signal amplitude, the current consumption can be further reduced to 3.7µA for low motion artifacts, achieving an NEF of 2.3.

V. Circuit Implementation

The proposed resistive feedback, current-reuse amplifier is designed and implemented together with a second stage amplifier. The *W/L* ratios of the input pairs are designed to be 150µm/1.0µm and 300µm/1.0µm for the NMOS pair and PMOS pair respectively. The values of the input capacitor C_1 and the DC servo feedback capacitor C_2 are designed to be 24pF and 1.2pF respectively. There are two gain settings implemented by the second stage amplifier together with off-chip components, providing a total gain of 30dB or 50dB. The core amplifier is implemented by a classic single-ended folded cascode amplifier together with capacitive feedback.

According to the discussion in Section II, applying noise scalability, the energy consumption of the frontend amplifier can be significantly reduced in the specified input noise range. This noise scalability should be realized by tuning the current through the input devices and changing the value of feedback resistors at the same time, since the optimal value of R_{in} is also a function of the noise voltage density $v_{in.noise}$. The values of $R_{in.opt}$ at different noise levels can be calculated by Eq. (8) and then verified and adjusted with simulations.

In practice, it is cumbersome to change R_{in} continuously while scaling the noise. Thus, in the IC implementation, two modes are introduced with two different values of R_{in}, for low and high input noise level. The currents $I_{3,4}$ will be tuned to obtain the right noise level within each mode, and the value of R_o is chosen according to R_{in} to keep the gain constant. The optimized values of R_{in} and the simulated performance for 10mV maximum motion artifacts are summarized in Table 3. The current and power listed in the table include the core amplifier, the CMFB circuitry and the DC servo-loop.

Table 3 Design parameters in two modes for the frontend amplifier when V_{inM}=10mV

Mode	$v_{in.noise}$	R_{in}	Bias Current	NEF	Power
Low noise	32(nV/$\sqrt{\text{Hz}}$)	5.6 kΩ	7.6µA	3.4	9.1µW
Low power	200(nV/$\sqrt{\text{Hz}}$)	392 kΩ	1.1µA	8.1	1.3µW

VI. Measurement and Benchmarking

The proposed current-reuse resistive feedback amplifier is implemented in a standard 0.18µm CMOS process. The frontend amplifier with DC servo-loop, the second stage

amplifier, the amplitude detector, the dynamical biasing circuit and the buffers to drive the off-chip load are shown on the die-photo (Fig. 7). The circuit core of the chip occupies an area of 0.9 mm^2. The performance of this design is verified by suitable measurements.

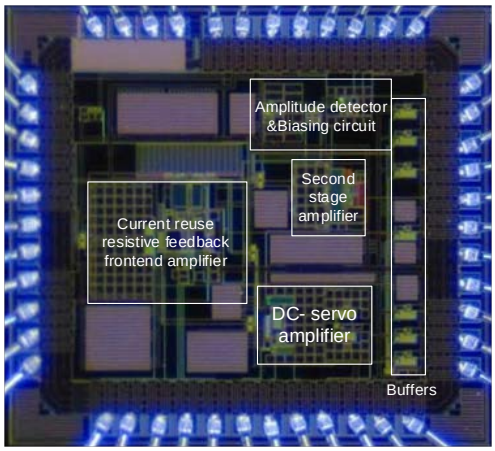

Fig. 7 Die-photo of the prototype amplifier

A. *Electric measurements*

Fig. 8 shows the measured AC transfer of the amplifier. The small signal gain is 50dB/30dB. The -3dB bandwidth is 0.3~172Hz, which is determined by the second stage amplifier. The linearity of the amplifier is tested by a 10Hz, $1mV_{pp}$ sinusoid signal at the high gain setting. Fig. 9 shows the output spectrum. The second and third harmonic components are respectively 53dB and 51dB lower than the fundamental component (150mV), resulting in a total harmonic distortion (THD) of 0.4%.

The noise performance of the amplifier for the two noise levels is measured with high gain setting (50dB) for 1mV maximum signal amplitude. The result is shown in Fig. 10. In the low-noise high-power mode, an output noise floor of $9.8\mu V\sqrt{Hz}$ is measured, corresponding to an input-referred thermal noise floor of $32.7nV/\sqrt{Hz}$. The total input-referred noise V_{rms} is 0.43μV in a signal band of 175Hz including the remaining 1/f noise component. In the high-noise low-power mode, an output noise floor of $5.9\mu V/\sqrt{Hz}$ is measured, corresponding to an input-referred noise floor of $196.7nV\sqrt{Hz}$. In this case, a V_{rms} of 2.6μV in the signal band of 175Hz is achieved.

The amplifier core consumes 6.3μW (NEF=2.8) and 0.9μW (NEF=6.6) for the two noise settings at 1mV motion artifact, including the proposed resistive current-reuse frontend amplifier and the second stage amplifier. The reason for the high value of NEF at the high noise setting is that the total current consumption in this case is more dominated by the DC servo loop, the second stage amplifier and the peak detection/dynamical biasing circuit. Therefore, the signal dependent dynamical biasing scheme can be switched off in high noise mode to save power.

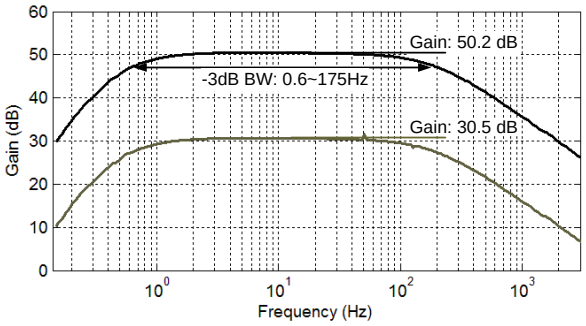

Fig. 8 Measured AC transfer of the amplifier

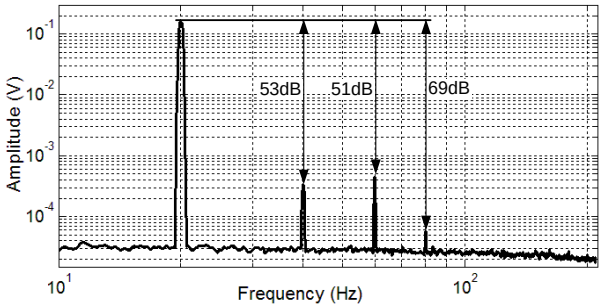

Fig. 9 Measured output spectrum of the amplifier for a $1mV_{pp}$ input signal

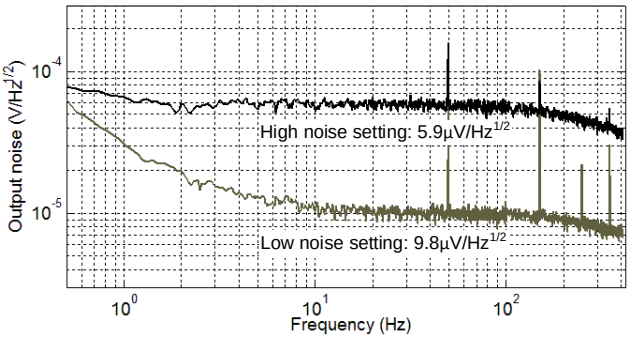

Fig. 10 The output voltage noise spectral at low power and low noise mode

B. *Benchmarking and discussion*

The proposed current-reuse resistive feedback amplifier together with the peak detector and dynamical biasing circuit is compared to previous related works in Table 4. The supply voltage of this amplifier is the lowest. The measured THD at $1mV_{pp}$ input is acceptable considering the reduced supply. The gain and CMRR of this work are in line with other works. The bandwidth and noise level suit well the fetal monitoring application. There are two noise settings of the proposed amplifier: 0.4μVrms, (6.3μW power) and 2.6μVrms, (0.9μW power). The proposed topology achieves better power efficiency (NEF) than the resistive feedback topology in [5] thanks to the current reuse, the optimization of the input resistance for minimum power consumption, and the signal dependent current biasing. Even compared to capacitive feedback amplifiers without current reuse technique [7][8], the NEF of this amplifier is better.

The proposed current reuse resistive feedback amplifier provides an input impedance of about 20MΩ at 50Hz, which is well beyond a chopper-stabilized capacitive feedback amplifier without impedance boosting technique. Compared with other chopper-stabilized resistive feedback amplifier without current

Table 4 Benchmarking of the proposed low-voltage amplifier with other works

	[7]	[5]	[8]	[13]	This work
Topology	(a)	(c)	(a)*	(b)*	Proposed
Technology	0.8µm	0.5µm	0.18µm	0.18µm	0.18µm
Supply (V)	1.8	3.0	1.8	1.8	1.2
Gain (dB)	41/50.5	52/58/64/68	40	40	30/50
Bandwidth (Hz)	0.4-180	0.5-125	0.5-100	0.5-100	0.6-175
THD @input amplitude	0.1%@5mVpp	0.5%@5mVpp	N/A	N/A	0.4%@1mVpp
Noise (μV_{rms})	0.95	0.65	0.91	0.8	0.4/2.6**
NEF	4.6	9.2	5.1	12.3	2.8/6.6**
Power (µW)	1.8	33.3	4.5	19.8	0.9/6.3**
CMRR (dB)	>100dB	>120	>90	82	>70
Z_{in} (Ω)	5M	~1G	>500M	2G	20M

*with impedance boosting **two noise settings

reuse [5], the 20MΩ input impedance provided by proposed amplifier is, however, rather low. There are two reasons for this low input impedance. First in this design, a capacitive DC servo-loop is used, which adds 1.2pF capacitance to the input of the amplifier. Second, in other designs, only the PMOS transistors are driven, and their bulk (N-Well) is connected to the source. In this way, the parasitic capacitance to ground is minimized. In our design, both PMOS and NMOS devices are driven, and the bulk of NMOS has to be connected to ground increasing the total capacitance to ground. In general, the proposed design trades-off input impedance for better power efficiency compared to other resistive-feedback implementations [5].

For capacitive topologies, the positive feedback technique shown in Fig. 2(c) has been proposed in [8] to boost the input impedance of topology (a) and (b) in Fig. 2. There are examples showing a wide range of boosted impedance from 30MOhm [14] to 500MOhm [8], because the optimum value of C_3 is rather difficult to control at implementation level, as discussed in section III.A. It is worth noting that the positive feedback technique can also be used in the proposed resistive feedback amplifier to boost the input impedance, if the application requirements demand very large input impedance.

CONCLUSION

A noise-reconfigurable current reuse resistive feedback chopper-stabilized amplifier is presented in this paper. The amplifier topology intrinsically provides higher input impedance than capacitive feedback chopper-stabilized amplifiers with external chopper. Several techniques are employed to enhance power efficiency: current-reuse is applied to the amplifier core, a capacitive feedback is used to eliminate DC electrode offsets, the value of the input resistor is optimized for high efficiency and the bias current is made adaptive to the maximum signal amplitude to spare power in user scenarios characterized by small motion artifacts. The amplifier is designed and implemented in a 0.18µm CMOS technology. Measurements show that the noise level of the frontend amplifier can be scaled from $32nV/\sqrt{Hz}$ to $197nV/\sqrt{Hz}$ while consuming 6.3µW to 0.9µW from a 1.2V supply, achieving an NEF from 2.8 to 6.6. This power efficiency is achieved while providing an input impedance (Z_{in}) of 20MΩ when chopping is on. The proposed topology can provide even higher input impedance, when applying suitable impedance boosting techniques.

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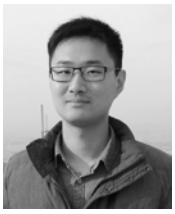

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