Analogue frontend amplifiers for bio-potential measurements manufactured with a-IGZO TFTs on flexible substrate

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***Abstract*— Three novel differential amplifier topologies using double gate a-IGZO TFTs on flexible substrate are presented in this paper. The designs exploit positive feedback and a load with self-biased top gate to achieve the highest static gain in single stage a-IGZO amplifiers reported to date. After fabrication, the three amplifiers exhibit respectively a static gain of 14 dB, 21.5 dB and 30 dB, with a bandwidth of 2 kHz, 400 Hz and 150 Hz. Also, for each circuit the input referred noise has been measured to be 420 μV_{rms}, 195 μV_{rms} and 146 μV_{rms}, respectively. Based on these results, the a-IGZO amplifier providing the highest gain is suitable as front-end for heart rate measurements and, with some further optimization verified in simulation, can also be used for other bio-potential applications, like electro hysterogram and electro cardiogram.**

***Index Terms*— a-IGZO, amplifier, bio-potential, ECG, EMG, EHG, flexible, flicker noise, front-end, thin film transistor.**

I. Introduction

HEART, muscles in activity and neural tissues generate bio-potentials, which are by nature signals distributed over the body surface. However, ambulatory bio-potential measurements are often impaired by patient movements, which induce strong variations in the impedance of the measurement electrodes. This causes large unwanted signals, called “motion artefacts”, which are typically in the same frequency range as the bio-potentials, and thus difficult to distinguish from the target signals. Compared to traditional methods of bio-potential monitoring using bulky wet and dry passive electrodes, ultra-light electrodes in adhesion to the skin and integrating analogue front-ends can potentially reduce motion artefacts, while increasing the robustness to common-mode electric disturbances like e.g. interference from the mains. This is because a very light electrode is likely to experience small mechanical forces and thus small alterations of the mutual position between electrode and skin during the movements. A technology platform able to manufacture ultra light-weight circuits on large area flexible substrates would thus be ideally suited to measure bio-potentials distributed on the body surface, while improving resilience to motion artefacts and interferers. Large-area electronics manufactured at near to ambient temperature on flexible plastic substrates seems thus an excellent fit to medical applications based on bio-potential measurements.

A first well-known application example is multi-led electro cardiogram (ECG) acquisition. Another interesting application is presented in [1], where the electro hysterogram (electrical activity due to the uterus contractions - EHG) is monitored by a matrix of electrodes placed on top of the abdomen of pregnant women. From the analysis of the EHG signals over a certain area the contraction conduction velocity can be extracted, which can be used to estimate preterm delivery with high accuracy. Further examples include EMG [2] and EEG measurements [3], muscular stimulation [4], etc.

Crucial to the development of electronics on flexible foils are semiconductor materials which can be processed at low temperature. The most popular are probably pentacene [5], amorphous Silicon (a-Si) [6], and amorphous Indium-Gallium-Zinc Oxide (a-IGZO) [7]. This last material is gaining increasing interest due to its higher mobility [8], which in circuits leads to higher transconductance, higher gain and lower thermal noise. Also the large area uniformity of a-IGZO [9] is very relevant to circuits, as it results in better matching, higher resilience to common mode disturbances, and lower offsets.

Many applications of a-IGZO Thin Film Transistors (TFTs) have been demonstrated already, such as large AMOLED display backplanes [10], USB powered NFC tags [11], and flexible x-ray imagers [12].

In order to enable all these applications, high-performance analogue, digital and mixed-signal circuit blocks manufactured with a-IGZO TFTs on flexible substrates need to be developed. Analogue building blocks such as amplifiers have been already shown [13] – [18], and also DACs [19], and logic circuits [11]. On the other hand, some other basic blocks are still not available. For instance, the implementation of stable reference circuits, such as bandgap references, is not trivial with a-IGZO, due to the lack of bipolar transistors and

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diodes. For this reason, it is difficult to build stable biasing circuits and supply regulators in this technology.

The focus of this paper is on analogue front-end amplifiers for bio-potential measurement manufactured with a-IGZO TFT on flexible substrate. More in detail, novel a-IGZO single stage amplifiers with high gain, which can be used as first stage in a bio-potential front-end chain, are proposed, designed and characterised. Increasing the gain of the first stage in a front-end relaxes the noise requirements of the following gain stages, thus improving overall power consumption and area occupation. Special attention is devoted to the experimental analysis of the amplifier noise performance, which is typically missing in prior literature, and to understand if these blocks can successfully support different kind of applications based on bio-potential measurements.

The paper is further organised as follows: In Section II the process technology is introduced, together with a model of the a-IGZO TFT channel current and noise. In Section III three novel a-IGZO high-gain amplifier topologies are introduced and analysed. Measurements of these amplifiers are presented in Section IV. In Section V the measurements results are discussed, followed by some conclusions in Section VI.

II. Process Technology and TFT Modelling

In this section, an overview of the a-IGZO TFT fabrication process is given, followed by an introduction to the modelling of channel current and noise.

A. a-IGZO TFT devices

The devices manufactured in our technology are TFTs with a-IGZO as semiconductor. Since only a-IGZO is used, only n-type transistors are available.

Fig. 1 shows the cross section of a typical device, which has a staggered bottom-gate top-contact structure. All the layers are processed at a maximum temperature of 200 ºC on top of a flexible PEN plastic substrate, which is hold on glass during manufacturing and released afterwards. The circuits realized can thus be bent without modifying in significant way their electrical characteristics, as it has been shown in [20].

First, a 100 nm chromium-molybdenum metal film, which provides the gate layer, is sputtered on top of the flexible plastic substrate, and patterned using photolithography. On top, a 200 nm SiO_2 gate insulator is formed by a PECVD process, which is followed by the DC sputtering of the IGZO layer with a thickness of 12 nm. After the IGZO deposition a photoresist layer is spin coated on top, and is exposed using maskless lithography tools. The IGZO layer is thus wet-etched in an oxalic acid solution, followed by the stripping of the photoresist layer. Above the semiconductor there is an Etch-Stop Layer (ESL), which prevents damage of the IGZO when processing the other layers. In order to create the contact openings, the ESL layer is etched and a second metal layer is sputtered to form the source and drain. Finally, a passivation layer (interlayer) is sputtered on top of the second metal layer in order to avoid interaction with the environment, and protect the layers underneath from further processing steps. The overall process is made on a 32 cm by 32 cm substrate.

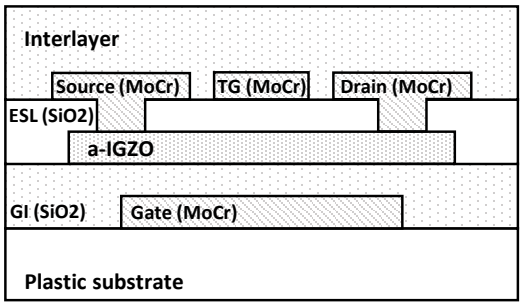

Fig. 1: Cross section of an a-IGZO TFT. The layer stack is formed as follows (from the bottom): Plastic substrate, gate metal, gate insulator (GI), a-IGZO, ESL, source/drain metal, and final insulator (interlayer).

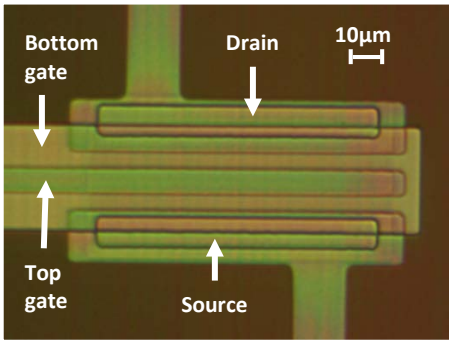

Fig. 2: Picture of a fabricated double gate TFT.

Due to the presence of the ESL on top of the semiconductor, it is possible to have an area overlapping the channel on the second metal layer, which can be used as a second (or top) gate (TG in Fig. 1). Because of the extension of the connection from the contact opening, the top gate will only have a partial overlap with the channel, as shown in Fig. 1. Fig. 2 shows a microscope picture of a double gate TFT, in which the metallization of gate, drain, and source are recognizable.

The minimum feature size of this technology is 5 µm, which results in a minimum channel length of 15µm for single gate devices, and 30 µm for double gate devices.

B. Channel current modelling

Fig. 3 shows the measured transfer curves of 100 single gate TFTs with the same aspect ratio, measured on the same foil, while Fig. 4 shows a sample output characteristic from this population of devices. In order to describe these characteristics, the analytical physical-based model described by Ghittorelli et al. in [21] has been implemented in a Verilog-A script, and run on an electrical simulator.

To extract the model parameters, first, the transfer and output curves have been measured on groups of devices with length scaling from 200 µm down to 15 µm and width scaling from 200 µm down to 15 µm. Then, the parameters for the channel model are extracted according to the procedure described in [22]. It has been observed that the model in [21] tends to overestimate the drain current due to contact effects. For this reason, the contact model described in [23] has been added to the simulation model, and its parameters have been

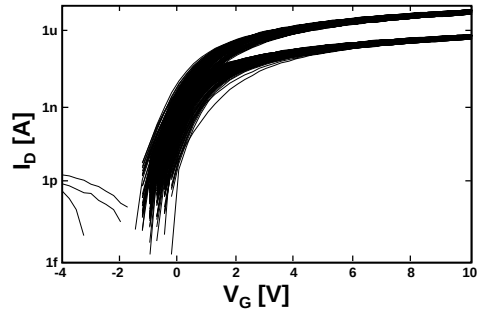

Fig. 3: Transfer characteristics measured on 100 single gate TFTs manufactured on the same foil, with W/L = 100 µm/30 µm at drain voltage of 0.1 V and 1 V

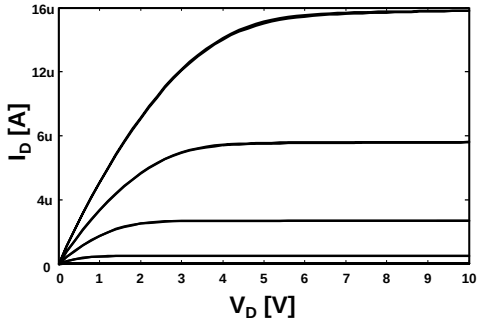

Fig. 4: Output curves measured on a TFT with W/L=100µm/30µm at V_G = {2; 4; 6; 8; 10} V

suitably extracted from the measurements.

In order to model the electrical characteristics of double gate TFTs, an approach similar to [24] has been followed. It has been observed that the TG bias modifies the transfer curves in two ways: a threshold modulation for negative TG bias, and a modulation of the on-current for positive TG bias. As observed in [24], threshold modulation occurs for negative TG-source bias voltages, which causes depletion of the region underneath the TG. The threshold voltage of the whole channel will increase as the depletion layer under the top gate increases, and this can be justified by a capacitive division between the bottom gate and top gate potential.

On the other hand, when a positive voltage is applied to the TG, a modulation of the channel on-current is observed. Under this bias condition, indeed, accumulation in the semiconductor layer under the TG occurs. If the main TFT channel above the bottom gate is formed, the total on-current is increased due to the presence of the second accumulation sheet. If the main TFT channel is absent, due to the bottom gate (VG) bias, the device remains off because the second accumulation sheet cannot reach the source and drain contacts.

Taking into account these phenomena, the influence of the TG bias on the transistor characteristics has been modelled for $V_{TG} < 0$ V as follows:

$$V_{TH} = V_{TH,0} - \eta V_{TG} \quad (1)$$

And for $V_{TG} > 0$V as:

$$I_D = I_{D,0}(1 + \alpha V_{TG}) \quad (2)$$

(1) describes the threshold modulation as linear function of TG voltage by means of a top gate coupling coefficient η, as explained also in [24].$V_{TH,0}$ is the value of threshold voltage with zero applied TG bias. For this particular technology, the thickness of the gate insulator layer is double compared to the ESL, and, due to different processing, the dielectric constant of the gate dielectric is lower than that of the ESL. This leads to a η which is as large as 2.1. The on-current increase with positive V_{TG} is modelled in (2) with a linear dependence of the on-current on the TG voltage, through the coefficient α. The value of α is extracted from measurement and is 0.25 V^{-1}. $I_{D,0}$ represent the drain current with zero applied TG bias. Fig. 5a shows the typical transfer characteristics obtained measuring a double gate TFT. Confirming our analysis, it can be observed that the transfer curve moves as the TG voltage increase from negative towards zero. For positive TG the subthreshold region is basically independent on V_{TG}, while the above threshold current increases as the TG voltage becomes more positive.

In Fig. 5b a comparison between the model and the measurements is shown for negative TG bias voltages in the range -5 V to -1 V. A very good agreement is reached. Fig. 5c shows the same comparison for positive TG bias voltages of 0 V, 2 V and 5 V. In this bias region, a larger disagreement between model and measurements can be observed. This is because the on-current modulation factor α is actually not exactly constant for changing TG bias. For this reason, further studies on the modelling of TG bias influence on the TFT

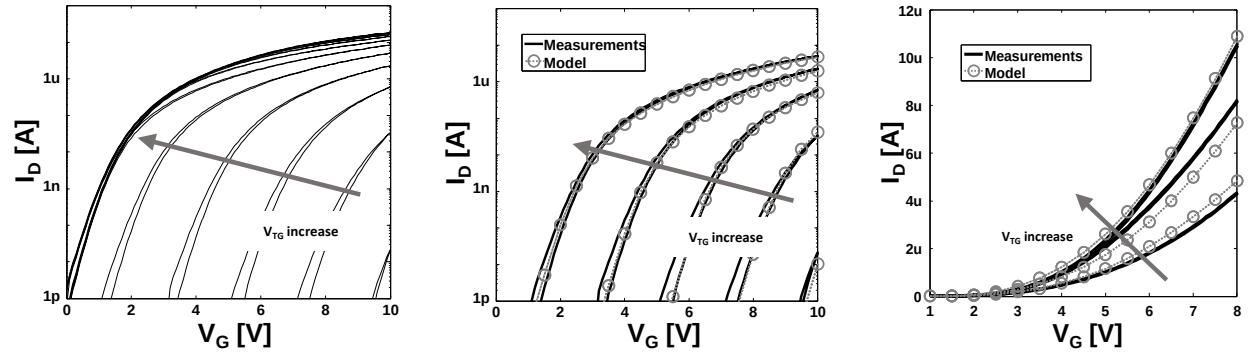

Fig. 5a: Transfer characteristics measured with V_{TG} in the range {-5,5} and a step of 1 V, increasing in the direction of the arrow. **5b:** Detail of negative V_{TG} measurements and simulations: a threshold modulation is observed. **5c:** Measurements and simulations for positive V_{TG} = 0; 2; 5 V: an on-current modulation is observed.

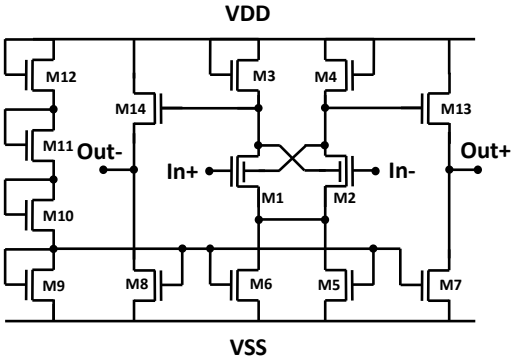

Fig. 6: Schematic of the amplifier with positive feedback and diode connected load.

characteristics are needed.

C. Device noise modelling

Current noise in field effect transistors is typically modelled by two main contributions: thermal noise and flicker noise. The former has been described using the Johnson formulation [25]:

$$S_{ID}(f) = 4k_B T(2/3 g_m) \quad (3)$$

Where k_B is the Boltzmann constant, T is the temperature, and g_m is the transconductance of the device.

For low frequency noise, the Hooge model described in [26] is used. Because of the dependence of the thermal noise on the transcoductance, numeric differentiation is typically needed to simulate thermal noise. This approach is prone to numeric errors. To avoid this, and also to have a tool which enables hand calculations, an analytic expression of the channel current has been used here [27]:

$$I_D = \frac{W}{L}\beta[V_{OV,S}{}^{\gamma} - V_{OV,D}{}^{\gamma}] \quad (4)$$

where the overdrive voltage $V_{ov,X}$ is defined as:

$$V_{OV,X} = V_{SS}\ln[1+\exp(\frac{V_G - V_X - V_{TH}}{V_{SS}})] \quad (5)$$

and X refers to source or drain nodes, while V_{SS} is the subthreshold slope. The parameters of this analytic model are extracted from measurements according to [28]. The transconductance is then calculated analytically as $\partial I_D/\partial V_G$, with I_D defined in (4), and it is used to calculate the thermal contribution to the total TFT noise Power Spectral Density (PSD) in simulation.

Flicker noise in a-IGZO devices is well described by mobility fluctuation theory, as shown in [29], and its PSD can be described as follows:

$$S_{ID}(f) = \frac{\alpha_H q I_D{}^2}{fWLC_i(V_{GS} - V_{TH})} \quad (6)$$

In (6) the PSD is function of geometrical TFT parameters, the bias point, and the Hooge coefficient α_H. The latter has been extracted from noise measurements on different circuit topologies, and is equal to 0.025. This value determined for α_H is well in line with values previously reported in literature [29], [30] for a-IGZO TFTs.

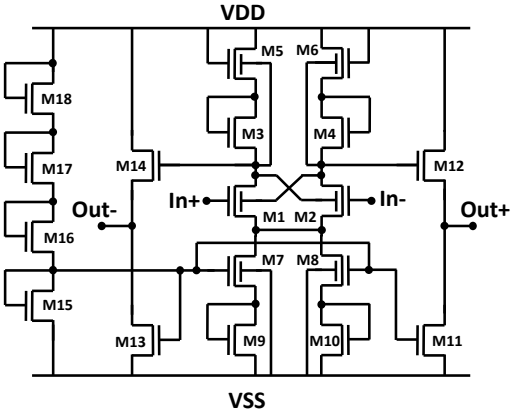

Fig. 7: Schematic of the amplifier positive feedback and a new topology for the load circuit.

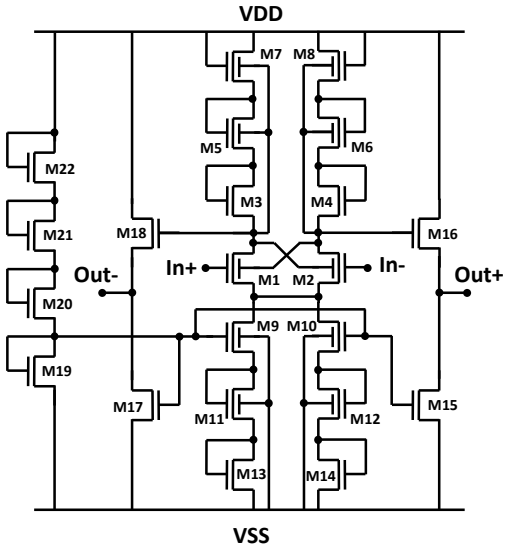

Fig. 8: Amplifier with positive feedback and a load circuit (M_3, M_5, and M_7) which drastically improves DC gain.

III. Design of Novel IGZO Amplifier Circuits

In this section, three novel amplifier topologies built using unipolar a-IGZO TFTs are presented. The main goal of these circuits is to improve the DC gain provided by a single stage amplifier. This is important and challenging, because unipolar TFT circuits, like the ones explored here, typically suffer from reduced gain. The best a-IGZO single stage amplifier reported in prior literature is described in [31], and its gain is 9.86 V/V.

Our first amplifier consists of a simple differential pair with positive feedback applied to the top gates of the input devices, which is used as a starting point for further optimization. The other two architectures contain non-conventional load circuits which exploit the top gate available in our technology.

Also, a first attempt to realize a reliable bias scheme for a-IGZO circuits is shown.

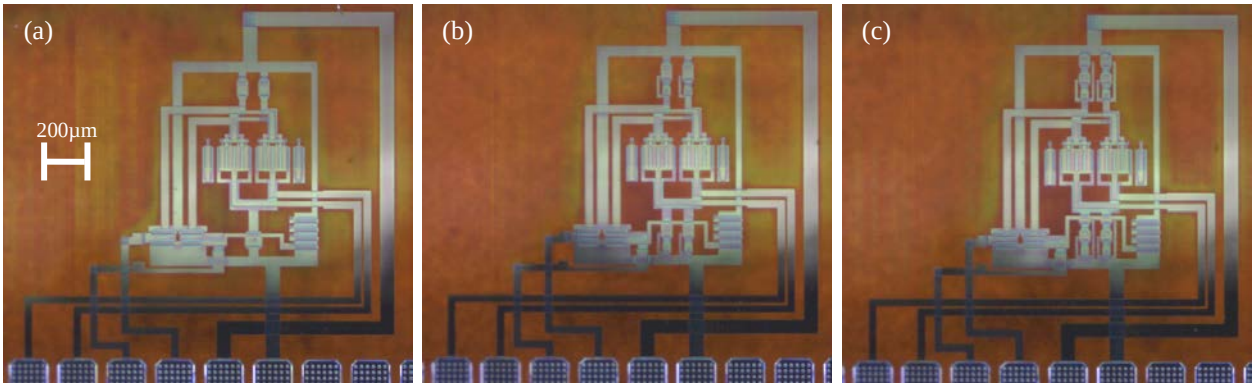

Fig. 9: Microphotograph of the amplifiers presented in Sections III.A (a), III.B (b), and III.C (c).

A. a-IGZO differential amplifier with positive feedback

Fig. 6 shows the schematic of the first topology studied. M1 and M2 are double gate devices, connected as a source coupled differential pair. Transistors M3 and M4 are n-type TFTs in a diode connected configuration, and act as load of the differential amplifier. The top gate of the drivers in each branch is connected to the output of the opposite branch, in a cross coupled fashion, creating a positive feedback which increases the gain. Analytically, the small-signal gain can be calculated to be:

$$G = \frac{g_{m1,2}/g_{m3,4}}{1-\alpha g_{m1,2}/g_{m3,4}} \tag{7}$$

in this equation the open loop gain is given by the ratio of driver to load transconductances, multiplied by the top gate coupling factor. Since the top gate-source DC bias point (V_{TG}) is positive, the coupling coefficient is reduced to on-current modulation coefficient α, which is 0.25. The loop gain is less than one, and the closed loop gain is increased by the positive feedback.

At the output stage, a buffer, which consists of a source follower stage M13-M14, is used to interface the amplifier with the measurement setup. It also has the function of level shifter, and brings the output DC voltage to a bias level similar to the input nodes. This enables the straightforward use of a resistive feedback network around the amplifier, if needed.

Transistors M5 to M12 compose the bias circuit of this amplifier. The supply voltage is divided by four through a voltage divider composed by M9 to M12. This voltage is then used to bias the gate of M5 to M8, which are used as tail current source for the amplifier stage and the buffers. Above threshold and in saturation region (4) becomes:

$$I_D = \frac{W}{L}\beta(V_{GS}-V_{TH})^{\gamma} \tag{8}$$

From eq. 8 the output bias point as function of the supply voltage can be easily calculated as:

$$V_O = V_{CC} - \left[\sqrt[\gamma]{\frac{S_6}{S_3}}(V_{CC}/4 - V_{TH}) + V_{TH}\right] - \left[\sqrt[\gamma]{\frac{S_{14}}{S_8}}(V_{CC}/4 - V_{TH}) + V_{TH}\right] \tag{9}$$

Here S_i represents the W/L ratio of the TFT M_i and V_{CC} $=V_{DD}-V_{SS}$ is the supply rail. From (9), it is easy to observe that, if $S_6=S_3$, and $S_{14}=S_8$, the output bias point will be equal to half of the supply rail, independently on the value of threshold voltage. Realising an output voltage bias point which is insensitive to threshold variations can be very useful in case of cascading different gain stages. Also, it allows alignment of the input and output common mode levels, enabling the use of resistive feedback networks. The proposed threshold-insensitive biasing of the output node works well as long as the devices are in saturation regime, and if the devices are matched. This biasing approach provides an efficient way to fix the voltage bias points independently of TFT threshold variations, which can be as large as a few volts between different technology batches. The drawback is that the bias current is not set directly by the biasing circuitry, but it is defined by the tail current source topology and the supply voltage. For this reason, the three amplifier topologies presented in this section will have different bias currents at the same supply voltage.

B. a-IGZO differential amplifier with positive feedback and source degenerated load with self-biased top gate

The amplifier presented in this section uses a new topology which increases the output resistance, and thus the DC gain. As shown in Fig. 7, M5 and M3 are diode connected TFTs in series, and the top gate of M5 is connected to the source of M3. When the current in this branch increases, the voltage across M_3 increases, and the V_{TG} of M_5 becomes more negative. When this happens, M_5 is depleted of charges and becomes more resistive. Therefore, the total small signal output resistance is larger than the series of two diode connected load, due to the effect of the second gate over M_5. The total output resistance can be expressed as:

$$R_{OUT} = \frac{1}{g_{m5}}\left[1+\frac{g_{m5}}{g_{m3}}(1+\eta)\right] \tag{10}$$

Since the V_{TG} is negative, η corresponds to the threshold modulation coefficient, which is typically bigger than 2 for this technology. As transistors M3 and M5 are equal, (10) clearly shows that this topology increases the small signal resistance of M3 by a factor of 1+ η.

The technique implemented for biasing this circuit is similar to the one described in section III.A. However, here the complete

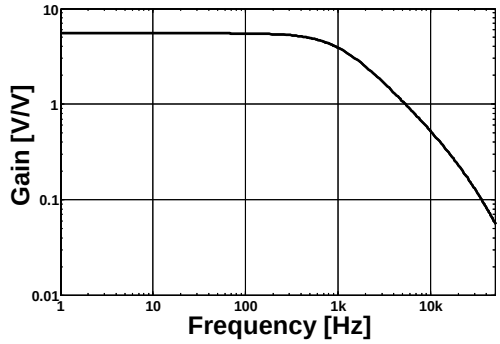

Fig. 10: Frequency response of the circuit in Fig. 6

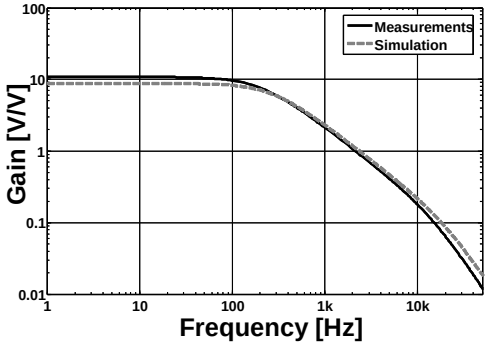

Fig. 12: Frequency response of the circuit in Fig. 7

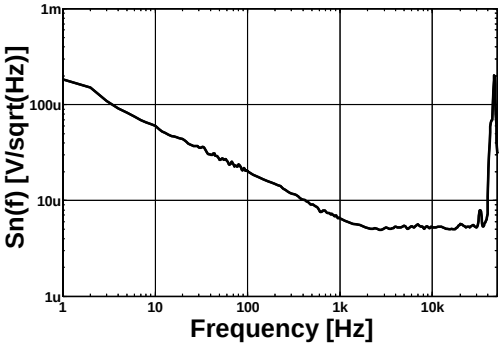

Fig. 11: Input noise spectral density of the circuit in Fig. 6

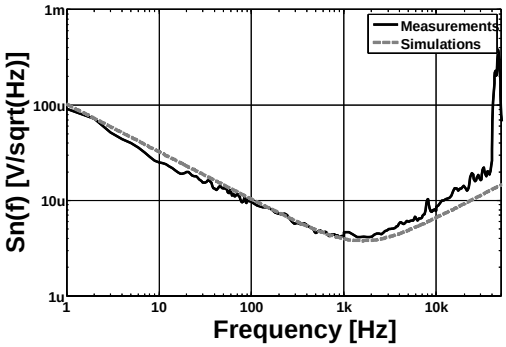

Fig. 13: Input noise spectral density of the circuit in Fig. 7

load circuit is replicated as a tail current source, namely M_7, M_9, M_8, and M_{10}. Also in this circuit S_{13}=S_{14}, and S_{11}=S_{12}, as in section III.A. Therefore, setting the V_{GS} of M_{13} (and thus of M14) and V_{G7} - V_{S9} (and thus V_{G5} - V_{S3}) equal to $V_{CC}/4$ will bring the output bias voltage to half of the supply rail.

C. a-IGZO differential amplifier with positive feedback and enhanced source degenerated load with self-biased top gate

The amplifier presented in this section represents a further improvement in terms of DC gain compared to the topologies discussed previously. The schematic is shown in Fig. 8.

This topology uses the same technique to increase the output resistance as described in section III.B, but adds another double gate diode load, M7, on top the stack, with its second gate connected to the source of M3.

The total output resistance can be expressed in this case as:

$$R_{OUT} = \frac{1}{g_{m7}} + \frac{1}{g_{m5}}(1+\eta) + \frac{1}{g_{m3}}(1+\eta)^2 \qquad (11)$$

(11) shows that the output resistance of M5 is increased by a factor of 1+ η, and the output resistance of M3 is increased by $(1+\eta)^2$, which leads to a remarkable increase in DC gain, compared to the stage presented in III.A.

For this amplifier, the input pair and the bias techniques are the same explained in section III.A and III.B.

IV. Measurement Results

The circuits presented in Section III have been designed and fabricated on foil as described in Section II. The plate contains devices for the characterization of the technology and several test circuits. The transfer and output characteristics of 12 TFTs with widths ranging from 15 µm to 200 µm and lengths ranging from 15 µm to 200 µm have been measured using the Keysight B1500A Semiconductor Parameter Analyser. The results have been used to extract the parameters of the model implemented in the simulator.

The measurement setup for the amplifiers consists of a voltage buffer, connected with probe needles and short coax cables the output of the amplifiers, and an instrumentation amplifier. The output of the instrumentation amplifier is fed into the HP35670A Dynamic Signal Analyser in order to measure the frequency response and output noise. The parasitic capacitance introduced by this setup is about 20 pF, and all measurements use a supply voltage for the amplifiers of ±10 V.

In the following subsections, the measurement results of the different amplifier topologies are reported. In the last subsection the agreement between measurements and circuit simulations is discussed.

A. Differential amplifier with positive feedback

The frequency response and noise spectral density referred to input for the amplifier in Fig. 6 (Section III.A) have been measured, and the results are shown in Fig. 10 and 11. The DC gain is measured to be 5.4 V/V, or 14 dB. The cutoff frequency reaches 2 kHz, due to the internal pole of the amplifier. The output pole is at about 20 kHz.

The noise spectral density clearly shows a flicker behaviour up to the corner frequency of 2 kHz, reaching about 200

$\mu V/Hz^{1/2}$ at 1 Hz, down to 5 $\mu V/Hz^{1/2}$ in the thermal noise region. The integrated equivalent noise at the input is 420 μV_{rms}. The measured current consumption of the gain stage is 2.5 µA.

B. Differential amplifier with positive feedback and source degenerated load with self-biased top gate

The measurements of the amplifier in Fig. 7 (Section III.B), shown in Fig. 12, demonstrate a DC gain of 12 V/V, or 21.5 dB, which is more than a factor two improvement on the previous topology. At the same time, because of the increase in output resistance, the bandwidth decreases to 400 Hz. The output pole, due to the load capacitance, stays at 20 kHz.

The measured noise spectrum is presented in Fig. 13. The noise spectral density at 1 Hz is 100 $\mu V/Hz^{1/2}$, and the total equivalent integrated noise at the input is 195 μV_{rms}.

It is interesting to notice that the graph shows a 1/f behaviour up to 1 kHz, followed by a positive slope in the noise spectral density at higher frequencies. This phenomenon is observed because the main contribution to the noise in the circuit comes from TFTs which are not the input pair. When this happens, the noise transfer function is different from the signal transfer function. For this reason, the spectrum of the input equivalent noise shows a behaviour which is different from the typical 1/f trend at low frequency and white noise at high frequency. In this particular case, as it is demonstrated analyzing the contribution of the different TFTs in an AC noise simulation, the largest contribution to the noise comes from the source degeneration TFTs M3 and M4 (Fig. 7), followed by the input pair.

The current consumption measured for the gain stage is 100nA.

C. Differential amplifier with positive feedback and enhanced source degenerated load with self-biased top gate

In Fig. 14 and 15 are shown the measurements of both the frequency response and input noise spectrum of the circuit in Fig. 8 (Section III.C). The frequency response shows that this circuit has a DC gain which reaches 35 V/V, or 30 dB, and a cutoff frequency of 150 Hz (Fig. 14). The topology adopted for the load gives thus a 16 dB improvement compared to the circuit with diode connected load.

The input noise spectral density is shown in Fig. 15, and the integrated input noise is 146 μV_{rms}. The same behaviour observed in the noise spectral density of Fig. 13 is present in the graph of Fig. 14, because the main contribution to the noise comes from the TFTs M_3 and M_4 in Fig. 8.

The low-frequency noise measurements require seven hours of measurements time, and we could not observe relevant changes of the amplifier performance during this operational time.

Repeating the noise measurements of this amplifier topology after 10 months of shelf life, the gain was found constant at 30dB, but the 3dB bandwidth decreased to 8Hz and the input referred noise increased to 290 µVrms. TFT stack optimization and suitable encapsulation layers are presently actively researched to improve shelf life stability.

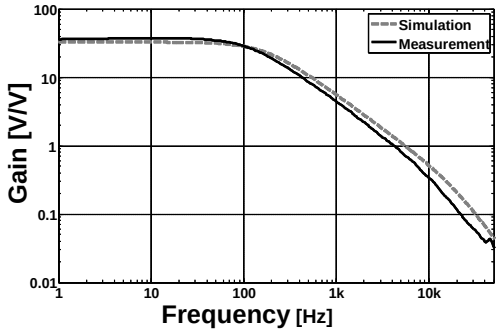

Fig. 14: Frequency response of the circuit in Fig. 8

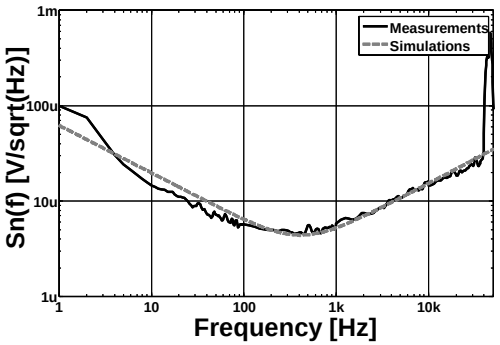

Fig. 15: Noise referred to input of the circuit in Fig. 8

The measured power consumption for the gain stage is 20 nA. It is important to notice that the chosen biasing strategy does not fix the tail currents, and thus circuits with different topologies do have different biasing currents. However, the DC gain of all circuits proposed in Section III is at the first order independent from the bias current, as it is actually determined by the ratio of transcoductances. For this reason we can be sure that the improvements in DC gain are actually achieved thanks to the novel circuit topologies proposed, and are not due to changes in the tail currents.

D. Circuit simulations

The measurements of the circuits described in sections III.A to III.C show very good agreement with the simulation results, which are obtained using the analytical physical-based model described in Section II and the parameter set extracted from the characterization TFTs. In particular, the graphs in Fig. 12 and 13 show that the model describes well the AC behaviour of the circuits.

Fig. 13 and 15 also show a good agreement between input noise spectral density measurements and the AC noise simulations based on the model presented in Section II. A comparison between the topologies presented in this work is given in Table I, while a comparison with previous literature has been given in Table III.

TABLE I
COMPARISON BETWEEN THE TOPOLOGIES PRESENTED IN THIS WORK

	Gain [dB]	BW [Hz]	Unity gain freq. [kHz]	Current cons. [nA]	Input referred noise [V_{rms}]	Noise efficiency factor
III.A	14	2000	4	2500	420 µ	582
III.B	21.5	400	2.5	100	195 µ	120
III.C	30	150	5.5	20	146 µ	66

V. DISCUSSION

A. Circuit results

A major drawback of designing circuits in a-IGZO technology is the lack of a complementary n and p-type devices, which strongly limits the options for circuit topologies, and especially has a detrimental impact on gain. For this reason, the second gate in the source/drain metal layer has been exploited here in order to design nonconventional topologies targeting high DC gain in single stage amplifiers. As the measurements show, the circuits in III.B and III.C reach a gain above 20dB, which allows relaxing the noise requirements of the following stages. It is worth mentioning that high gain unipolar topologies based on loads in zero-V_{GS} configuration are not suitable to our technology, since the value of the threshold voltage is always above zero, and thus bias currents would become too low to guarantee any useful bandwidth.

The poor speed performance obtained compared to silicon devices is due to the low mobility offered by a-IGZO, which is at least two orders of magnitude lower than crystalline silicon, and to the high value of parasitic capacitances in the non self-aligned TFT devices offered by our technology.

As discussed in Sections IV.B and IV.C, the noise performance in the proposed amplifiers is mainly influenced by TFTs in the load circuits. This means that there is still margin to improve the noise performance of these gain stages.

It is interesting to notice that in current literature on low frequency noise in a-IGZO TFTs, a dependence of the input-referred flicker noise on the bias current has been noticed [30]. However, a difference of just a factor 4 can be observed between the low-frequency noise densities in Fig. 11 and 15, while the bias current in these two circuits differs by almost two orders of magnitude. Deriving the input referred flicker noise from (6) and using the simplified current model in (4) the input flicker noise for a single TFT can be written as:

$$S_{n,in}(f) = \frac{2\alpha_H q}{C_i \gamma^2 W^{\frac{\gamma+1}{\gamma}} L^{\frac{\gamma-1}{\gamma}} f} \sqrt[\gamma]{\frac{I_D}{\beta}} \tag{12}$$

The γ parameter obtained from parameter extraction is 3.3, thus scaling the current by 2 orders of magnitude should result in a decrease in PSD only by a factor of 7. Therefore, even if a dependency of the 1/f noise from the bias point exists, reducing the current to decrease low frequency noise is not a very effective strategy. Standard approaches such as increasing the area of the devices will be much more effective and can be used to further improve the noise level in the amplifiers proposed in this work.

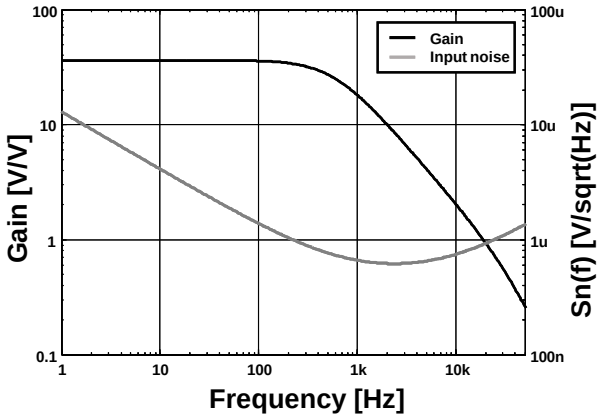

Fig. 16: Simulation results of gain and input noise spectral density for the amplifier described in III.C, optimized for improved noise performances.

TABLE II
WIDTH AND LENGTH OF THE TFTS IN TOPOLOGY III.C, BEFORE AND AFTER OPTIMIZATION.

TFT	W/L [µm/µm] before optimization	W/L [µm/µm] after optimization
M1, 2	400/30	2000/30
M3, 4, 13, 14	15/15	100/100
M5,6,7,8,9,10,11,12	30/30	120/100

B. Application perspective

The characteristics of flexibility and large area coverage, make our technology suitable for medical applications in which the acquisition of bio-potential on a surface is helpful or necessary. One example is described by Rabotti et al. in [1], where a matrix of passive electrodes is used to acquire electro EHG signals. These signals are used to monitor the uterine action potential conduction velocity, in order to predict preterm labour of pregnant women. The system uses at a moment a matrix of passive electrodes and a large number of discrete bio-potential amplifiers, resulting in an obtrusive and unpractical solution. A matrix of electrodes on foils with embedded a-IGZO TFT bio-potential amplifiers would be an excellent approach to ensure wearability and comfort of use in this application. In [1] it has been shown that it is possible to extract conduction velocity with very good accuracy from signals having an SNR of 5.88 dB. Here the SNR is expressed as:

$$SNR = \frac{V_{sign,pp}}{2\sqrt{2}V_{n,rms}} \tag{13}$$

The amplitude of the EHG signal is typically more than 500 µVpp in a 10 Hz bandwidth: the requirement for a front end to meet the target SNR is thus an input noise of 90 μV_{rms}. The best of the presented amplifiers reaches 125 μV_{rms}, input noise in 10Hz band, therefore the target SNR demanded by EHG seems at reach. Indeed, Fig. 16 shows the simulation of gain and input noise for the amplifier topology presented in III.C, after some further optimization in the transistor dimensions to

TABLE III
PERFORMANCE COMPARISON

	Gain [dB]	BW [kHz]	Unity gain freq. [kHz]	Power cons. [µW]		Nr. of stages
[10]	22.5	5.6	31	160		3
[11]	19	25	330	6760		2
[12]	25	220	3900	2320		2
[13]	34	5	N.A.	570		1
[14]	18.7	108	427	0.9		3
[15]	24.5	6	32	N.A.		3
[28]	19.9	0.25	2.5	N.A.		1
This work	30	0.15	5.5	0.4*	188.4**	1

Power consumption for a 20V supply voltage: *including only the gain stage; ** including the gain stage and the output buffer, which was designed to drive an off-chip load of 20pF.

decrease the input noise. This amplifier shows an input noise of 20 μV_{rms} in the EHG band, with a current consumption in the gain stage of 32 nA, and thus is sufficiently low-noise for EHG measurements. Besides, if chopping is used to decrease the influence of 1/f noise on the amplification chain, applying a chopping frequency of only 30 Hz to the amplifier presented in Section III.C will already be sufficient to meet the SNR required for EHG measurements.

Another case study which is worth mentioning is Heart Rate (HR) monitoring during physical activities, described in [32]. In this kind of wearable application, the use of a flexible electronic frontend could be a very interesting option, for its potential of decreasing motion artefacts. The authors of [32] use a Doubechies orthonormal wavelet to improve the detection rate of R-spikes present in the ECG signal. The algorithm is evaluated by analysing real signals with different SNR, from 36 dB to 6 dB, and the results show a correct detection rate of 94.8% on signals with 6 dB of SNR.

Considering the amplitude of R-waves, which is typically larger than 1 mV_{pp} in a 100 Hz bandwidth, the input noise in band can be as high as 177 μV_{rms}. This is larger than the input noise measured for the amplifier presented in section III.C. Therefore, we can say that our best amplifiers are already suitable for HR detection in the presence of typical signal amplitudes.

Finally, the noise performance required for medical diagnosis on ECG [33] is less than 30 μV_{rms} integrated noise in a 150 Hz band, which means that none of the amplifiers we measured meets this requirement. However, the noise-optimized amplifier simulated in Fig. 16 has an input equivalent noise in the ECG band of 29.5 μV_{rms} and thus would be suitable, from the SNR perspective, to perform medical-grade ECG measurements, even without chopping

VI. CONCLUSION

In this paper different topologies of high-gain single stage a-IGZO amplifiers have been presented, together with their dynamic measurement and, for the first time in literature, their experimental noise characterization. As a first result, the novel amplifier topologies shown in this paper improve the DC gain compared to single-stage a-IGZO amplifiers previously presented in literature. Table II shows TFT dimentions before and after optimization. Secondly, the value of the Hooge parameter α_H extracted by low frequency noise circuit measurements is in agreement with previous literature results available for a-IGZO TFTs. Finally a very good agreement has been achieved between circuit simulations of noise and AC dynamics of the amplifiers circuits and the corresponding measurements. The experimental characterization shows that the proposed amplifier which achieves the best integrated input noise can be used for HR detection in typical cases. Furthermore, simulations demonstrate that with an improved design, both EHG measurements and medical grade ECG acquisition can be performed using an a-IGZO front-end. The integration of ultra-lightweight electrodes and front-end amplifiers on a foil in adhesion with the skin appears thus as a promising innovative route to build systems for the measurement of bio-potentials distributed on the body surface with the ability to ensure high immunity from motion artefacts.

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