New phenomena in halfmicron isolation technology

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New phenomena in Halfmicron Isolation technology

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under supervision of:

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Abstract

Reducing the spacing between active devices is one way of improving the packing density of CMOS integrated circuits. This implies reduction of the dimensions of the field oxide, used to isolate active devices. This report deals with new phenomena, which occur at reducing the oxide width to values in the order of 0.5μm. 2- and 3-dimensional simulation programs have been used to study these phenomena.

Using the modified LOCOS technology, a 2-dimensional effect called the over-all corner effect is found. At a LOCOS width of 0.7μm, this effect reduces the depletion width at the oxide-silicon boundary, which causes the parasitic current to decrease.

3-dimensional simulations were carried out for an isolation technology called BOX, in order to investigate the influence of the so-called side-wall inversion. For oxide widths in the order of 0.5μm, this 3-dimensional effect has a considerable influence on the characteristics of a MOST in the neighbourhood of the inverted side-wall.

Preface

This report deals with the project concluding my study at the department of Electrical Engineering of the Eindhoven University of Technology. The graduate work has been carried out at the Philips Research Laboratories Eindhoven from october 1986 until august 1987.

My special appreciation goes to my coach, Ir. P.A. van der Plas, for many useful and encouraging suggestions and discussions, and the reviewing of this report. I would like to thank him for the support he has given me during the project.

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Finally, I would like to thank Ing. R. Petterson for the helping hand he has offered me with the computer problems I had to deal with.

Sjef Kisters, august 1987

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Chapter 1

Introduction

Mainly because of its low power consumption, CMOS technology has become the mainline VLSI technology. In CMOS n- and p-channel transistors are integrated in the same device. Starting off with a p-type substrate, n-channel transistors are easily made. To create an n-type environment for the p-channel transistor, an n-type area called the *n-well* is constructed. Figure 1.1 shows a cross-section of the CMOS-structure with its basic elements.

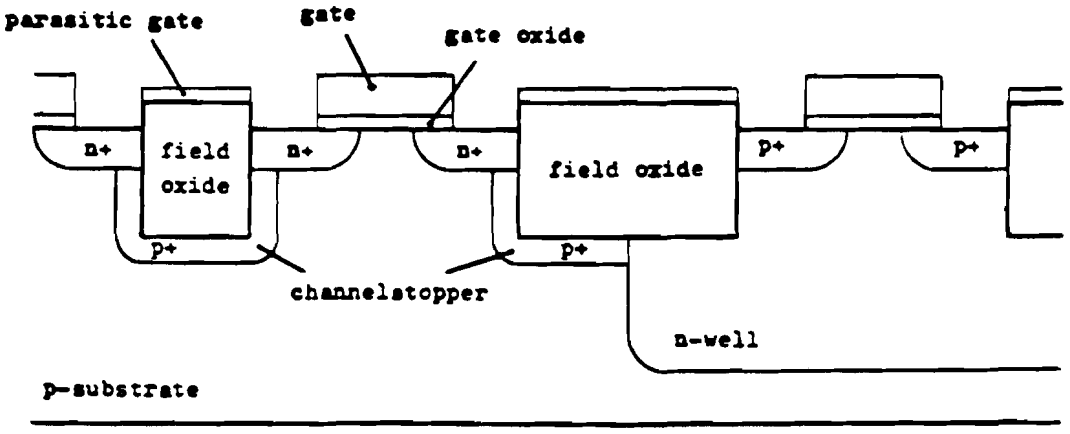

Figure 1.1: *The basic CMOS structure*

To separate the transistors integrated in the device electrically, isolation is needed. The principle of isolation is relatively simple: a thick oxide film (the so-called *field oxide*) and a high dopant concentration under this oxide (the so-called *channelstopper*) will increase the threshold voltage in order to avoid inversion in the isolation area, thus isolating the devices electrically.

Figure 1.1 demonstrates that the isolation structure can be seen as a *parasitic transistor*. The parasitic gate is formed by a polysilicon or metal interconnection and the field oxide corresponds to the parasitic gate oxide.

One way of improving the packing density is reducing the spacing between active devices. In [ref1], a new field oxide, based on the LOCOS technology, is presented. Spijkers [ref2] used this modified LOCOS technology to examine the influence of reducing the width of the field oxide on the performance of the isolation structure. In that report, n- to n-channel, p- to p-channel and n- to p-channel spacings have been examined.

In this report new phenomena at even smaller dimensions have been studied. Therefore, using modified LOCOS technology, the n- to n-channel parasitic transistor has been simulated in order to investigate 2-dimensional effects. For these simulations, a 2-dimensional simulation program called SEMMY was used. Furthermore, simulations were done to study a 3-dimensional phenomenon. For these simulations, the 3-dimensional simulation program TRIPOS was used. To facilitate simulations with TRIPOS, BOX was used for isolation because of its rectangular shape.

Chapter 2

Device Isolation by LOCOS

2.1 The Isolation Structure

Because of its simplicity, Local Oxidation of Silicon (LOCOS) is the universal isolation technique for IC fabrication. This technique is based on the fact that silicon nitride can be used to mask the underlying silicon against oxidation. Using a nitride mask, it is possible to oxidize the silicon in selected regions. During the oxidation, silicon-dioxide grows in the area not protected by the nitride, which can be seen in figure 2.1. This figure also shows the implant of the channelstopper, which takes place before the growing of the field oxide. The implant of the channelstopper can be done after the oxide pad is removed at the selected regions.

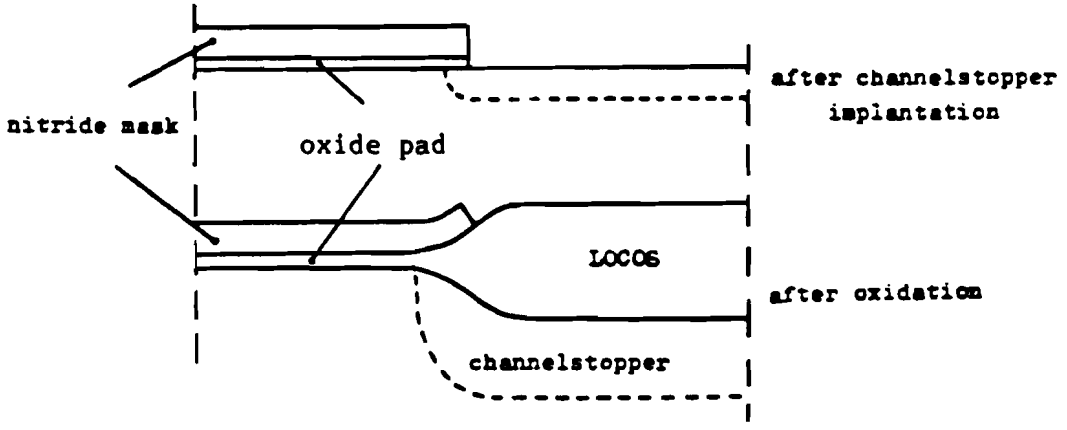

Figure 2.1: *The LOCOS structure*

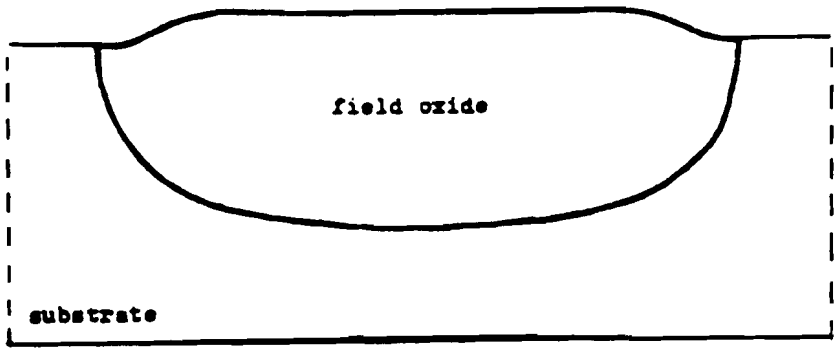

Figure 2.2: *Modified LOCOS*

Figure 2.1 shows two of the mayor disadvantages of the LOCOS technology: oxide enchroachement under the nitride mask (the so-called bird's beak formation), and lateral diffusion of the channelstop implant. These effects become very important when device dimensions are reduced.

In [ref1] an improved version of LOCOS is presented. This modified LOCOS leads to an almost bird's beak free structure, which is shown in figure 2.2. To avoid the lateral diffusion of the channelstopper, retrograde-well technology is used. The channelstopper is implanted after field oxidation by a high energy ion implantation. Because the stopping power of silicon-dioxide nearly equals the stopping power of silicon, the dashed line in figure 2.3 gives the site of the maximum concentration of the well-implant. The retrograde-well process results in a well defined and effective channelstopper, which is self-aligned to the active area.

For future channel lenghts of about 0.5μm, the oxide width is chosen to be 0.7μm. With the described new isolation process, the maximum oxide thickness will then be 0.5μm.

2.2 The Simulated Structure

From a SEM-picture, the shape of the 0.7μm wide LOCOS-structure is determined to be as shown in figure 2.4. The two n^+ - regions, together with the parasitic gate, form a parasitic field transistor which is used for investigation of the electrical performance of the isolation. For convenience, the p-substrate in figure 2.4 is assumed to have a constant doping concentration. In practice, this value will be the doping concentration of the p^+ - channelstopper at the oxide-silicon boundary.

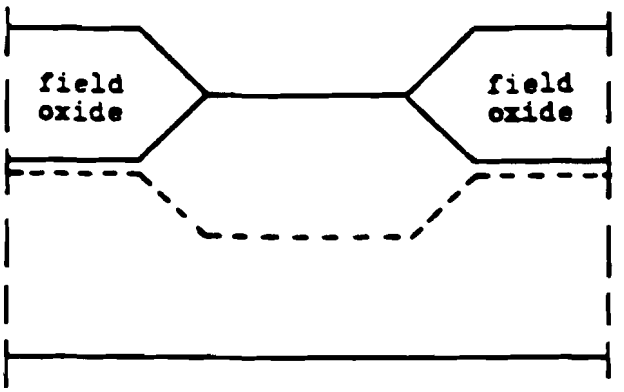

Figure 2.3: *Location of the topdope after the high energy ion implantation*

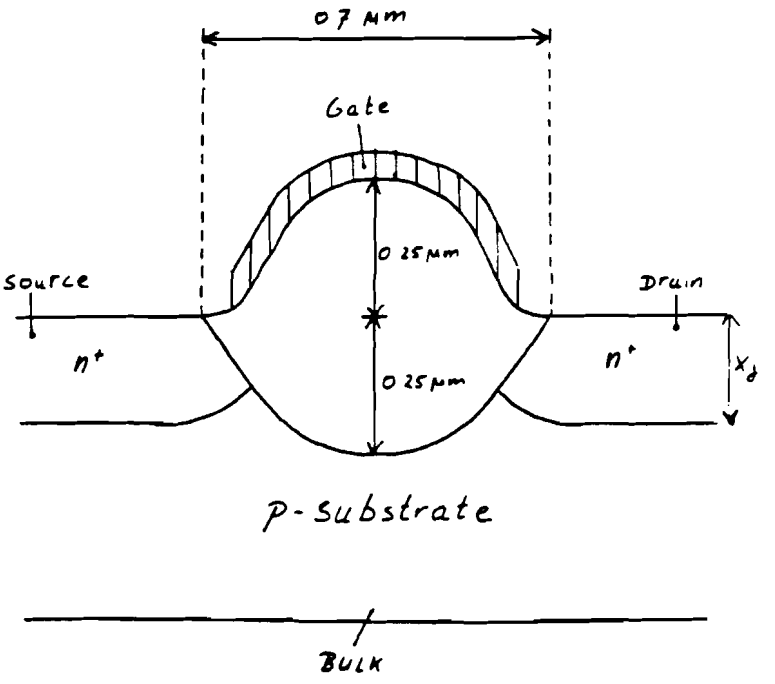

Figure 2.4: *Approximation of the LOCOS structure*

The diffused source and drain of the parasitic transistor are assumed to have a doping profile which can be modelled by a Gaussian function in the y-direction and a double error function in the x-direction [ref3]:

$$N_{x,y} = \frac{N_{top}}{2}[exp(-\frac{y^2}{C^2})][erf(\frac{x - x_L}{C}) - erf(\frac{x - x_R}{C})] \qquad (2.1)$$

where x_L and x_R are the left and right mask edges, N_{top} is the maximum doping concentration, which is chosen to be $1 \times 10^{20} cm^{-3}$. C is a constant related to the diffusion coefficient.

2.3 Simulation Set-up

To limit the number of parameters to be varied, the maximum allowable parasitic current has been set to 10^{-11} A/cm.

The future reduction of active spacing will increase short-channel effects such as punch-through and hot carrier injection, which must be suppressed. One way of achieving this is reduction of the supply voltage. Therefore, the supply voltage is set to 3.3V, which will probably be the new standard for CMOS. For worst case simulations, we choose the maximum voltage to be 3.3V + 10% = 3.6V.

In order to obtain information about the performance of the structure shown in figure 2.4, the following electrical phenomena will have to be investigated:

Subthreshold behaviour Because the parasitic current has to be small at the maximum gate and drain voltage, the device is acting in subthreshold region; the corresponding drain current is called the subthreshold current. In this region the relationship between $ln(I_d)$ and V_g approaches a straight line. The subthreshold slope is defined by:

$$S \equiv (ln10)\frac{dV_g}{d(lnI_d)} \simeq \frac{kT}{q}(ln10)(1 + \frac{C_d}{C_{ox}}) \qquad (2.2)$$

where V_g denotes the gate voltage, I_d the drain current, C_d the depletion capacitance and C_{ox} the oxide capacitance.

Punch-through behaviour Reducing the field oxide width decreases the distance between the depletion layers at source and drain. The potential barrier between source and drain will be reduced, causing the parasitic current to increase. This effect is called lateral punch-through. Figure 2.5 illustrates the barrier lowering at decreasing field oxide width. The presence of this effect must be avoided, which means a limiting factor in the reduction of the field oxide width.

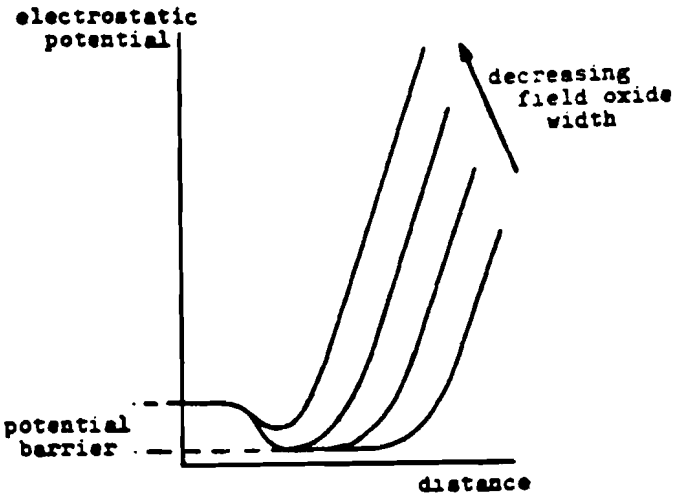

Figure 2.5: *Reduction of the potential barrier at decreasing field oxide width*

2.4 The 2-D Simulation Program

The simulations on the structure of figure 2.4, are done with the program package SEMMY.

SEMMY uses the finite elements method to calculate the solution of 2-dimensional potential problems in reverse biased semiconductors, see [ref4]. SEMMY cannot calculate currents in a device, but is currently the only program available that can simulate structures with slant lines or rounded shapes.

To calculate currents a special subroutine called INSEM has been used. With this subroutine small currents, such as punch-through currents, can be calculated from the SEMMY potential output.

2.4.1 Fundamental equations

It is assumed that in reverse biased semiconductors the currents are too small to influence the space charge and therefore the electrostatic potential in the device. In that case the continuity equations are eliminated and only the Poisson equation has to be solved:

$$divgrad(\Psi) = -\frac{\rho}{\varepsilon} \tag{2.3}$$

with:

Ψ = the electrostatic potential

ρ = the space charge density

ϵ = the permittivity

The space charge density is given by:

$$\rho = q(p - n + N_d - N_a) \tag{2.4}$$

with:

p = the hole density

n = the electron density

N_a = the acceptor doping concentration

N_d = the donor doping concentration

Bolzmann statistics are assumed for the hole and electron densities, so:

$$p = n_i exp(\frac{q(\phi_p - \Psi)}{kT}) \tag{2.5}$$

and:

$$n = n_i exp(\frac{q(\Psi - \phi_n)}{kT} \tag{2.6}$$

with:

n_i = the intrinsic carrier concentration

ϕ_p = the Fermi potential for holes

ϕ_n = the Fermi potential for electrons

Equations (2.3), (2.4), (2.5) and (2.6) together with the boundary conditions uniquely define the potential distribution in an off-state device.

For contacts equipotential lines are used. Assuming charge neutrality at these equipotential lines, the electrostatic potential along the contacts is (see [ref5]):

$$\Psi_n = \phi_n + \frac{kT}{q} ln(\frac{N_d}{n_i}) \tag{2.7}$$

for an n-region contact and for a p-region contact:

$$\Psi_p = \phi_p - \frac{kT}{q} ln(\frac{N_a}{n_i}) \tag{2.8}$$

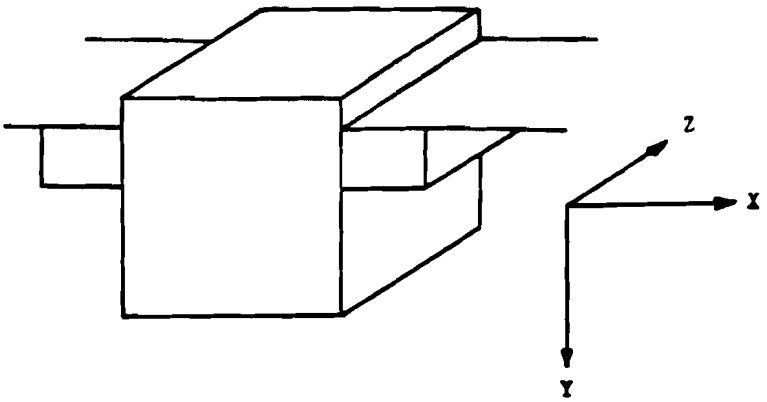

Figure 2.6: *Axis definition*

2.4.2 Calculating the parasitic current

Calculation of the electron current density

In [ref2] the subroutine INSEM, used to calculate parasitic currents, is described. The following expression for the electron current density between point A with Fermi-potential ϕ_{FA} and point B with Fermi-potential ϕ_{FB} is derived:

$$J_n = \frac{n_i(exp(\frac{-q\phi_{FB}}{kT}) - exp(\frac{-q\phi_{FA}}{kT}))}{\int_A^B \frac{1}{qD_n} exp(\frac{-q\Psi}{kT}) dr} \tag{2.9}$$

Calculation of the net electron current

Equation (2.9) is a current density expression. Therefore additional data is needed to derive the net electron current:

- the location of the current path
- the 'area' occupied by the current path

Figure 2.6 illustrates the definition of the axis used in INSEM. Because SEMMY is a 2-dimensional simulation program, there is no z-dimension and the electron current is determined in A/cm. The location of a current path is simply along a line of local maxima in the potential distribution.

The current density along the potential maxima is known from equation (2.9). But, the current will spread over a wider area with a decreasing density. Figure 2.7 shows a possible form of the potential distibution along the y-axis to illustrate this.

The calculation is as follows. The boundaries y_{bor1} and y_{bor2} are determined with a given voltage ΔV. The value of ΔV is chosen to match with

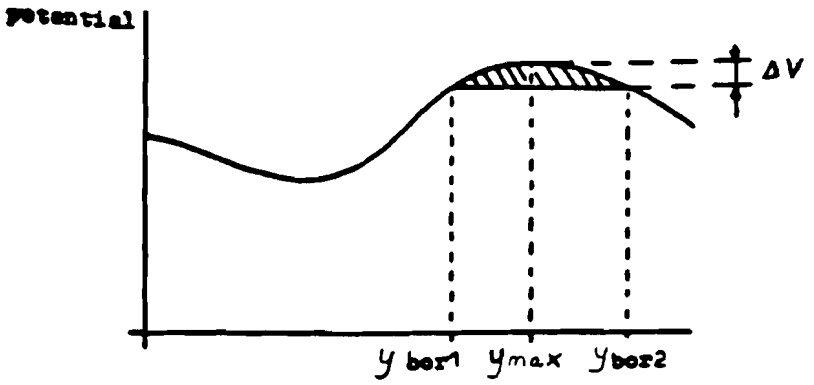

Figure 2.7: *Potential distribution along the y-axis*

the point in the potential distribution where the contribution to the current is reduced to 1 percent of the current at y_{max}. The electron concentrations determine the current densities, so an integration is carried out over the ratio of these electron concentrations:

$$'area' = \int_{y_{bor1}}^{y_{bor2}} \frac{exp(\frac{-q\Psi}{kT})}{exp(\frac{-q\Psi_{max}}{kT})} dy \tag{2.10}$$

The total electron current would be determined by multiplying equations (2.9) and (2.10). But in general the current path is not perpendicular to the integration axis (=y-axis). So the total electron current is the multiplication of (2.9), (2.10) and a factor $sin(\beta)$, where β is the angle between the current path and the integration axis.

2.5 Simulations and Results

2.5.1 Influence of the backgrounddope

Figure 2.8 shows the parasitic current as a function of the backgrounddope for a junction depth at source and drain of 0.2μm.

For values of the backgrounddope below $5 \times 10^{16} cm^{-3}$ an almost exponential relation between the backgrounddope and the parasitic current can be seen, caused by lateral punch-through. Figure 2.9 illustrates the presence of punch-through for low values of the backgrounddope, with a plot of the potential distribution in the parasitic channel, underlying the results of figure 2.8. It is clear that reduction of the doping concentration leads to a considerable barrier lowering, indicating punch-through.

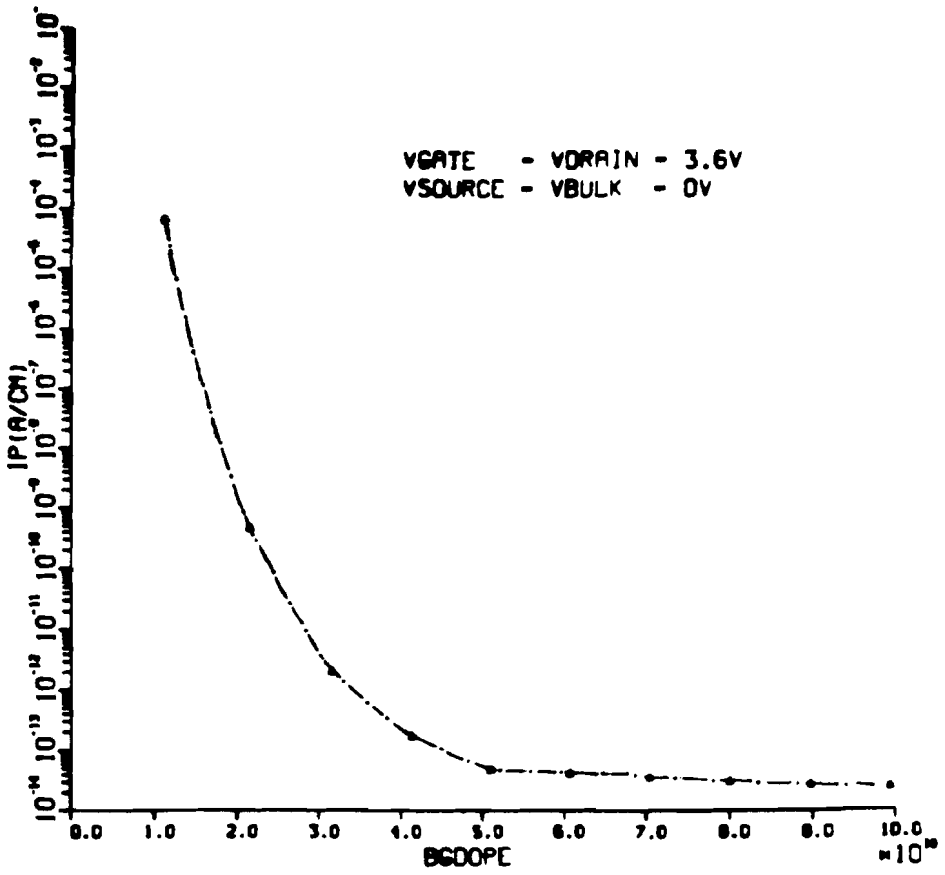

Figure 2.8: *Parasitic current as a function of the backgrounddope*

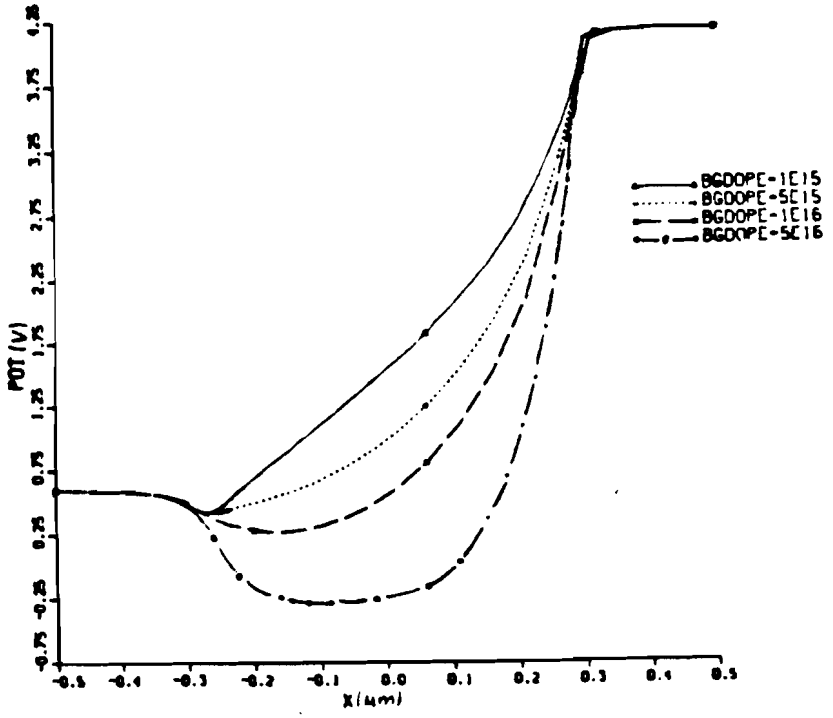

Figure 2.9: *Influence of the backgrounddope on the electrostatic potential at the oxide-silicon boundary*

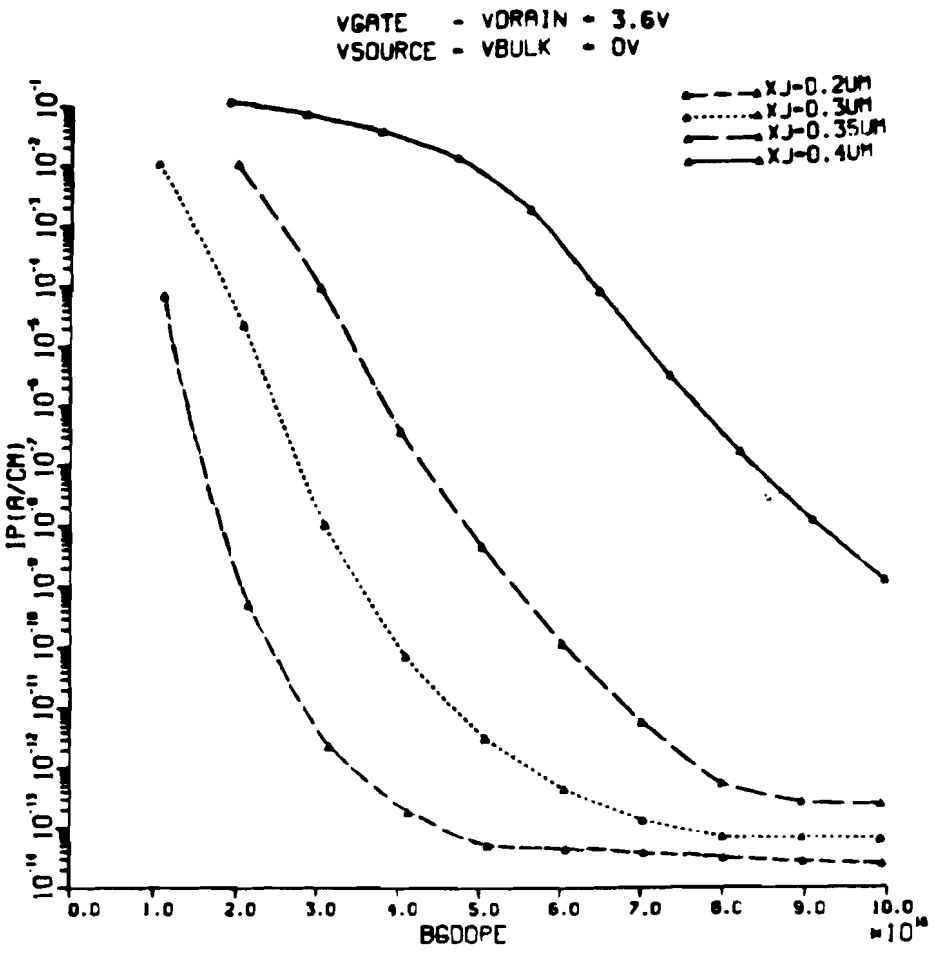

Figure 2.10: *Influence of the junction depth on the parasitic current*

For higher values of the backgrounddope, figure 2.8 shows an almost constant parasitic current, caused by weak inversion of the silicon surface. It is advantageous to choose the value of the backgrounddope at this part of the curve, not only because the parasitic current is then kept below the allowable maximum, but also because then variations in the backgrounddope will not affect the value of the parasitic current.

Conclusion For a junction depth of $0.2\mu m$, the value of the backgrounddope has to be above $5 \times 10^{16} cm^{-3}$.

2.5.2 Influence of the junction depth

Figure 2.10 shows the parasitic current as a function of the backgrounddope for various values of the junction depth.

It can be seen that, for values below $5 \times 10^{16} cm^{-3}$, increasing the junction depth from $0.2\mu m$ to 0.3, 0.35 and $0.4\mu m$ leads to an enormous increase of the parasitic current. This can be explained by the fact that increasing the

junction depth leads to a reduction of the effective $n^+ - n^+$ spacing, causing lateral punch-through. In addition to this effect, the influence of the corner-effect, which will be explained in chapter 3, diminishes at increasing junction depths. This also causes the parasitic current to increase.

Figure 2.10 also shows a problem all simulation programs for reverse biased semiconductors have: at a junction depth of 0.4μm, the depletion regions at source and drain start to approach each other. In this case, the splitting of the quasi-fermi levels, see section 2.4, is not obvious and therefore difficult to determine. This causes the potential distribution to become less dependent of the backgrounddope for low values of that dope, leading to an almost constant parasitic current.

Conclusion Using junction depths of 0.3μm and 0.35μm, the backgrounddope has to be above respectively $7 \times 10^{16} cm^{-3}$ and $1 \times 10^{17} cm^{-3}$, whereas higher values of the junction depths need even higher values of the backgrounddope to prevent punch-through and reduce the parasitic current.

2.5.3 Influence of the oxide thickness

The influence of reducing the oxide thickness is given in figure 2.11. It is obvious that reducing the oxide thickness from 0.5μm to 0.4μm hardly affects the value of the parasitic current. This is remarkable, since previous results, see [ref2], did show a greater dependence on the field oxide thickness.

2.5.4 Subthreshold behaviour

Figure 2.12 shows the subthreshold curve at a backgrounddope of $5 \times 10^{16} cm^{-3}$. An arbitrary threshold voltage is defined as the gate voltage for which the parasitic current has a value of 10^{-6} A/cm. The threshold voltage is found to have a value of about 16V in case of a drain voltage of 0.1V, and 12.5V at a drain voltage of 5V. These values ensure that, even in worst case situations, inversion will be avoided in the field isolation region.

The following values of the subthreshold slope are obtained from figure 2.10:

$$S_{V_{drain}=0.1V} = 1.32\text{V/decade.}$$

$$S_{V_{drain}=5.0V} = 1.12\text{V/decade.}$$

Normally, the subthreshold slope is hardly influenced by the applied drain voltage, but in this case the depletion width at the oxide-silicon boundary is influenced by the depletion region at the drain junction, because of the very small $n^+ - n^+$ spacing. This effect is shown in figure 2.13, which gives an equipotential plot for both situations.

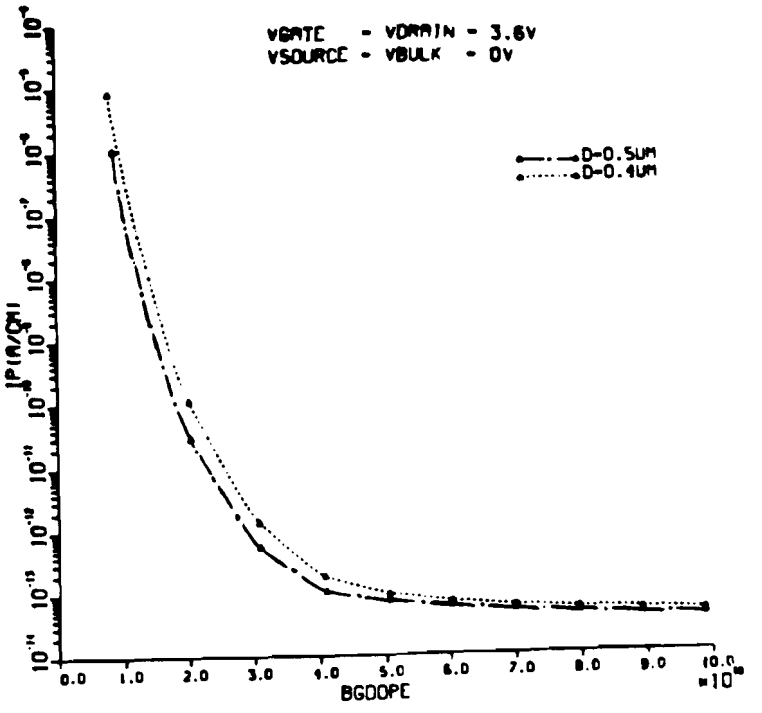

Figure 2.11: *Influence of the oxide thickness on the parasitic current*

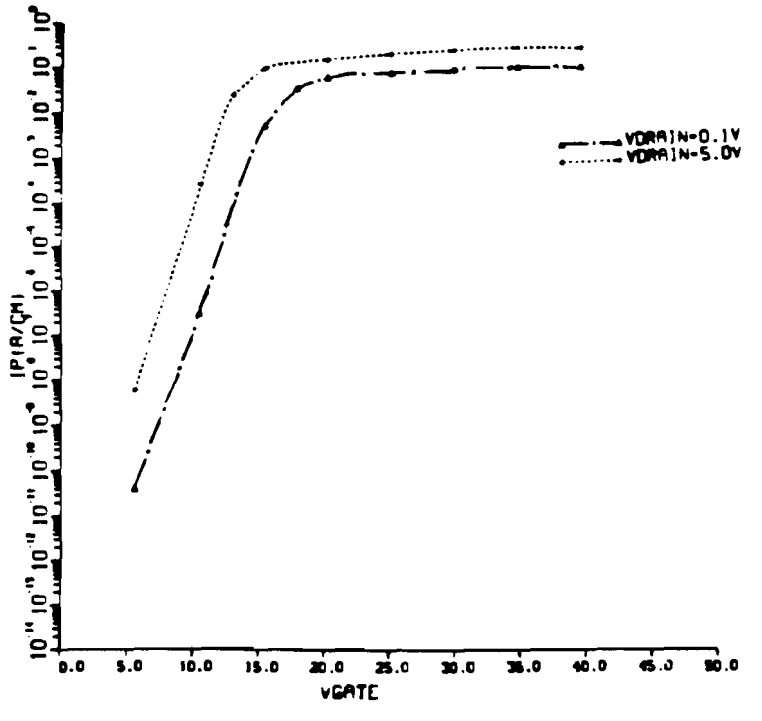

Figure 2.12: *The subthreshold curve of the parasitic transistor*

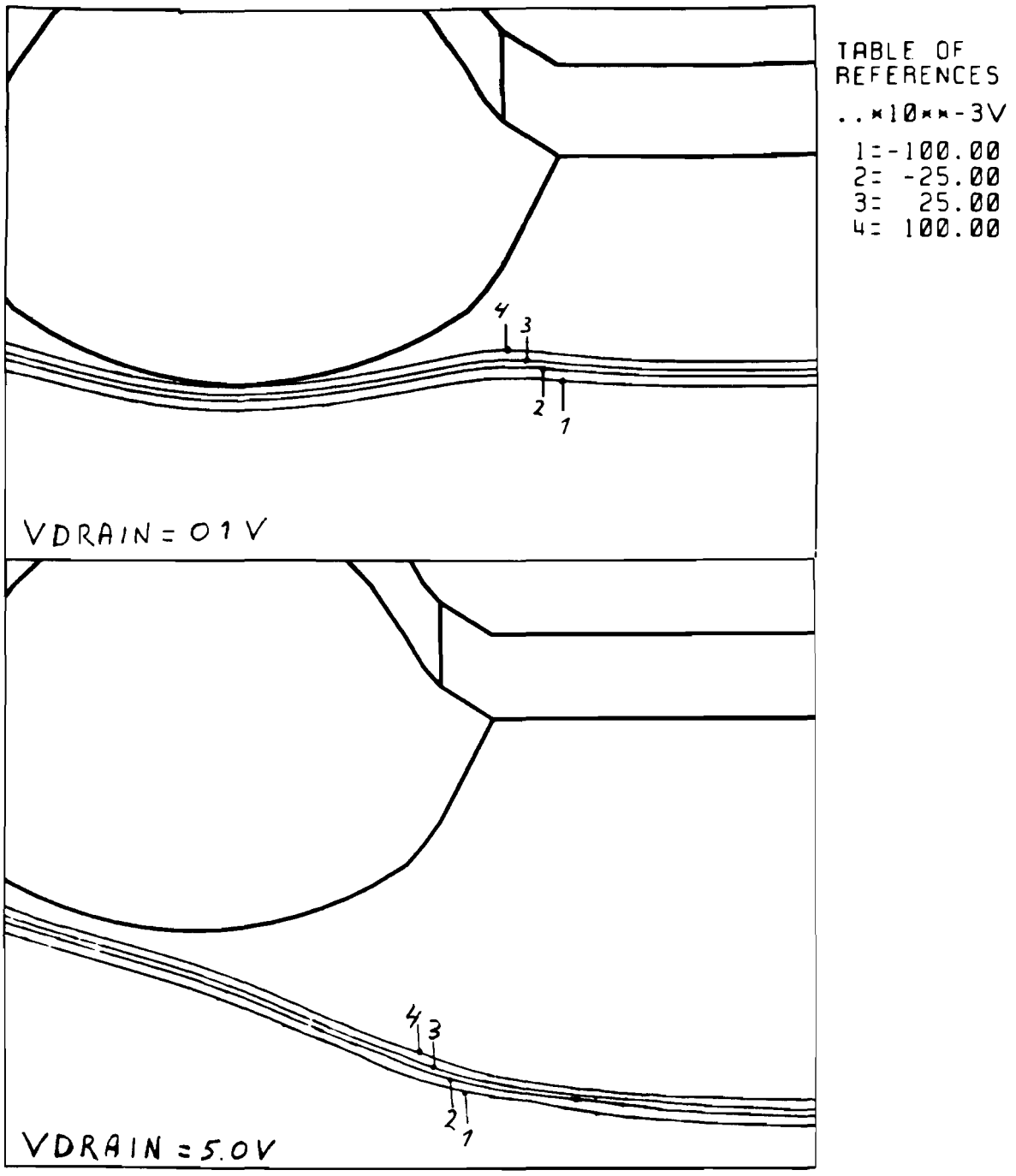

Figure 2.13: *The influence of the drain voltage on the depletion width*

It can be seen that in case of a drain voltage of 5V, the depletion layer under the gate oxide will be wider than in case of a drain voltage of 0.1V. This causes the depletion capacitance to decrease and, according to equation (2.2), we see that the subthreshold slope will be lower.

Chapter 3

The Effective Oxide Thickness

3.1 Introduction

In order to obtain more information about the performance of the LOCOS-isolation, it is interesting to investigate how thick the gate oxide of a normal MOST would have to be to obtain the same electrical properties as the LOCOS-structure. Thus, an effective oxide thickness of the LOCOS can be defined, as illustrated in figure 3.1.

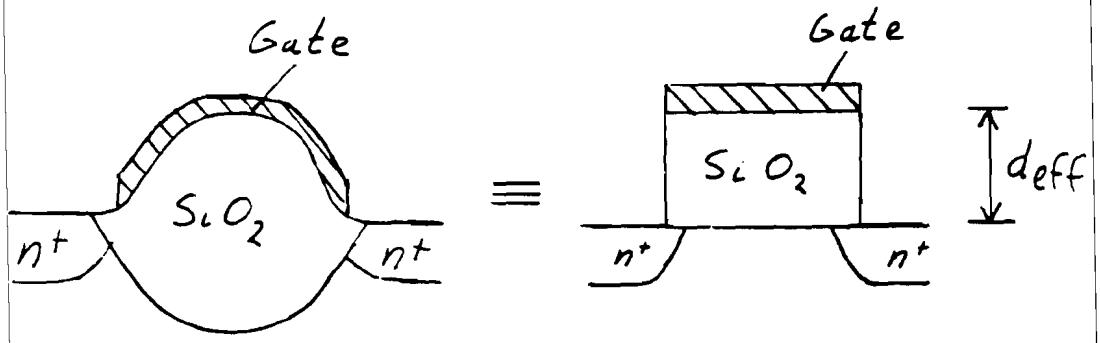

Figure 3.1: *Definition of the effective oxide thickness*

Since the thickness of the LOCOS varies from 0 to 0.5μm, the effective oxide thickness is expected to lie between these values.

3.2 Calculation of the Effective Oxide Thickness

In [ref2] a theory for calculating the subthreshold slope is described. Using this theory leads to the following expression for the subthreshold slope:

$$S = \frac{kT}{q}[ln10][1 + \frac{C_D}{C_{ox}}[1 - (\frac{2}{a^2})(\frac{C_D}{C_{ox}})]] \tag{3.1}$$

The oxide capacitance per unit area is defined as:

$$C_{ox} = \frac{\varepsilon_{ox}}{d} \tag{3.2}$$

where d denotes the oxide thickness. The depletion capacitance per unit area is defined as:

$$C_D = \frac{\varepsilon_{si}}{D} \tag{3.3}$$

where D denotes the depletion width at the oxide-silicon boundary. Furthermore

$$a = \sqrt{2}(\frac{\varepsilon_{si}}{\varepsilon_{ox}})(\frac{d}{L_D}) \tag{3.4}$$

where L_D denotes the Debye length.

Knowing the value of the subthreshold slope from the simulations, and taking

$$C_{ox} = \frac{\varepsilon_{ox}}{d_{eff}} \tag{3.5}$$

the effective oxide width can be calculated. In chapter 2 the value of the subthreshold slope for a backgrounddope of $5 \times 10^{16} cm^{-3}$ and V_{drain} equal to 0.1V was found to be 1.32 V/dec. Using the method described above, the following value for the effective oxide thickness is found:

$$d_{eff} = 0.55\mu m$$

This is a remarkable result, since this value is even higher than the maximum oxide thickness of the LOCOS. From equation (3.3), it is found that an explanation of this effect could be a wrong value for the depletion capacitance. A lower value for the depletion width D would decrease the oxide thickness d.

3.3 The over-all Corner Effect

At reduced field oxide widths, used to isolate transistors with channel lengths in the order of $1\mu m$, 2-dimensional effects have to be considered. One of these effects is the so-called corner effect [ref6]. This effect leads to a smaller

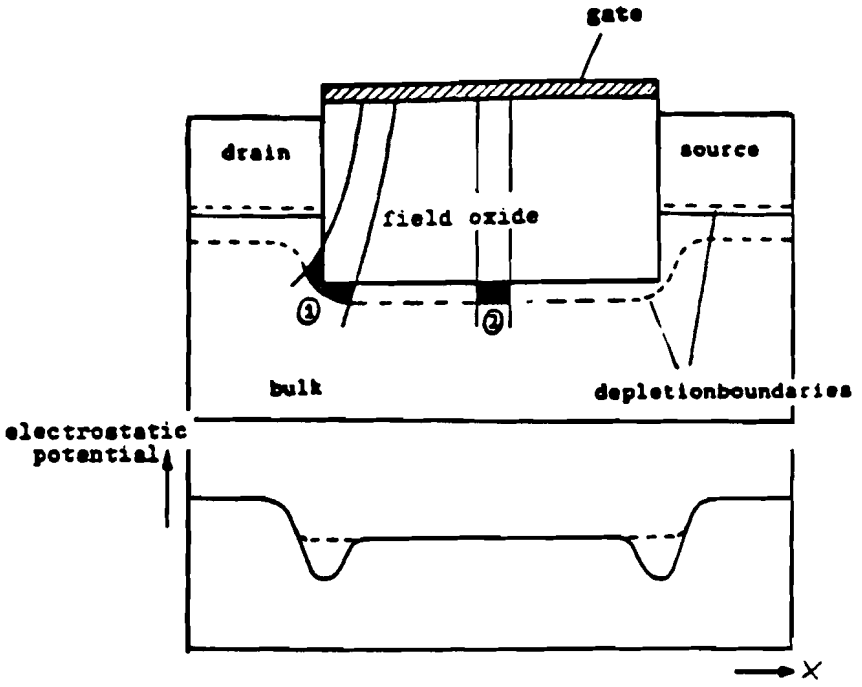

Figure 3.2: *Demonstration of the corner effect*

depletion width at sharp corners of the oxide. This is illustrated in figure 3.2.

The boundaries of the two shaded areas in figure 3.2 consist of the oxide-silicon boundary, the depletion boundary and two electric field lines. The distance between the field lines in both situations is chosen in such a way that the enclosed surface charge on the gate is the same in both situations. Therefore the charge enclosed by area 1 ($Q1$) is equal to the charge enclosed by area 2 ($Q2$). Because of the spreading of the electric field lines, the depletion boundary has to be closer to the oxide in situation 1 in order to fulfil the charge equilibrium criterion ($Q1 = Q2$). Because the depletion width is smaller at the corners, the potential is reduced at these corners.

In our situation the field oxide has no sharp corners, but the strong bending of the LOCOS could cause the electric field lines to spread out along the whole oxide-silicon boundary, thus reducing the depletion width along the whole oxide boundary, which explains the high value which was found for the effective oxide thickness in the previous section.

Because the influence of this effect concerns the whole LOCOS-silicon boundary, it can be called the 'over-all' corner effect. In order to illustrate this effect, several specific simulations were done.

3.3.1 The influence of the oxide width

According to the previous discussion, making the oxide width larger than 0.7μm should lead to a wider depletion region at the oxide-silicon boundary

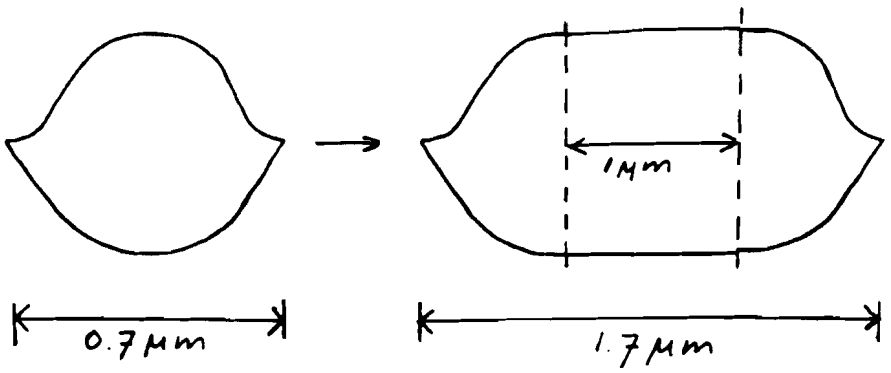

Figure 3.3: *Making a wider field oxide*

and therefore a lower value of the threshold voltage and the subthreshold slope is expected. In order to check these effects, a rectangular piece of oxide with a lenght of 1.0μm and thickness 0.5μm was inserted in the middle of the LOCOS-structure, resulting in an oxide width of 1.7μm, see figure 3.3. Figure 3.4 shows the effect of the larger oxide width on the depletion width. For both situations four equipotential lines are plotted. It is found that the depletion layer will be wider in the situation of an oxide width of 1.7μm. Figure 3.5 shows the subthreshold curves for both situations. The lowering of the threshold voltage is evident, as well as the lowering of the subthreshold slope.

3.3.2 The influence of the oxide bending

According to the theory of section 1.7, increasing the bending of the oxide boundary should lead to an increase of spreading of the electric field lines and therefore lead to a stronger over-all corner effect. Figure 3.6 shows two devices which were used to investigate the influence of the oxide bending. Both devices have an oxide width of 0.7μm and an oxide thickness of 0.5μm, but the depth of the oxide thickness in silicon is increased from 0.25μm to 0.3μm.

Table 3.1 gives some values which were found for the subthreshold slope for drain voltages of 0.1V and 5V. The junction depth equals 0.2μm and the backgrounddope equals $5 \times 10^{16} cm^{-3}$

It is found that a stronger bending of the oxide leads to a higher subthreshold slope. Once more, the presence of the over-all corner effect is illustrated.

Table 3.1: *Subthreshold slope (V/dec) for different LOCOS dimensions and drain voltages*

LOCOS DEPTH IN SILICON (μm)	OXIDE WIDTH (μm)	DRAIN VOLTAGE (V)	
		0.1	5.0
0.25	0.7	1.32	1.12
	1.7	1.09	1.09
0.30	0.7	1.63	1.32
	1.7	1.28	1.28

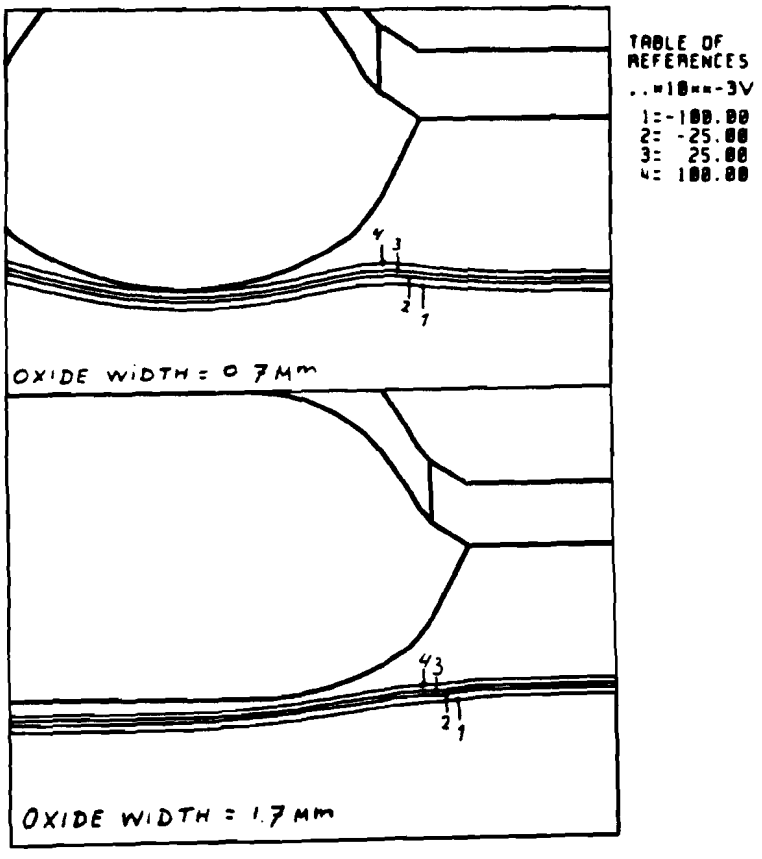

Figure 3.4: *The influence of the oxide width on the depletion width*

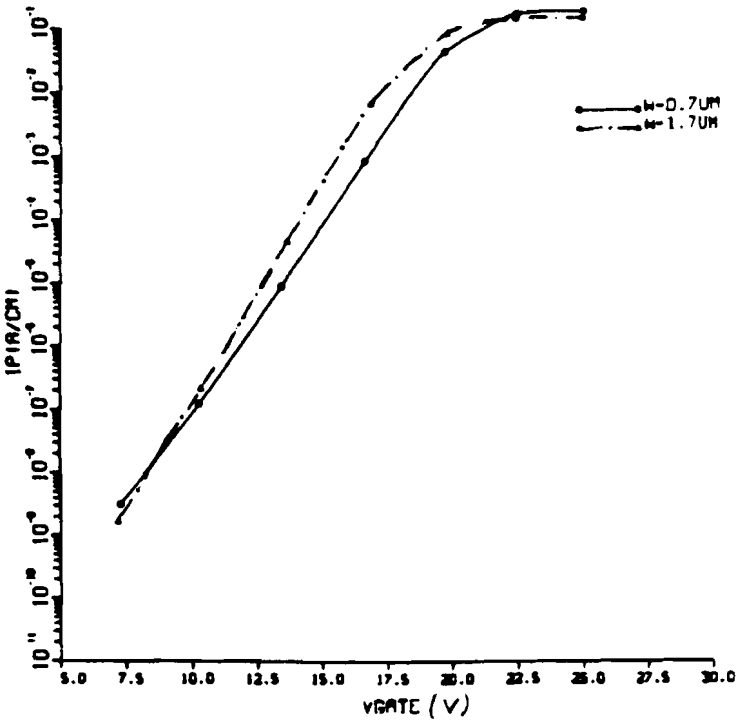

Figure 3.5: *The influence of the oxide width on the subthreshold curve*

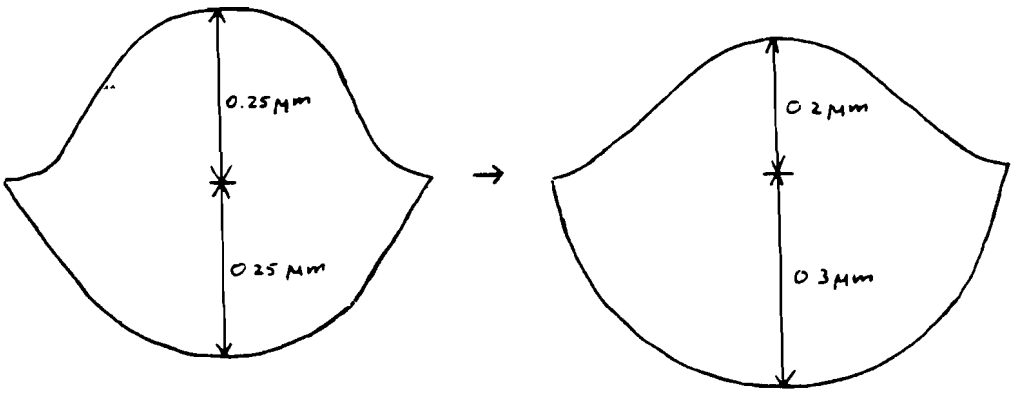

Figure 3.6: *Stronger bending of the oxide-boundary*

Chapter 4

BOX-isolation

4.1 Introduction

In 1980, a new isolation-technology was presented ([ref7], [ref8]), which results in a bird's beak-free isolation structure. Since isolation is achieved by Burying OXide into etched grooves, this technology is called BOX. The fabrication process is schematically outlined in figure 4.1 The absence of

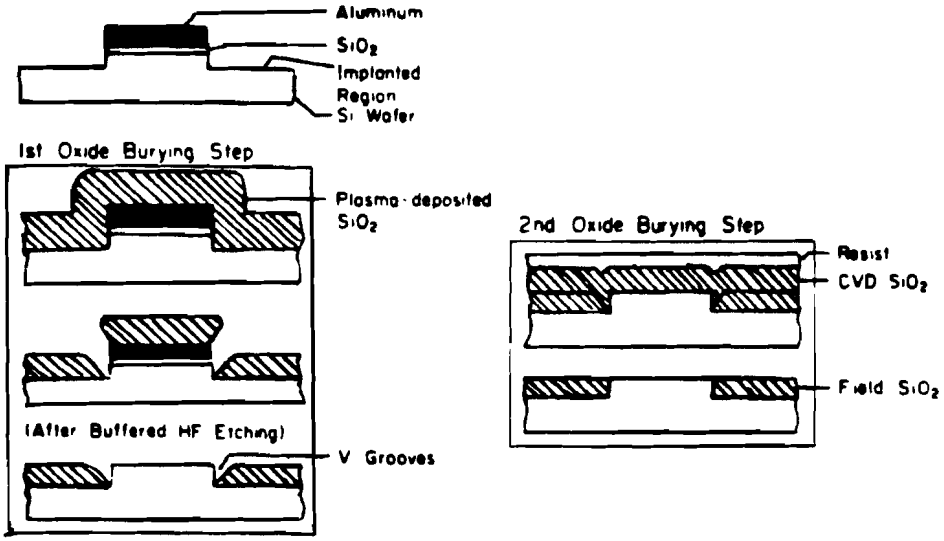

Figure 4.1: *Fabrication process steps of BOX*

the bird's beak and the near-perfect planar surface, make BOX a potential isolation technology for VLSI fabrication processes. It facilitates increasing gate electrode pattern accuracy and increases the punch-through voltage between neighbouring diffused junctions.

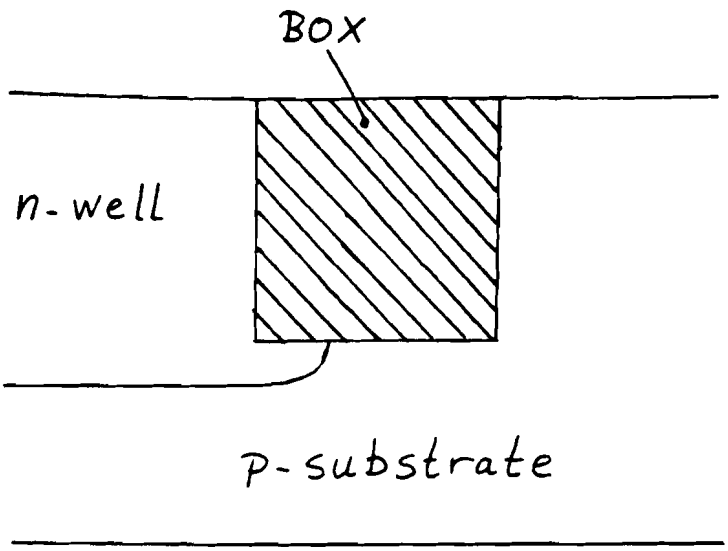

Figure 4.2: *A CMOS-situation*

4.2 Side-wall Inversion

In [ref11] it is found that one of the major problems of BOX is side-wall inversion. Figure 4.2 shows a CMOS-situation for BOX to explain this effect. At reduced oxide widths, applying a voltage to the n-well will influence the potential at the other side of the oxide. In the worst case, inversion can occur at this side-wall. This explains the name 'side-wall inversion'.

With LOCOS, the occurence of this problem is suppressed by the out-diffusion of the channelstopper. For BOX, a difficult implantation at the vertical sides of the oxide will have to be done, because of the absence of the self-aligned channelstopper. In addition to this, the oxide-charge will be higher than in case of LOCOS-isolation, because the quality of the deposited oxide, see figure 4.1, is inferior to the grown LOCOS-oxide.

Table 4.1 shows MOST threshold voltages for various small values of the oxide thickness and the substrate dope. The oxide-charge is chosen to be $1 \times 10^{11} q$.

From this table it is found that, at reduced oxide widths, even for low values of the well-voltage, side-wall inversion may occur . In section 4.4 simulations are described, which were made in order to obtain information about the occurence of this effect.

Because of the 3-dimensional character of the described side-wall inversion, simulations are carried out with a 3-dimensional simulation program. In the next section, this program will be described.

Table 4.1: *MOST Threshold voltages (V)*

DOPE	*OXIDE WIDTH (μm)*				
(cm^{-3})	0.5	0.4	0.3	0.2	0.1
5E15	2.21	1.71	1.22	0.72	0.22
1E16	4.39	3.45	2.52	1.59	0.66
5E16	14.0	11.1	8.30	5.46	2.62
1E17	21.4	17.0	12.7	8.41	4.10

4.3 The 3-D Simulation Program

The simulations, described in the following sections, were made with the simulation program TRIPOS. TRIPOS uses the finite difference method to solve 3-dimensional electrostatic potential problems in reverse biased semiconductors [ref9]. It solves the Poisson equation, so no currents can be calculated.

With [ref10], an estimation for the value of the (parasitic) current between a source and drain of different transistors is found to be:

$$I = qD_n n_{top} \frac{W^* Z^*}{L^*} exp(-\frac{qV_{max}}{kT}) \tag{4.1}$$

where n_{top} denotes the topdope of the source diffusion. V_{max} denotes the maximum value of the potential barrier between source and drain, which is illustrated by figure 4.3. L^* denotes the effective length of the region of electrons near point P, see figure 4.3, which controls the current, W^* and Z^* denote the effective width in both directions perpendicular to the direction of the current path. In case of a 2-dimensional simulation, W^* denotes the device width.

The value of L^* can be approximated by the distance along the current path between the points where $\psi = \psi_P + \pi kT/4q$, with ψ_P the potential in P. The same approximations are found for W^* and Z^*, except for the fact that in this case the potential has to be $\pi kT/4q$ lower than in P.

4.4 Simulations and results

4.4.1 The location of the current path

Simulations were made with the device which is schematically shown in figure 4.4.

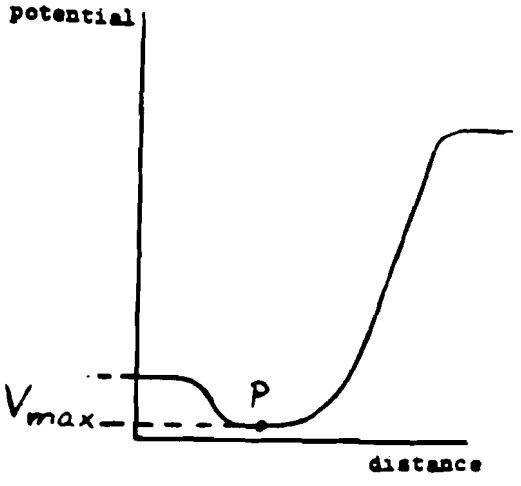

Figure 4.3: *Definition of* V_{max}

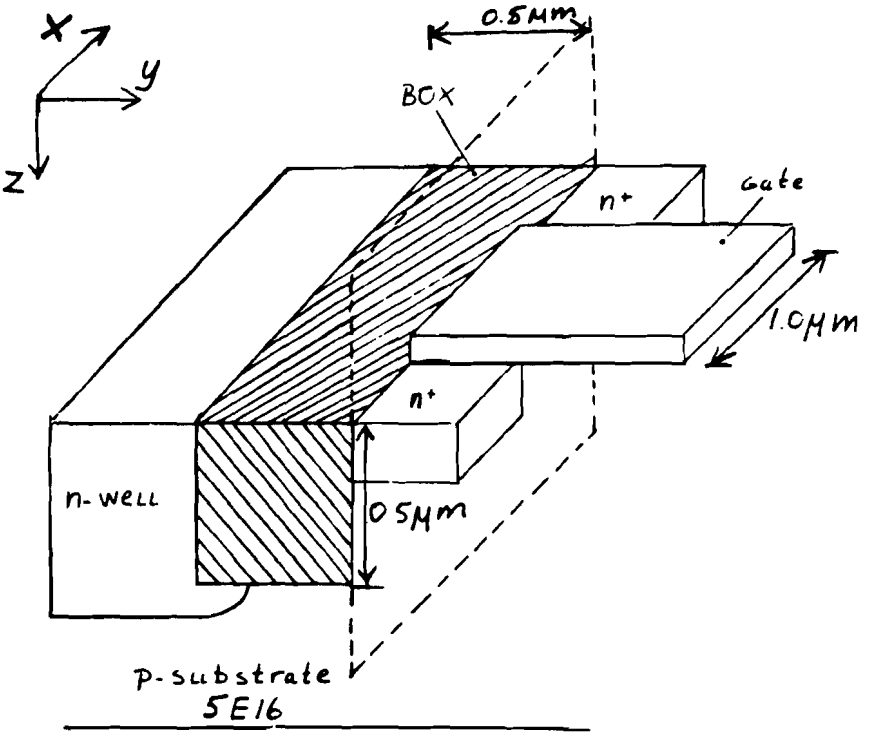

Figure 4.4: *The simulated structure*

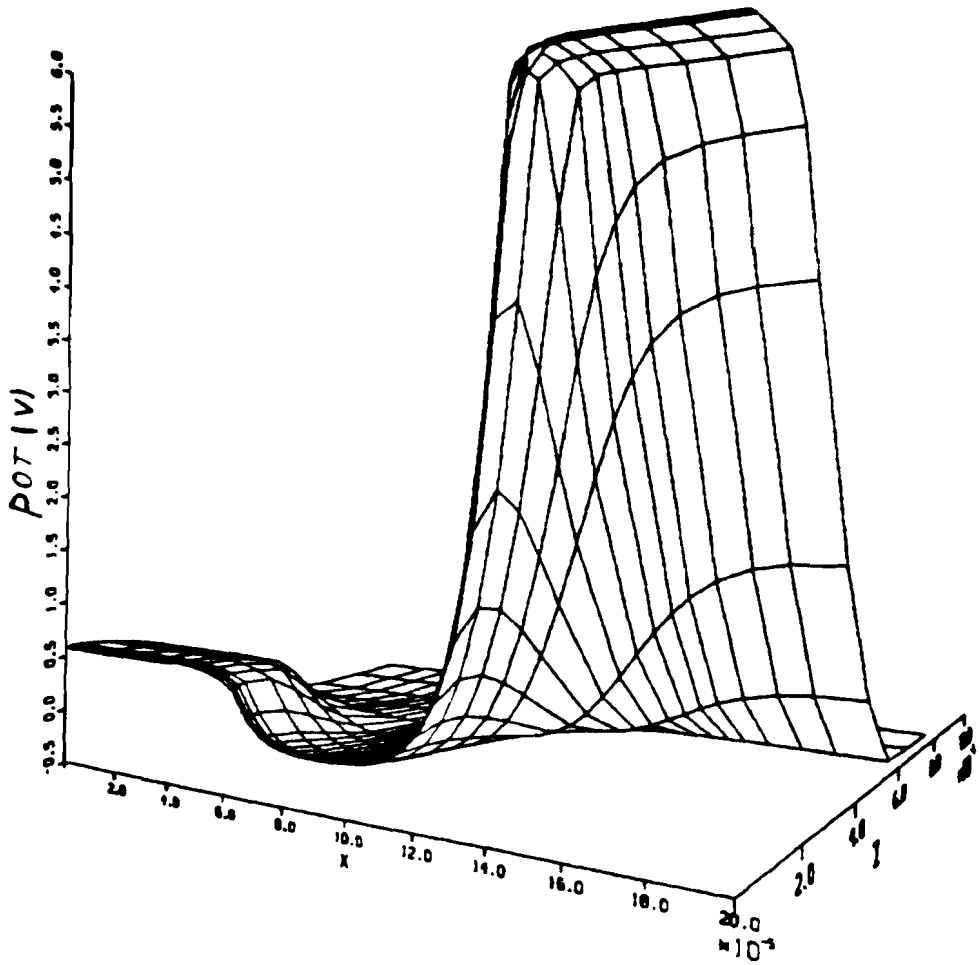

Figure 4.5: *The potential distribution at the side-wall with a view from the gate*

Figure 4.5 shows the potential distribution at the side-wall (given by the dashed line in figure 4.4), with a view from the gate. The gate-voltage was set to 0V, the drain- and well-voltage to 5V.

The potential barrier between source and drain is found to have the lowest value right underneath the gate, so the drain current will flow in a surface channel under the gate, like in the normal situation. In this case the influence of the n-well and the oxide-charge will raise the potential at the oxide-boundary, see figure 4.6, so the current path will be located in the region schematically given in figure 4.7.

From figure 4.7 we see that the BOX-structure can be regarded as the gate oxide of a parasitic transistor, given by the dotted line. The n-well can be seen as gate and drain of this transistor. Because of the corner effect, see chapter 3, no current will flow around the oxide.

The influence of the described parasitic transistor will depend on parameters including the oxide-thickness and the applied voltage to the well. Therefore the simulations described in the following sections were done.

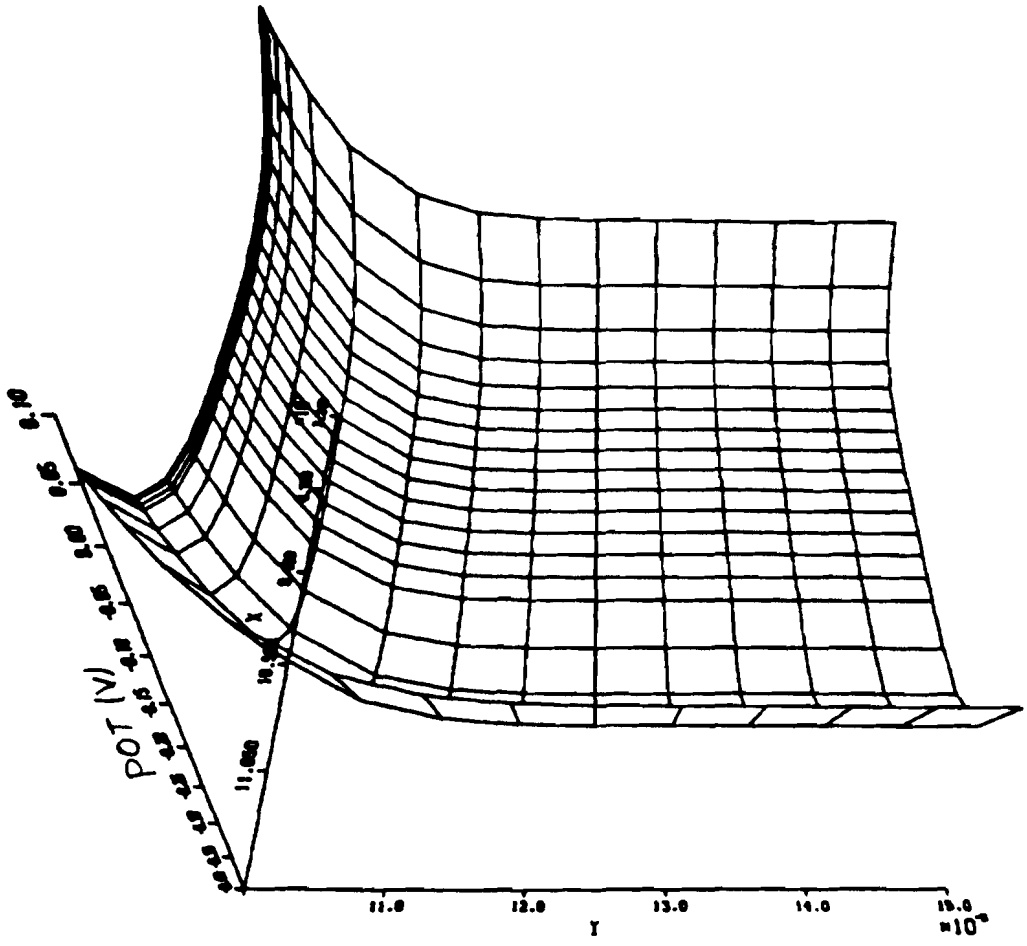

Figure 4.6: *Raising of the potential at the oxide-silicon boundary*

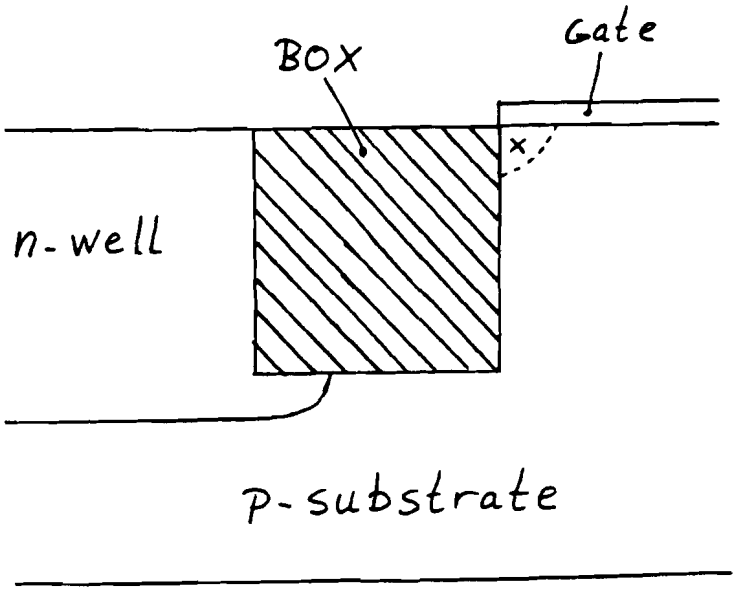

Figure 4.7: *Location of the current path*

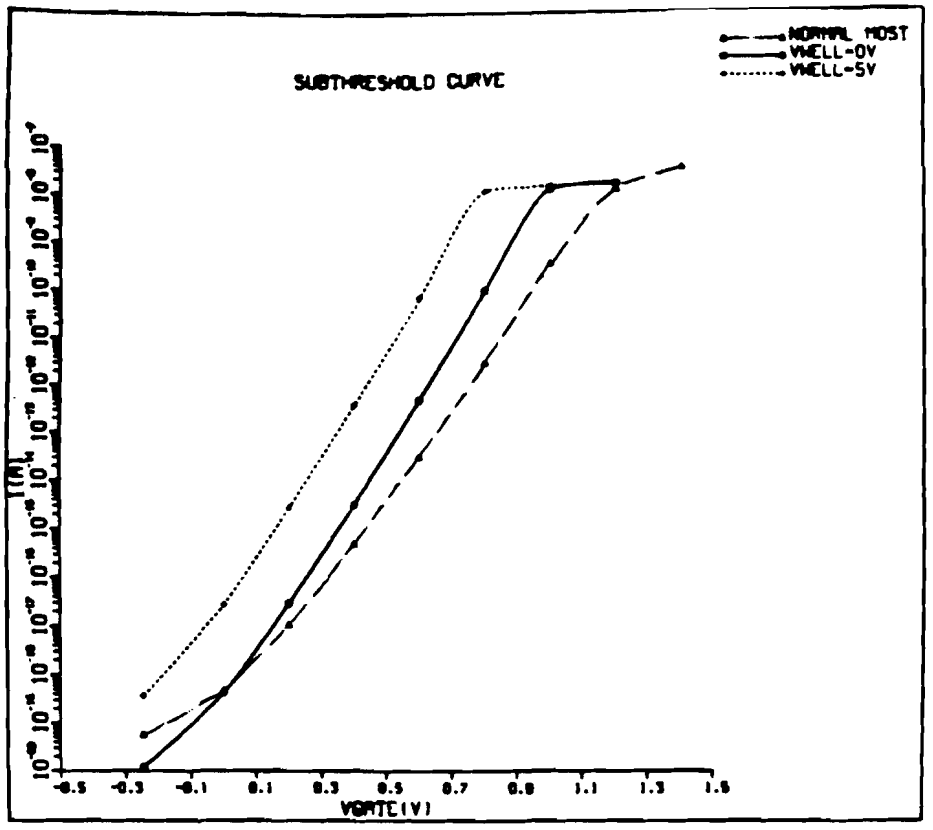

Figure 4.8: *Influence of the presence of the well*

4.4.2 Influence of the presence of the well

In order to find the influence of the presence of the n-well, the subthreshold curve was determined for the MOST in the structure of figure 4.4. First the subthreshold curve was calculated without the presence of the well, afterwards with a well-voltage of 0V and 5V. The drain voltage was set to 0.1V. Figure 4.8 shows the resulting curves. The presence of the well is found to have a considerable influence on the subthreshold behaviour.

4.4.3 Influence of the oxide width

Figure 4.9 shows the influence of reducing the oxide width on the subthreshold curve of the simulated MOST. Again, a considerable influence on the subthreshold behaviour is found.

4.4.4 Influence of the applied voltage to the well

Figure 4.10 shows the influence of the voltage applied to the well at an oxide width of 0.5μm. The influence of the applied voltage is found to be considerable, as in the previous cases.

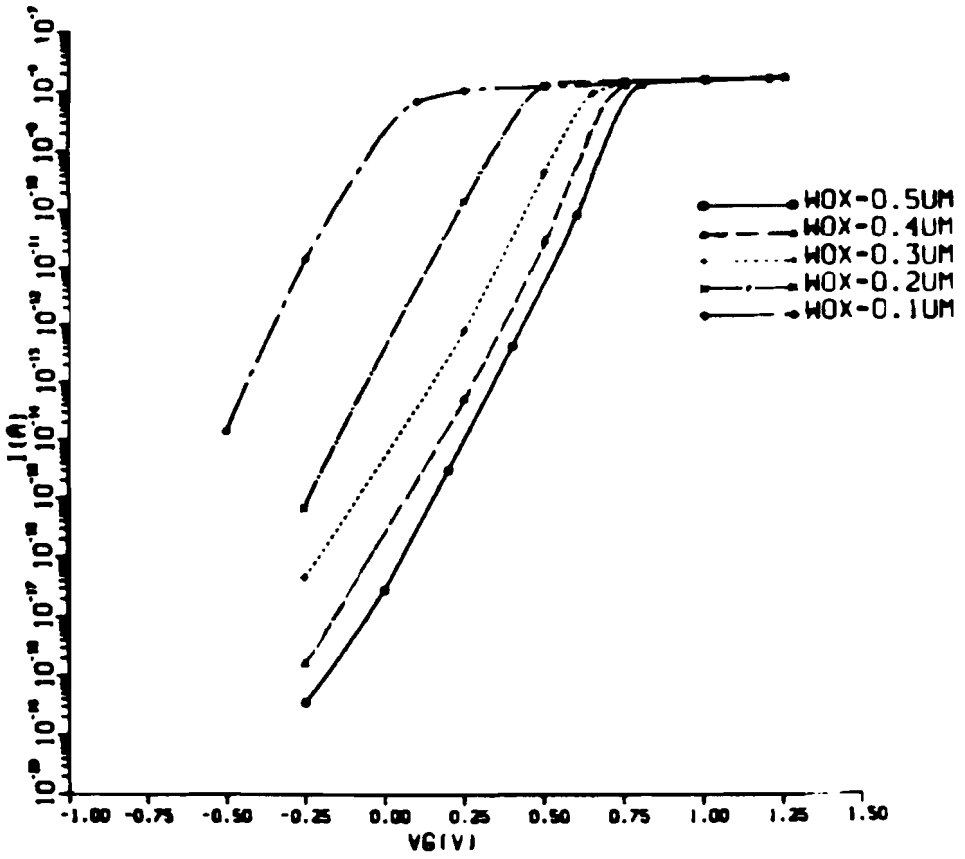

Figure 4.9: *Influence of the oxide width*

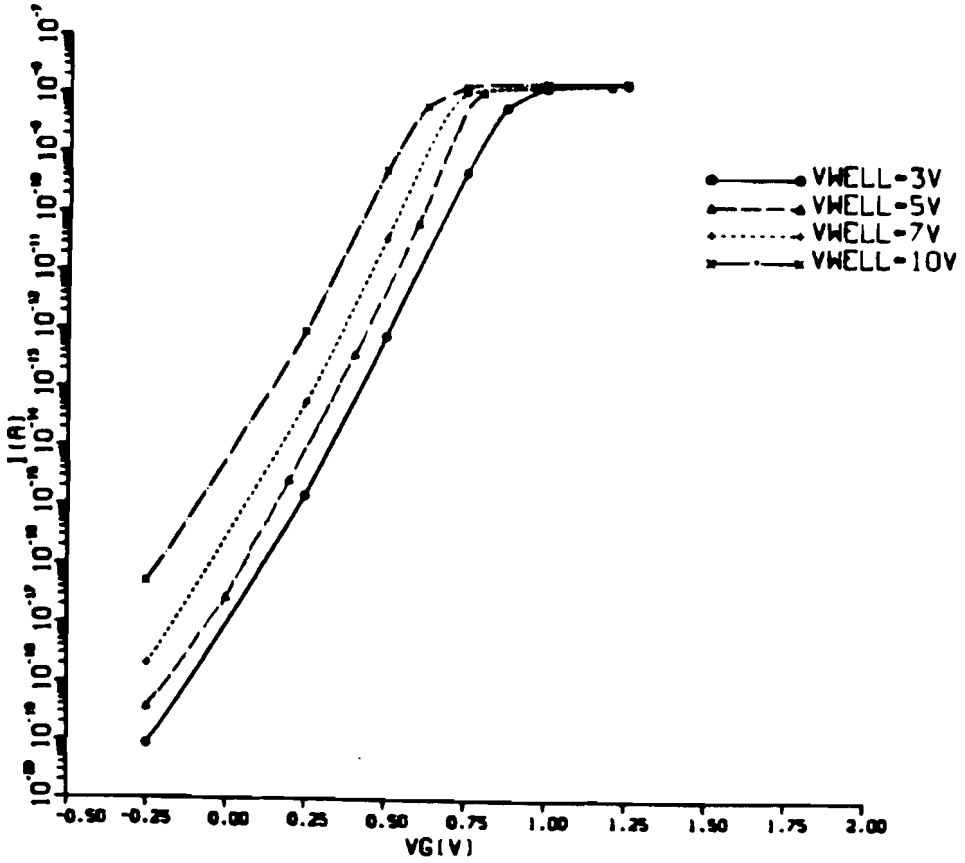

Figure 4.10: *Influence of the well-voltage*

4.5 Discussion

The outstanding isolation properties of BOX, as stated in several publications, are in contrast with the negative feature described in this chapter. The occurence of side-wall inversion will influence the characteristics of transistors sited next to that side-wall, which must be avoided. The 3-dimensional character of side-wall inversion, indicates the advantage of using a 3-dimensional simulation program. BOX can only be useful for future VLSI design, if means are developed to solve this problem.

Chapter 5

Conclusions

In this report, results of 2- and 3-dimensional simulations on CMOS device isolation techniques were described.

By choosing the right values for the various variables, an n^+ - n^+ spacing of 0.7μm can be achieved with the modified LOCOS isolation technology. The parasitic current of this device is found to be reduced by the over-all corner effect, a 2-dimensional effect which reduces the depletion width at the oxide-silicon boundary.

From 3-dimensional simulations on BOX isolation technology, the presence of side-wall inversion for oxide widths in the order of 0.5μm is found. This 3-dimensional effect influences the characteristics of an adjacent MOST and implies a potential limiting factor for future reduction of active device spacings.

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Appendix A

List of Symbols

Symbol	Description	Unit
C_D	Depletion capacitance	F
C_{ox}	Oxide capacitance	F
d	Oxide thickness	cm
d_{eff}	Effective oxide thickness	cm
D	Depletion width	cm
D_n	Diffusion coefficient for electrons	cm^2/s
ϵ	Permittivity	F/cm
ϵ_{ox}	Permittivity in Silicon dioxide	F/cm
ϵ_{si}	Permittivity in Silicon	F/cm
ϕ_n	Fermi potential for holes	V
ϕ_p	Fermi potential for electrons	V
I_d	Drain current	A
J_n	Electron current density	A/cm^2
k	Boltzmann constant	J/K
L_D	Debye length	cm
μ_n	mobility for electrons	cm^2/Vs
n	electron concentration	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
N	Doping concentration	cm^{-3}
N_a	Acceptor doping concentration	cm^{-3}
N_d	Donor doping concentration	cm^{-3}
N_{top}	Maximum doping concentration	cm^{-3}
p	Hole density	cm^{-3}
Ψ	Electrostatic potential	V
Ψ_s	Surface electrostatic potential	V
q	Elementary charge	C
ρ	Space charge density	C/cm^{-3}
S	Subthreshold slope	V/decade
x_R	Right mask edge	
x_L	Left mask edge	
x_j	Source/drain junction depth	μm