Low stress power factor correctors for universal input applications

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Low Stress Power Factor Correctors for Universal Input Applications

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Preface

This report describes my graduation assignment done at Philips Lighting in Eindhoven in the period march 2006 – april 2007. This assignment has given me the opportunity to get insight of Power Factor Corrector circuits. The assignment also included a practical part, which gave me besides theoretical knowledge also a lot of practical experience.

During my work, many problems were encountered, some of them were solved by myself, but many others were solved after some good suggestions were given. Therefore I would like to thank Marcel Hendrix and Jorge Duarte for their support last year. I would also like to thank Ron Jacobs for his support and Rob Braan for his interest in my work. Last but not least I would like to thank the people at "Fluo", besides their technical support they created comfy environment for me.

This assignment finalizes my study which I started in 2001. Especially the first years were difficult; therefore I would like to thank my parents and my girlfriend for their support.

SUMMARY

In this report three Power Factor Corrector (PFC) topologies are analyzed: SEPIC, Low stress Buck Boost and Single inductor Buck Boost. For the SEPIC PFC and Low stress Buck Boost PFC an efficiency analysis is done. From it is concluded the Low stress Buck Boost PFC offers a higher efficiency with respect to the SEPIC PFC. Therefore an prototype is build and validated by measurements.

In the first two chapters a general introduction is given. It is explained why PFCs are needed and what its function is. Also some PFC topologies and controlling strategies are discussed briefly.

In chapter three, three PFC topologies for universal input applications are analyzed: the SEPIC PFC, Low stress Buck Boost PFC and the Single inductor PFC.

In the fifth chapter an efficiency analysis is done, comparing the SEPIC PFC with the Low stress Buck Boost PFC. From the results can be concluded the Low stress Buck Boost PFC is better than the SEPIC PFC. In chapter four it is explained how both PFCs are modeled.

In chapter six it is discussed how a prototype of the Low stress Buck Boost is realized and is chapter seven the measurement results are discussed.

CONTENT

1 INTRODUCTION

Since the list of domestic equipment which use AC/DC conversion is still growing, the energy suppliers have strict norms for maintaining the grid quality. Polluting the grid by causing harmonic distortion or demanding apparent power leads into additional losses. Harmonic distortion will lead into speed variations of the generator at the power plant, which is unwanted. Demanding apparent power causes additional conduction losses and needs oversized transmission lines. Besides these additional losses a polluted grid might cause disturbances for other users.

To overcome these problems there are general rules for electronic. Since lighting is widely applied, it not only takes a significant part of the total energy consumption, but might also cause serious pollution of the grid. These facts result into relative strict rules for lighting equipment.

To meet these requirements, manufacturers of lighting electronics often apply a Power Factor Corrector (PFC) in their equipment. With a PFC, the power factor is almost optimal and the harmonic distortion can be kept within the limits. Such a PFC is based on Switch Mode Power Supply (SMPS) topology and will be restricted by its properties.

Fluorescent lamp driver (such as TL tubes) are usually fed by a DC bus voltage which is higher than the peak input voltage. In this case the boost topology can be applied. However, in some (industrial) situations the peak input voltage can be higher than the required bus voltage. In this situation the boost topology is not suitable anymore and another topology, called universal input, must be applied.

There are different SMPS topologies for universal input situations (situations where the rectified input voltage can also be lower than the output voltage) and with all these topologies a proper power factor is obtainable. However, the efficiency, component stress, harmonic distortion and also the complexity of the circuit will differ. This report focuses on the efficiency and component stress of the PFC. Not only because a ballast (including PFC) with a very high efficiency is commercially attractive. But also because a high efficiency leads into less heating problems, which means the housing can be smaller. By reducing the component stress, not only the efficiency increases, but also less complicated components can be used, which makes a cheaper PFC (and ballast) possible.

In this report an efficiency comparison between two PFC topologies, suitable for universal input applications, will be done. Finally the topology with the highest efficiency will be designed and build. The goal is to design a PFC with the following specifications:

V_{IN}	$312-530\ V_{RMS}$ @ $50\ Hz$
PF	>0.98
THD	$<10\%$
V_{OUT}	$450\ V_{DC}$
P_{out}	$100-320\ W$
$Mains\ surge$	$2\ kV$

After building this prototype, the efficiency and other properties of the PFC will be determined by measurements.

2 CHAPTER 2 POWER FACTOR CORRECTION

In this chapter first the need for a Power Factor Corrector (PFC) will be explained. After that it is shown how switched mode power supplies can be used to maintain a unity power factor. Different control techniques for Power Factor Correctors will be discussed in the last section of this chapter.

2.1 THE NEED FOR A POWER FACTOR CORRECTOR

As mentioned in the previous section, the input voltage of a ballast needs to be rectified and converted to a certain constant bus-voltage. (Fig 2.1). This bus voltage is the input for the lamp driver.

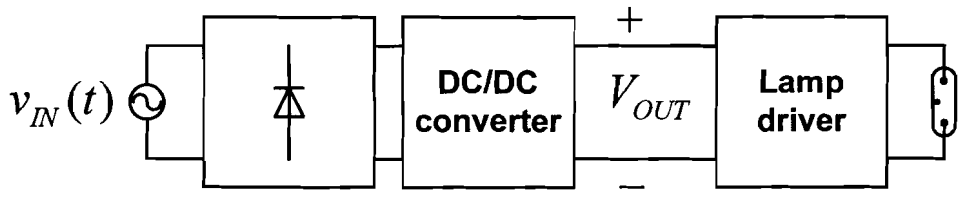


Figure 2.1, Functional schematic of a lamp ballast.

A conventional rectifier consists of a rectifier bridge and a buffer capacitor, as shown in Fig 2.2.

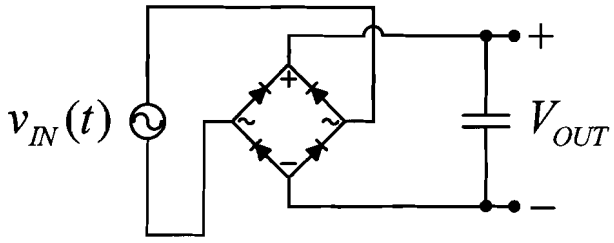


Figure 2.2, Conventional rectifying circuit.

The disadvantage of this method is that there will only flow a current when the capacitor voltage is lower than the input voltage, resulting in a discontinuous and distorted input current as shown in Fig 2.3.

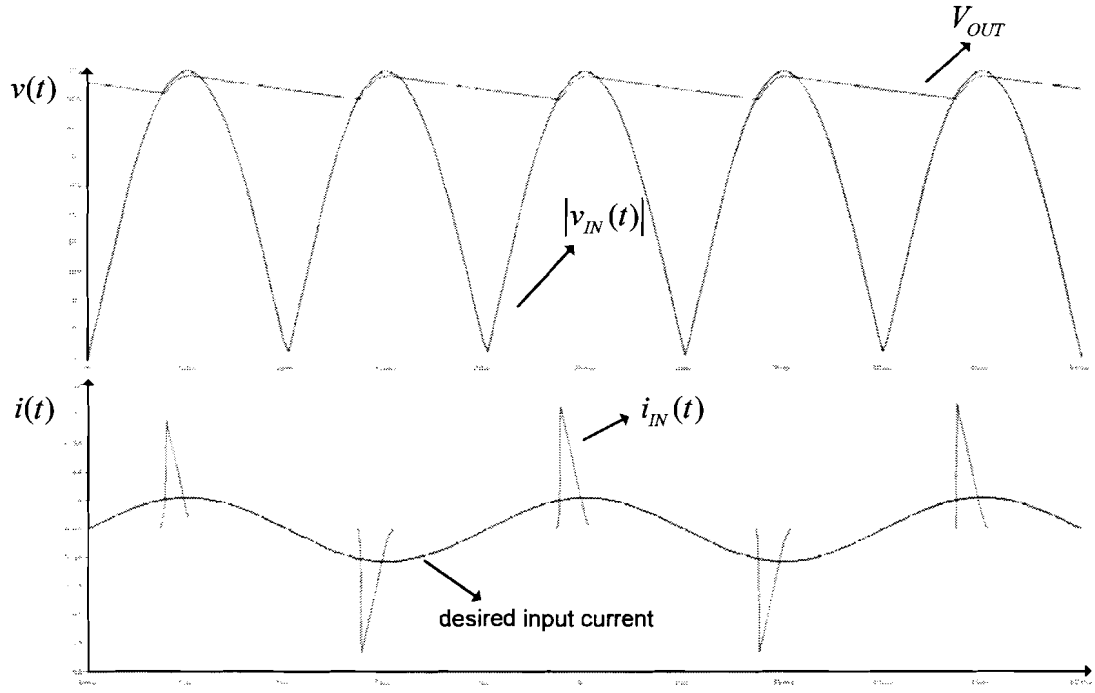


Figure 2.3, Waveforms of a conventional rectifier circuit.

Since this will affect the quality of the grid and thus must be avoided, there are strict (especially for lighting) rules for electronic equipment which must be met. For low power applications (several watts) a conventional rectifier in combination with a small low pass filter can still be used. However for higher power levels this will be unpractical and another rectifying and voltage regulation method needs to be used; a Power Factor Corrector (PFC).

2.2 SWITCHED MODE POWER SUPPLIES (SMPS)

As we will see later, a PFC is based on Switched Mode Power Supplies (SMPS) technology. Some well known topologies are: boost, buck, Ćuk, SEPIC and buck boost. In the case of the boost topology the input voltage must always be lower than the output voltage, the buck converter can only transform downwards, while the others (Ćuk, SEPIC, and buck boost) can transform in both directions. There are many methods for controlling SMPS's and PFC's. Some PFC controlling methods are discussed in [1]. The common approaches are:

- Continuous conduction mode (CCM)
- Discontinuous conduction mode (DCM)
- Boundary conduction mode (BCM)

For a simple boost converter, shown in Fig 2.4, the current waveforms for these controlling methods are shown in Fig 2.5.

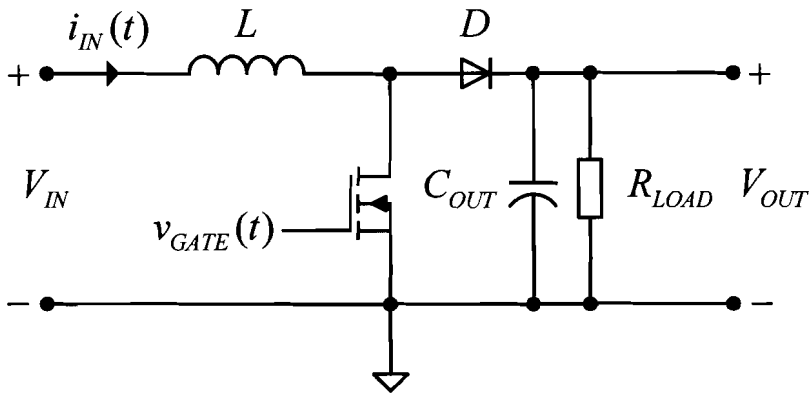


Figure 2.4, A simple boost converter.

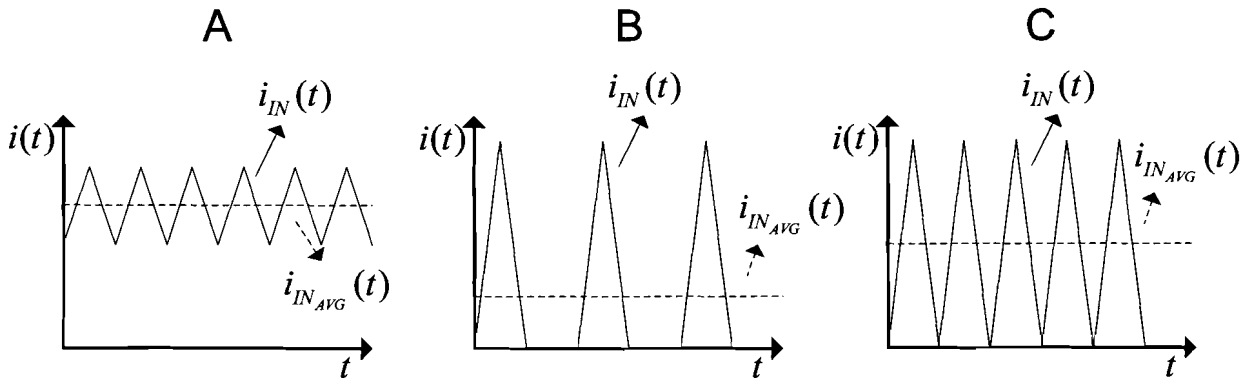


Figure 2.5, Input current for several controlling methods, CCM (A), DCM (B) and BCM (C).

Continuous conduction mode (A) is usually applied in high power applications. The switching frequency is constant and the shaped current is close to the average current, so oversized components are not needed. Disadvantages of this mode are the continuous conduction losses and the switching losses; both the switch and the diode are hard switched.

Discontinuous mode (B) is usually applied in low power applications, in this mode there is no continuous energy transfer to the output. An advantage is that the diode is switched off softly and the switch also turned on softly. Disadvantages of this method are that the switching frequency is not fixed and that the peak values (voltage and current) are much larger than the average values (voltages and currents), demanding oversized components.

For 'medium' power applications there is a compromise between CCM and DCM; Boundary conduction mode (BCM). It is similar to DCM but the switch will immediately be turned on again after the diode current has become zero. This has the advantage that, compared to DCM, less over sizing of the components is needed. And the switching losses are lower than CCM. A disadvantage is the varying switching frequency and the fact that the peak current values are still much larger than the average values.

Usually, in lighting applications BCM is applied. The efficiency is higher than CCM which leads to less heating problems and cheaper components can be used than for DCM.

2.3 SWITCHED MODE POWER SUPPLIES AS POWER FACTOR CORRECTOR

As mentioned in the previous section, the function of a PFC is to deliver a certain constant DC output voltage while at the same time the current drawn from grid must meet the rules. These two functions of a PFC can be defined by:

- Regulate the output to the desired voltage.
- Shape the input current in such a way that it will meet at least the rules.

A PFC is based on a switched mode power supply (SMPS), and a dedicated controller will control the SMPS in such a way that the input current will be sinusoidal and the output voltage is constant. Thus, in fact there are two control loops; one loop shaping the input current and one loop regulating the output voltage. An example of a PFC based on a boost (SMPS) topology will be used for gaining insight in PFC technology. A simplified schematic of a boost PFC is shown in Fig 2.4.

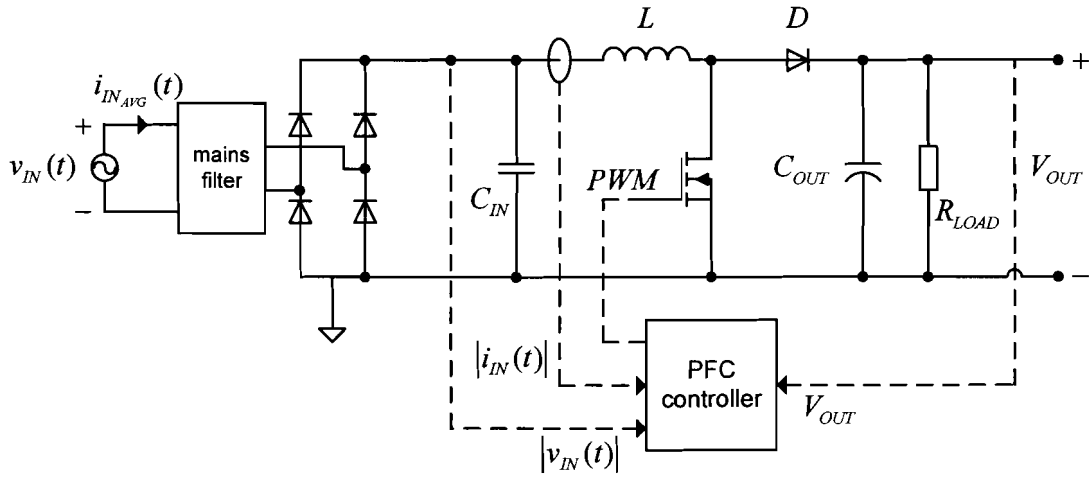


Figure 2.6, Simple boost PFC.

The input current will be shaped by using high frequency PWM which requires a large bandwidth. The bandwidth of the output voltage controller however, must be very small (in the order of 10 to 20 Hz). Since the input current and voltage are both sinusoidal, the instantaneous input power will be sinusoidal (with an offset) too. The instantaneous output power however, is approximately constant. By allowing a ripple (with twice the line frequency) on the output capacitor the instantaneous difference between in -and output power can be absorbed. This means that the voltage regulator may not reject this ripple, when the ripple is rejected the output power is constant and constant input power without a distorted input current is not possible.

Assuming that the boost PFC shown in Fig 2.6 is operating in BCM, its input current and output voltage are both shown in Fig 2.7.

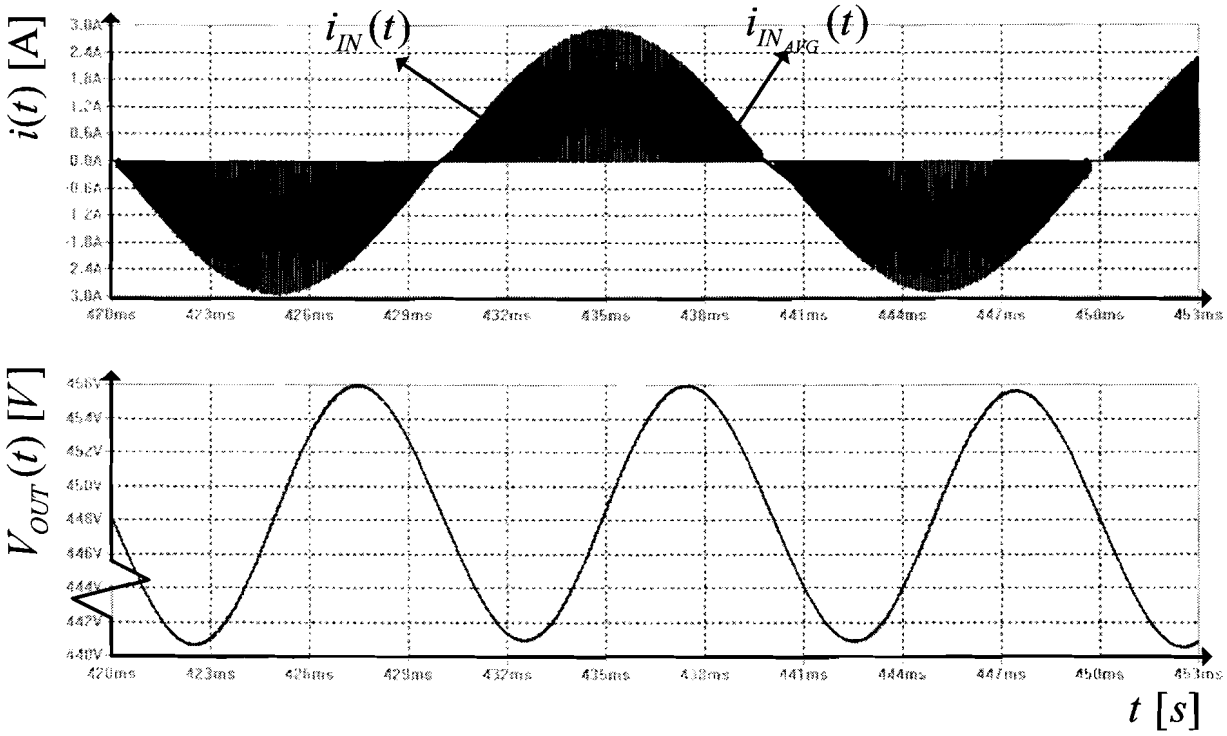


Figure 2.7, Not filtered input current $i_{IN}(t)$, filtered input current $i_{IN_{AVG}}(t)$ and output voltage $V_{OUT}(t)$ of the Boost PFC.

In this figure (Fig. 2.7) it can be seen that the PFC shapes a pure (average) sinusoidal input current, even the ripple at the output is clearly visible. Since the bandwidth of voltage control loop is very small, this ripple will appear and a unity power factor is possible.

Assuming the input current is:

$$i_{IN}(t) = \hat{I}_{IN}\left|\sin(\varpi t)\right| \tag{1.1}$$

and the input voltage is:

$$v_{IN}(t) = \hat{V}_{IN}\left|\sin(\varpi t)\right| \tag{1.2}.$$

the instantaneous input power equals:

$$p_{IN}(t) = \hat{I}_{IN}\hat{V}_{IN}\sin^2(\varpi t) = \frac{\hat{I}_{IN}\hat{V}_{IN}}{2}\left(1-\cos(2\varpi t)\right). \tag{1.3}$$

The output voltage and the load are nearly constant , which means the output power is also constant and is given by (1.4).

$$P_{OUT} = \frac{V^2_{OUT}}{R_{LOAD}} \qquad (1.4)$$

Since the instantaneous input power has a sinusoidal part and the output power is constant, some energy must be stored for a short time. This will be done in the output capacitor and will lead into a ripple voltage across the capacitor with twice the line frequency.

It can be concluded that shaping a sinusoidal input current with a boost PFC as shown in Fig. 2.6 will always result into a ripple voltage across the output capacitor.

2.4 POWER FACTOR CORRECTORS FOR UNIVERSAL INPUT APPLICATIONS

In the previous section the boost PFC has been discussed briefly. However, applying a boost topology as a PFC is only possible when the instantaneous input voltage is never higher than the output voltage. Since a PFC must be investigated which is suitable for universal input voltage, the boost topology cannot be applied. Topologies that are suitable for universal applications are:

- SEPIC
- Çuk
- Zeta
- Flyback
- Buck boost
- Low stress buck boost

The converters are shown in Fig 2.8, 2.9 and 2.10.

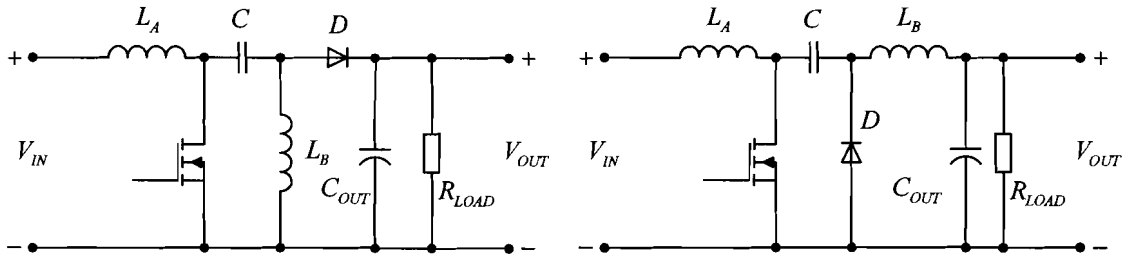


Figure 2.8, SEPIC and Çuk converter.

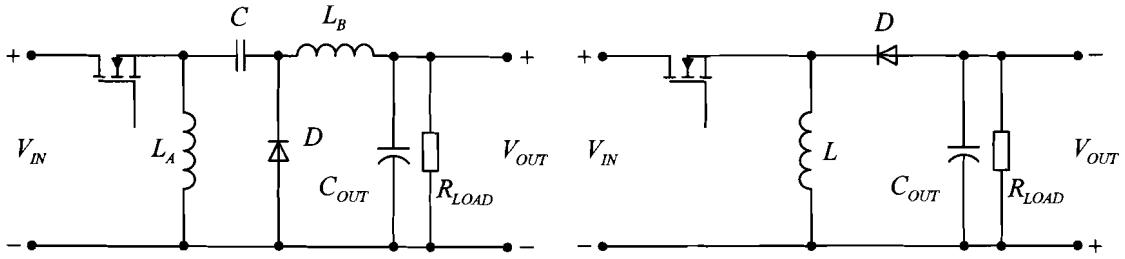


Figure 2.9, Zeta and Flyback converter.

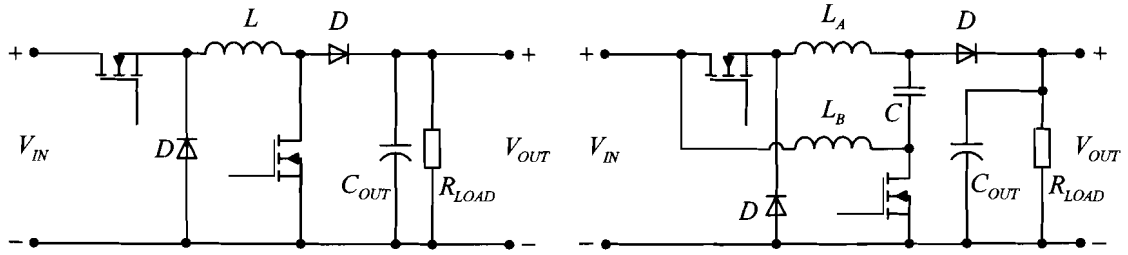


Figure 2.10, Buck boost and Low stress buck boost converter.

When comparing SMPS topologies for PFC applications there are several aspects of (economic) interest, e.g. the number of components, the component stress and whether the input current is continuous or not. When less components are used, the PFC might be cheaper. When the component stresses are lower, less advanced and thus cheaper components can be used. When the input current is continuous the input filter can be kept smaller and the stresses will also be lower.

Since (a part of) the assignment is to compare the SEPIC PFC with the Low stress Buck Boost PFC, only these two topologies will be analyzed in detail in chapter 3.

3 CHAPTER 3 LOW STRESS POWER FACTOR CORRECTORS FOR UNIVERSAL INPUT APPLICATIONS

In this chapter the SEPIC PFC and Low stress buck boost PFC will be analyzed. Since the Buck boost PFC is similar to the Low stress buck boost PFC, this topology will be analyzed too.

3.1 SEPIC

In this section first the SEPIC topology operating with a constant input voltage will be discussed. In the second part the SEPIC as PFC in BCM will be discussed.

3.1.1 The SEPIC converter

In this section it is assumed the SEPIC converter is operating in BCM (or CCM) and supplied with a constant input voltage. The SEPIC converter contains two inductors, two capacitors, one diode and one switch as shown in Fig 3.1

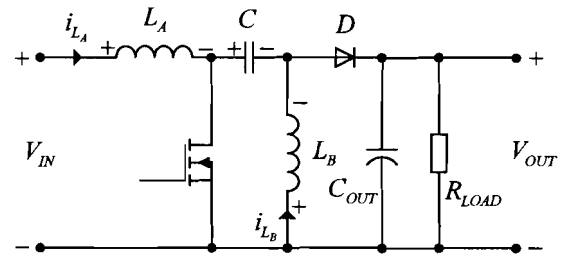


Figure 3.1, SEPIC converter.

Since the converter is operating in BCM mode, there are only two states (in CCM there are also two states); in the first state the switch is closed and the diode is blocking, in the second state the switch is opened and the diode conducting. The two states are shown in Fig 3.2.

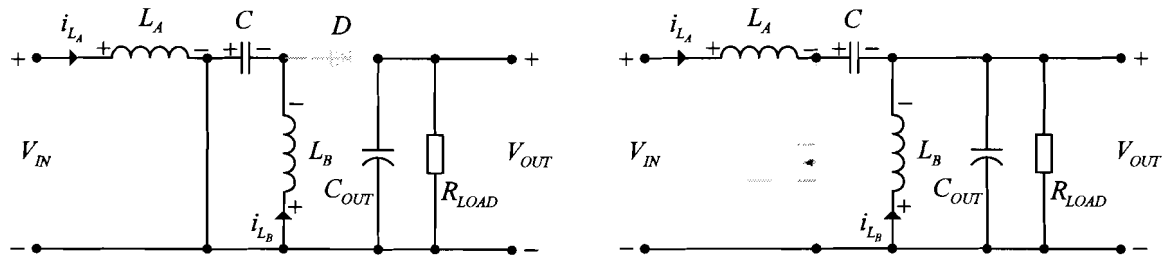


Figure 3.2, Two states of the SEPIC converter.

Assuming the output capacitor (C_{OUT}) is very large, the output voltage (V_{OUT}) may be considered constant. The series capacitor C is assumed so large that the voltage across C will be constant during a high frequency cycle. In this situation the current flowing through the inductors in the first state can be written as:

$$i_{L_A} = \frac{V_{IN}}{L_A} t + I_{A2} \qquad (1.5) \qquad i_{L_B} = \frac{V_C}{L_B} t + I_{B2}. \qquad (1.6)$$

where I_{A2} and I_{B2} are the initial conditions and V_C is the voltage across the series capacitor C. The current will increase until the switch is turned off at $t = T_1$ and the second mode will start. The inductor currents at $t = T_1$ equal

$$I_{A1} = \frac{V_{IN}}{L_A} T_1 + I_{A2} \qquad (1.7) \qquad I_{B1} = \frac{V_C}{L_B} T_1 + I_{B2}. \qquad (1.8)$$

In the second state the switch is opened and the diode is conducting. In this situation the input voltages can be expressed as:

$$V_{IN} = V_{L_A} - V_{L_B} + V_C \Rightarrow V_{IN} - V_C = L_A \frac{d}{dt} i_{L_A} - L_B \frac{d}{dt} i_{L_B}. \qquad (1.9)$$

Integrating the right hand expression of (1.9) and applying the boundary conditions gives:

$$(V_{IN} - V_C)t + L_A I_{A1} - L_B I_{B1} = L_A i_{L_A} - L_B i_{L_B}. \qquad (1.10)$$

At $t = T_2$ the second state ends and the first mode starts again. The inductor currents i_{L_A} and i_{L_B} at $t = T_2$ are respectively I_{A2} and I_{B2}, and (1.10) becomes:

$$(V_{IN} - V_C)T_2 + L_A I_{A1} - L_B I_{B1} = L_A I_{A2} - L_B I_{B2}. \qquad (1.11)$$

By substituting (1.7) and (1.8) into (1.11) it follows that the voltage across the series capacitor equals the input voltage, thus $V_{IN} = V_C$. Now the steady state capacitor voltage is known, the inductor currents for the second state can be formulated:

$$i_{L_A} = -\frac{V_{OUT}}{L_A} t + I_{A2} \qquad (1.12) \qquad i_{L_B} = -\frac{V_{OUT}}{L_B} t + I_{B2}. \qquad (1.13)$$

where I_{A2} and I_{B2} are the initial conditions of the second state. At the end of the second state, at $t = T_2$, the first state starts again meaning that the end conditions of the second state

must equal the initial conditions of the first state. The initial conditions of the first state are thus:

$$I_{A2} = -\frac{V_{OUT}}{L_A} T_2 + I_{A1} \qquad (1.14) \qquad I_{B2} = -\frac{V_{OUT}}{L_B} T_2 + I_{B1}. \qquad (1.15)$$

By combining these initial conditions of the first state with the initial conditions of the second state, the transfer function of the SEPIC converter can be found.

$$\begin{cases} I_{A1} = \frac{V_{IN}}{L_A} T_1 + I_{A2} \\ I_{A2} = -\frac{V_{OUT}}{L_A} T_2 + I_{A1} \end{cases} \qquad (1.16) \qquad \begin{cases} I_{B1} = \frac{V_C}{L_B} T_1 + I_{B2} \\ I_{B2} = -\frac{V_{OUT}}{L_B} T_2 + I_{B1} \end{cases} \qquad (1.17)$$

The solution of both sets gives, of course, the same transfer function. By defining the duty cycle $T_1 = \delta$ and $T = T_1 + T_2 = 1$, the transfer function of the SEPIC converter becomes:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\delta}{1-\delta}. \qquad (1.18)$$

and the transfer characteristic is shown in Fig 3.4.

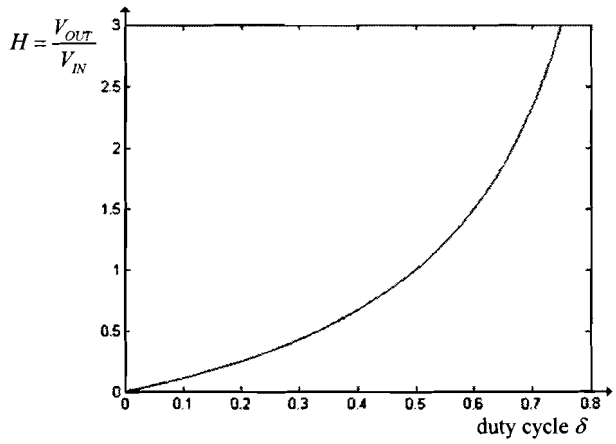


Figure 3.4, Transfer characteristic of the SEPIC converter.

3.1.2 SEPIC Power Factor Corrector in Boundary Conduction Mode

In the previous section the SEPIC converter is discussed for situations with a fixed input voltage, however in PFC applications, the input voltage is a rectified sine wave. Since the frequency of the input voltage is much lower than the switching frequency, it may be assumed that the input voltage is constant during a high frequency cycle. As mentioned

earlier, for lighting applications a PFC operating in BCM is preferable. A SEPIC PFC operating in BCM is well described in [2].

3.1.2.1 Currents and switching frequency of the SEPIC PFC

For analyzing the SEPIC PFC in BCM it is assumed the voltage across the output capacitor is constant and the input voltage is constant during a high frequency switching cycle. The voltage across the series capacitor equals the input voltage, as proved in the previous section. When operating in BCM, the switch will be closed until a certain reference current, $i_{PEAK}(t)$, is reached. Since unity power factor and low harmonic distortion are desired, $i_{PEAK}(t)$ must be proportional with the input voltage. The input voltage $v_{IN}(t)$ and the reference current $i_{PEAK}(t)$ are defined by:

$$v_{IN}(t) = \hat{V}_{IN} \left|\sin(\varpi t)\right| \tag{1.19}$$

$$i_{PEAK}(t) = \hat{I}_{PEAK} \left|\sin(\varpi t)\right|, \tag{1.20}$$

where $\hat{V}_{IN}$ is the amplitude of the grid (input) voltage and $\hat{I}_{PEAK}$ is the amplitude of the reference current. $\hat{I}_{PEAK}$ depends on the desired output voltage and the ratio between the output voltage and the amplitude of the input voltage, which will be discussed later.

When the switch is turned on (left hand picture in Fig. 3.5), the current through the switch starts increasing from zero. Since the current through the switch is the sum of the two inductor currents the switch current can be expressed as

$$i_{SWITCH}(t) = i_{L_A}(t) + i_{L_B}(t) = \frac{v_{IN}(t)}{L_A} t + \frac{v_{IN}(t)}{L_B} t = \frac{v_{IN}(t)(L_A + L_B)}{L_A L_B} t. \tag{1.21}$$

When the reference current, $i_{PEAK}(t)$, is reached at $t = T_{ON}$, the switch will be turned off. T_{ON} is the time span the switch is turned on and can be found by combining (1.20) and (1.21):

$$T_{ON} = \frac{\hat{I}_{PEAK}}{\hat{V}_{IN}} \frac{L_A L_B}{L_A + L_B} = \frac{\hat{I}_{PEAK}}{\hat{V}_{IN}} L_E \tag{1.22}$$

where $L_E = L_A // L_B$. Since equation (1.22) contains only constants this means that T_{ON} will be constant for a constant load and a constant $\hat{V}_{IN} / V_{OUT}$ ratio.

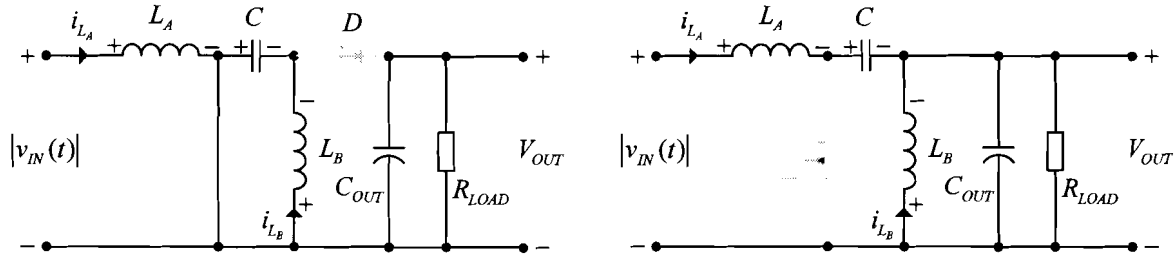


Figure 3.5, Two states of the SEPIC PFC.

After $i_{PEAK}(t)$ is reached, the switch will be turned off and the diode starts conducting as shown in the right hand picture of Fig. 3.5. When the diode is conducting the current through the diode is decreasing until it becomes zero and the diode will block. The current through the switch at $t = T_{ON}$ equals

$$i_{SWITCH}(t) = \frac{v_{IN}(t)}{L_E} T_{ON} . \tag{1.23}$$

Since the switch is turned off at $t = T_{ON}$ the initial condition of the diode current equals (1.23) and the diode current can be written as:

$$i_{DIODE}(t) = \frac{v_{IN}(t)}{L_E} T_{ON} - \frac{V_{OUT}}{L_E} t . \tag{1.24}$$

The time the diode is conducting is defined by t_{OFF}, which is the time t for which (1.24) becomes zero:

$$t_{OFF}(t) = \frac{v_{IN}(t) T_{ON}}{V_{OUT}} . \tag{1.25}$$

Since t_{OFF} is depending on $v_{IN}(t)$, it is not constant during a grid cycle. This also means that during a grid cycle the switching frequency, given by (1.26), will not be constant.

$$f_{SEPIC}(t) = \frac{1}{T_{ON}\left(1 + \frac{v_{IN}(t)}{V_{OUT}}\right)} = \frac{1}{\frac{\hat{I}_{PEAK} L_E}{\hat{V}_{IN}}\left(1 + \frac{v_{IN}(t)}{V_{OUT}}\right)} \tag{1.26}$$

3.1.2.2 Input current of the SEPIC PFC

In PFC applications the input current is a point of interest. In the SEPIC PFC the current through the switch is the sum of the inductor currents while the input current equals the current through L_A. This means the controller shapes the current through the switch and

not the input current. The switch will be turned off after the sum of both inductor currents has reached $i_{PEAK}(t)$ and after the sum of both inductors currents has becomes zero, which means there is no information of the separated inductor currents. In fact there is a shift, $i_{SHIFT}(t)$ between the inductor currents which satisfies the charge balance. This means that the total change of charge in the series capacitor C, during a high frequency cycle, must be zero. This condition is satisfied in equation (1.27)

$$\left(\Delta i_{L_B}(t) - i_{SHIFT}(t)\right)T_{ON} = \left(\Delta i_{L_A}(t) + i_{SHIFT}(t)\right)t_{OFF}(t). \qquad (1.27)$$

where $\Delta i_{L_A}(t)$ and $\Delta i_{L_B}(t)$ are changes of the average inductor currents during a high frequency cycle given by:

$$\Delta i_{L_A}(t) = \frac{v_{IN}(t)}{2L_A}T_{ON} \qquad (1.28)$$

$$\Delta i_{L_B}(t) = \frac{v_{IN}(t)}{2L_B}T_{ON}. \qquad (1.29)$$

By substituting (1.28) and (1.29) into (1.27), $i_{SHIFT}(t)$ can be written as function of the other variables (see for derivation Appendix B.1):

$$i_{SHIFT}(t) = \frac{v_{IN}(t)T_{ON}}{2}\left(\frac{V_{OUT}}{\left(V_{OUT} + v_{IN}(t)\right)L_B} - \frac{v_{IN}(t)}{\left(V_{OUT} + v_{IN}(t)\right)L_A}\right) \qquad (1.30)$$

The average input current can now be written as

$$i_{IN}(t) = \Delta i_{L_A}(t) + i_{SHIFT}(t). \qquad (1.31)$$

By substituting (1.28) into (1.31) and simplifying (appendix B.2) the average input current can be written as:

$$i_{IN}(t) = \hat{I}_{PEAK}\frac{\left|\sin(\varpi t)\right|}{2\left(1 + \frac{\hat{V}_{IN}\left|\sin(\varpi t)\right|}{V_{OUT}}\right)}. \qquad (1.32)$$

Equation (1.32) shows that the input current is not purely sinusoidal and that some harmonic distortion will occur, depending on the $\hat{V}_{IN}/V_{OUT}$ ratio. Because of this line distortion it is not possible to determine mean values for the input current (the "$\sqrt{2}$ ratio"). This makes power analysis and also the steady state analysis of $\hat{I}_{PEAK}$ a little bit more difficult. Assuming there are no losses is the PFC, the average input power must equal the average output power, thus $P_{IN} = P_{OUT}$. The average input power can be determined by

$$P_{IN} = \frac{1}{T}\int_0^T v_{IN}(t)i_{IN}(t)dt = \frac{4}{T}\int_0^{T/4} v_{IN}(t)i_{IN}(t)dt = \frac{\hat{V}_{IN}\hat{I}_{PEAK}}{\pi}\int_0^{\pi/2\varpi} \frac{\varpi \sin^2(\varpi t)}{\left(1+\frac{\hat{V}_{IN}|\sin(\varpi t)|}{V_{OUT}}\right)}dt = \frac{\hat{V}_{IN}\hat{I}_{PEAK}}{\pi}\mu(\hat{V}_{IN},V_{OUT}) \quad (1.33).$$

Where $\mu(\hat{V}_{IN},V_{OUT})$ is a non linear function which is derived in appendix B.3. The normalized $\mu(\hat{V}_{IN},V_{OUT})$ function is shown in Fig 3.5.

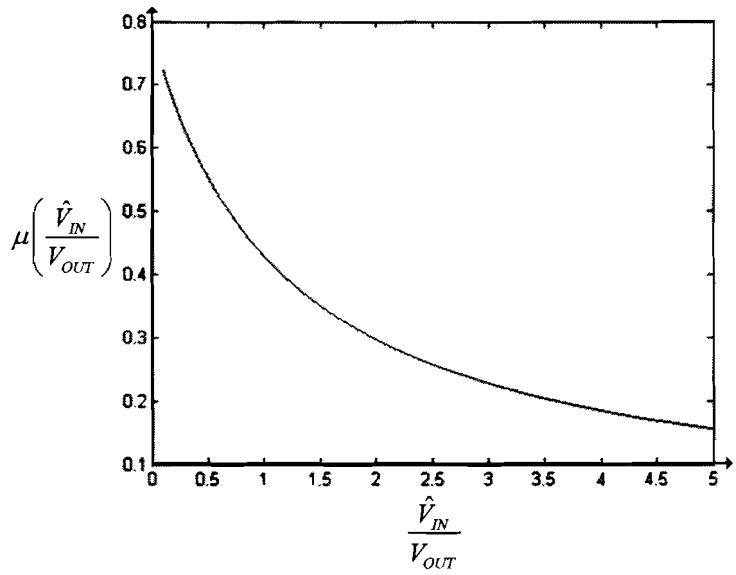


Figure 3.5, $\mu(\hat{V}_{IN},V_{OUT})$ function.

Now $\hat{I}_{PEAK}$ can be written as function of the output power:

$$\hat{I}_{PEAK} = \frac{P_{IN}\pi}{\hat{V}_{IN}\mu(\hat{V}_{IN},V_{OUT})} \quad (1.34)$$

3.2 SINGLE INDUCTOR BUCK BOOST

In this section the Single inductor Buck Boost (SiBB) converter will be discussed. A loss analysis of this converter is not done, however, it is thought valuable to do this analysis because of the similarity with the Low stress Buck Boost converter. First the converter will be introduced briefly for a constant input voltage, after that the Single inductor Buck Boost PFC will be discussed.

3.2.1 Single inductor buck boost converter

The Single inductor Buck Boost converter, shown in Fig 3.6, contains two switches. which means that four states can be formed.

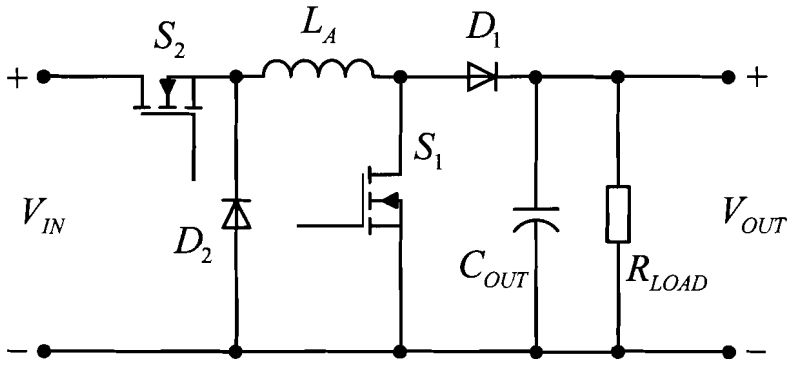


Figure 3.6, Single inductor Buck Boost converter.

In fact three modes can be defined, the boost mode, the buck mode and the buck boost mode. A boost converter is formed when the buck switch (S_2) is closed and the output voltage is controlled by the boost switch (S_2). When S_1 is opened, a buck circuit is formed which is controlled by S_1. However, there is a third mode, called the buck boost mode. In this mode the switches are turned off and on simultaneously. Since these three modes are well established topologies and are well discussed in literature [3], [4], their voltage transfer function will not be derived in this report. The voltage transfer functions for CCM (or BCM) of the three modes are.

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-\delta} \tag{1.35}$$

for the boost mode,

$$\frac{V_{OUT}}{V_{IN}} = \delta \tag{1.36}$$

for the buck mode and

$$\frac{V_{OUT}}{V_{IN}} = \frac{\delta}{1-\delta} \tag{1.37}$$

for the buck boost mode.

3.2.2 Single inductor buck boost as PFC

As mentioned in the previous section, the two switch Buck Boost topology can form three different modes. When applying the Buck Boost topology as PFC, this offers the possibility for different control strategies. If the amplitude of input voltage is higher than the output voltage, the PFC can always operate in buck boost mode. However, for the other two modes there are restrictions. Since the instantaneous input voltage can be higher or lower than the output voltage, the PFC has to switch to another mode within a line cycle. The controlling strategy for this case is shown in Fig 3.7.

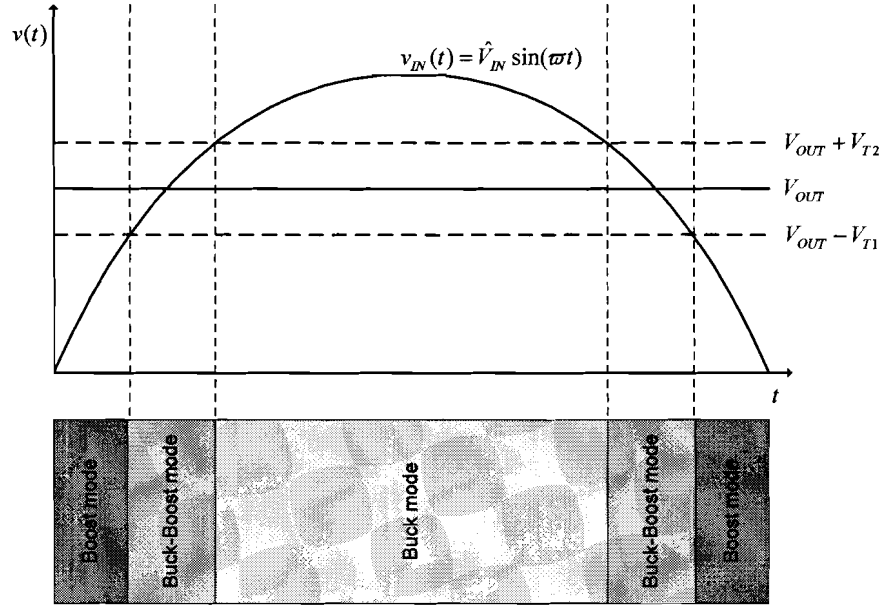


Figure 3.7, Single inductor Buck Boost converter.

When the PFC is operating in BCM, the switching frequency will decay to zero when the instantaneous input voltage reaches the output voltage. Since this will produce audible noise and cause problems with the input filter, this situation must be avoided. This can be done by introducing the buck boost mode when the instantaneous input voltage is near the output voltage, which is also shown in Fig 3.7. Operating in three modes during a grid cycle requires a more complex controlling circuit, this might raise the question why the PFC is not only operating in the buck boost mode. There are two arguments for that question, the first is that the buck boost operation leads into increased stresses, which will be seen later. The second argument is that this section is a introduction for the Low stress Buck Boost converter which can only operate in buck boost mode for a short time. Now the control strategy is introduced, the more detailed properties will be discussed in the next sections.

3.2.2.1 Boost mode of the Single inductor Buck Boost PFC

In the boost mode, the buck switch is continuously closed, which results in the simplified circuit shown in Fig 3.8.

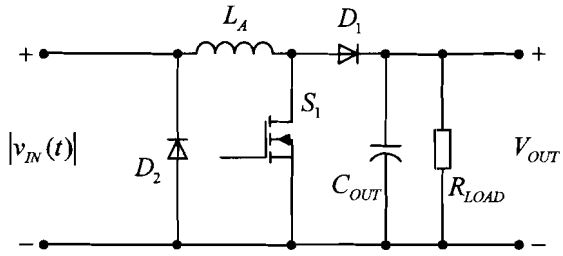


Figure 3.8, Single inductor Buck Boost PFC in boost mode.

The two different states of the PFC are shown in Fig 3.9.

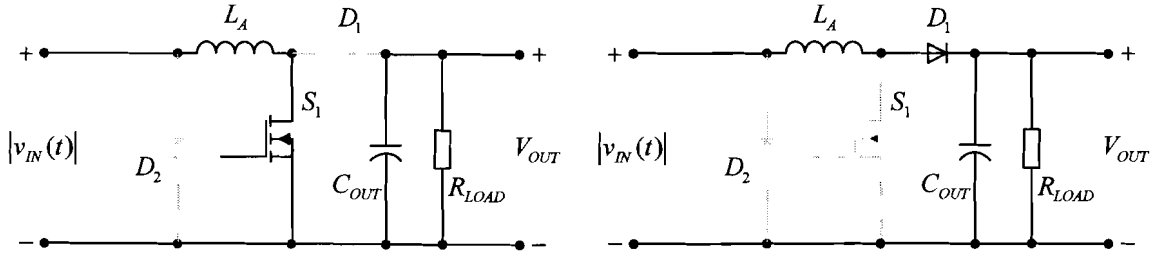


Figure 3.8, The two states of the Single inductor Buck Boost PFC in boost mode.

In the first state, the switch is closed and the inductor voltage will increase until the reference current, $i_{PEAK}(t)$, is reached. The inductor current can be written as:

$$i_{L_A} = \frac{v_{IN}(t)}{L_A} t \,. \tag{1.38}$$

After a time span T_{ON}, the reference current $i_{PEAK}(t)$ is reached. T_{ON} can be calculated by:

$$T_{ON} = \frac{L_A \hat{I}_{PEAK}}{\hat{V}_{IN}} \tag{1.39}$$

which is a constant.

When the switch is turned off the diode is conducting and the current through L_A will decrease from $i_{PEAK}(t)$ to zero. The current in the second stage is given by:

$$i_{L_A} = i_{PEAK}(t) + \frac{v_{IN}(t) - V_{OUT}}{L_A} t \qquad \text{for} \qquad v_{IN}(t) < V_{OUT} \,. \tag{1.40}$$

The time the current needs to become zero, which BCM is equal to the time the switch is turned off, is defined by $t_{OFF}(t)$ and is given by:

$$t_{OFF}(t) = \frac{|i_{PEAK}(t)|L_A}{V_{OUT} - |v_{IN}(t)|} \quad \text{for} \quad v_{IN}(t) < V_{OUT}. \tag{1.41}$$

By combining (1.39) and (1.41) it is easy to find the switching frequency

$$f_{BOOST}(t) = \frac{\hat{V}_{IN}\left(V_{OUT} - \hat{V}_{IN}|\sin(\varpi t)|\right)}{V_{OUT}L_A\hat{I}_{PEAK}} \quad \text{for} \quad v_{IN}(t) < V_{OUT}. \tag{1.42}$$

3.2.2.2 Buck mode of the Single inductor Buck Boost PFC

In the buck mode the boost switch is not used. The two states of the PFC in this situation are shown in Fig 3.9.

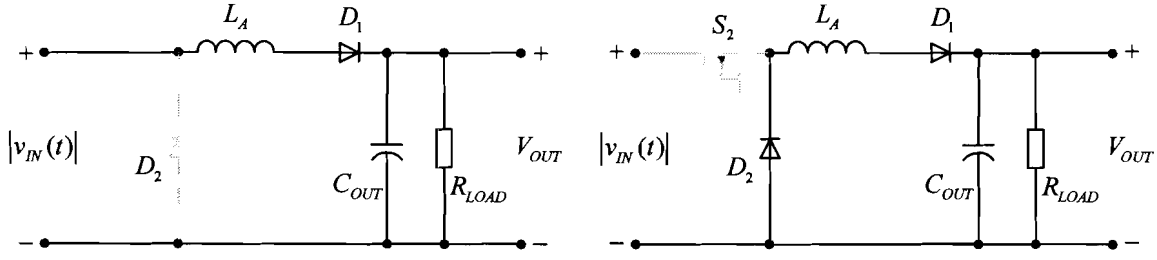


Figure 3.9, The two states of the Single inductor Buck Boost PFC in buck mode.

In the first states the switch is turned on until the $i_{PEAK}(t)$ is reached, in the second state the switch is turned off and the diode is conducting until the inductor current reaches zero. The current through the inductor for both situations is given by (1.43) and (1.44) respectively.

$$i_{L_A} = \frac{v_{IN}(t) - V_{OUT}}{L_A}t \quad \text{for} \quad V_{OUT} < v_{IN}(t) \tag{1.43}$$

$$i_{L_A} = i_{PEAK}(t) - \frac{V_{OUT}}{L_A}t \quad \text{for} \quad V_{OUT} < v_{IN}(t) \tag{1.44}$$

And the times the switch is turned on and off are respectively given by:

$$t_{ON}(t) = \frac{L_A\hat{I}_{PEAK}|\sin(\varpi t)|}{\hat{V}_{IN}|\sin(\varpi t)| - V_{OUT}} \quad \text{for} \quad V_{OUT} < v_{IN}(t) \tag{1.45}$$

and the off time:

$$t_{OFF}(t) = \frac{L_A \hat{I}_{PEAK} |\sin(\varpi t)|}{V_{OUT}} \qquad v_{IN}(t) > V_{OUT} . \tag{1.46}$$

The switching frequency can be found by combining the last two equations

$$f(t)_{BUCK} = \frac{V_{OUT}\left(\hat{V}_{IN} |\sin(\varpi t)| - V_{OUT}\right)}{L\hat{I}_{PEAK}\hat{V}_{IN} \sin^2(\varpi t)} \qquad v_{IN}(t) > V_{OUT} . \tag{1.47}$$

3.2.2.3 Buck boost mode of the Single inductor Buck Boost PFC

In the buck boost mode the two switches are turned on and turned off simultaneously. The two states are shown in Fig 3.10.

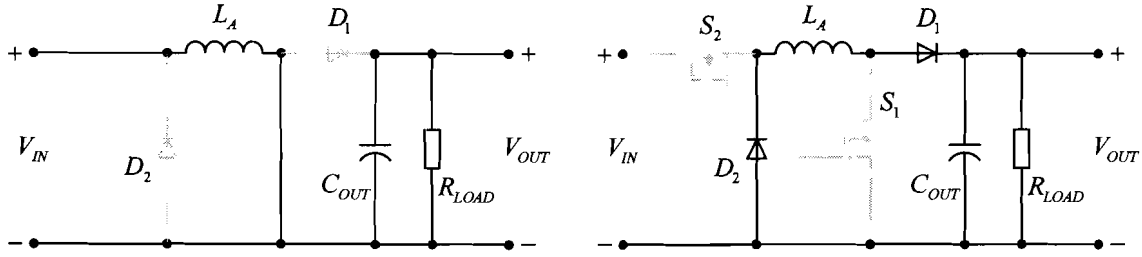


Figure 3.10, The two states of the Single inductor Buck Boost PFC in buck boost mode.

The currents the first and the second stage are given by (1.48) and (1.49) for respectively

$$i_{L_A} = \frac{v_{IN}(t)}{L_A} t \tag{1.48}$$

$$i_{L_A} = i_{PEAK}(t) - \frac{V_{OUT}}{L_A} t . \tag{1.49}$$

And the times the switch off and on, T_{ON} and $t_{OFF}(t)$ are respectively given by

$$T_{ON} = \frac{L_A \hat{I}_{PEAK}}{\hat{V}_{IN}} \tag{1.50}$$

$$t_{OFF}(t) = \frac{L_A \hat{I}_{PEAK} |\sin(\varpi t)|}{V_{OUT}}. \tag{1.51}$$

The switching frequency can be determined by combining (1.50) and (1.51):

$$f_{BUCKBOOST}(t) = \frac{V_{OUT}\hat{V}_{IN}}{L_A \hat{I}_{PEAK}(V_{OUT} + \hat{V}_{IN}|\sin(\varpi t)|)} \tag{1.52}$$

3.2.2.4 High frequency cycles

The SEPIC and Boost PFC both have a continuous input current, this implicates that the input current is not zero at the moment the diode is conducting. A high frequency cycle of the input current of the boost PFC is shown in Fig 3.11.

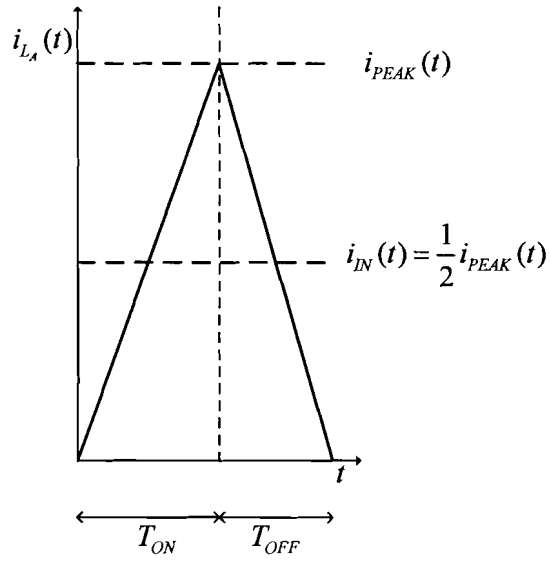


Figure 3.11, High frequency cycle of the Boost PFC.

It is easy to conclude that the average input current of the Boost PFC equals one half of the reference current ($i_{PEAK}(t)$) and the input current will be perfectly proportional with the reference current. However, when operating in the buck or buck boost mode the input current is not continuous. Both high frequency cycles are shown in Fig 3.12.

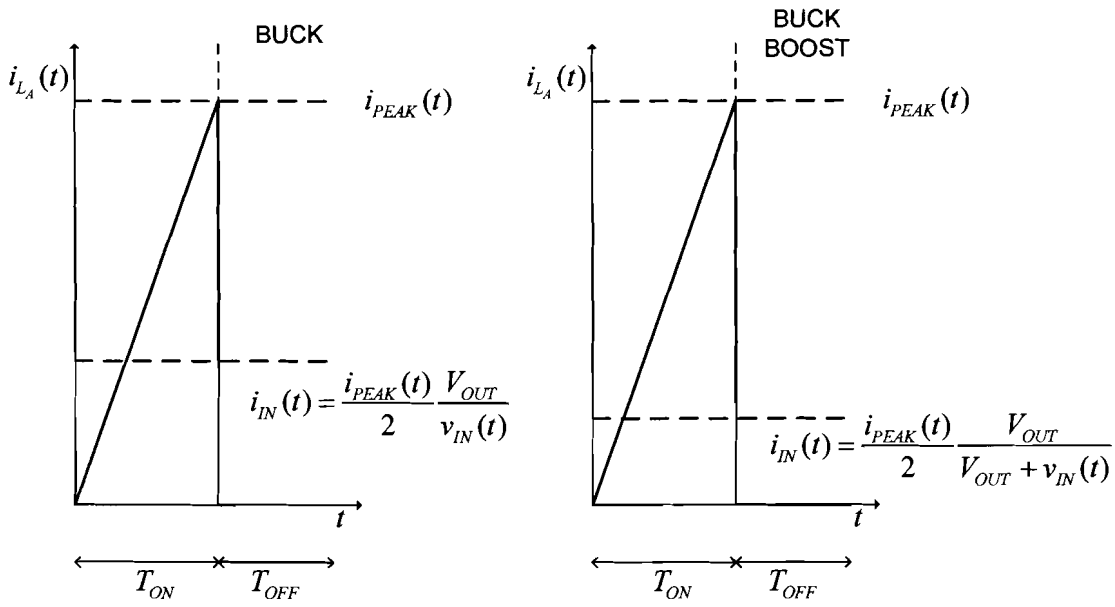


Figure 3.12, High frequency cycle in the Buck and a Buck Boost mode.

From Fig 3.12 it can be concluded the average input current is not proportional related with $i_{PEAK}(t)$, this introduces harmonic distortion and will force the controller to increase the amplitude of the reference current (I_{PEAK}) to maintain the output voltage.

3.2.2.5 Average input current for the different modes

As mentioned in the previous section, the energy transfer in the buck and buck-boost mode is lower than in the boost mode. This will force the controller to increase the reference current, which will be determined in the next section. For determining the reference current it is necessary to know the average input current in the different modes, which will be determined in this section.

The average input current during a high frequency cycle can be determined by:

$$i_{IN}(t) = \frac{1}{T}\int_0^T i(t)dt \qquad (1.53)$$

In the case of the boost mode, it is already known that the average input current equals half the reference current thus $i_{IN_{BOOST}}(t) = i_{PEAK}(t)/2$. For the buck boost mode and buck mode however, the average current is not known. In the case of the buck boost mode, there is only an input current during the interval T_{ON}, thus (1.53) can be written as:

$$i_{IN_{BUCKBOOST}}(t) = \frac{1}{T_{ON}+t_{OFF}(t)}\int_0^{T_{ON}} i_{L_A}(t)dt = \frac{1}{T_{ON}+t_{OFF}(t)}\int_0^{T_{ON}} \frac{v_{IN}(t)}{L_A}tdt\,. \qquad (1.54)$$

Since $t_{OFF}(t)$, $v_{IN}(t)$ and $i_{PEAK}(t)$ may be considered constant during a high frequency cycle and by substituting (1.50) and (1.51), (1.54) becomes:

$$i_{IN_{BUCKBOOST}}(t) = \frac{T_{ON}}{T_{ON} + t_{OFF}(t)} \frac{v_{IN}(t)}{2L_A} = \frac{\left(\frac{L_A \hat{I}_{PEAK}}{\hat{V}_{IN}}\right)^2}{\frac{L_A \hat{I}_{PEAK}}{\hat{V}_{IN}} + \frac{L_A \hat{I}_{PEAK} |\sin(\varpi t)|}{V_{OUT}}} \frac{v_{IN}(t)}{L_A} = \frac{i_{PEAK}(t)}{2} \frac{V_{OUT}}{V_{OUT} + v_{IN}(t)} \tag{1.55}$$

This means that the average current in the buck boost mode is a factor $V_{OUT} / \left(V_{OUT} + v_{IN}(t)\right)$ lower than in with the boost mode.

The average input current for the buck mode can be found in the same manner as for the buck boost mode. Substituting (1.43) into (1.54) gives:

$$i_{IN_{BUCK}}(t) = \frac{1}{T} \int_0^T i(t)dt = \frac{1}{t_{ON}(t) + t_{OFF}(t)} \int_0^{t_{ON}(t)+t_{OFF}(t)} \frac{v_{IN}(t) - V_{OUT}}{L_A} tdt = \frac{t_{ON}^2(t)}{t_{ON}(t) + t_{OFF}(t)} \frac{v_{IN}(t) - V_{OUT}}{2L_A} \tag{1.56}$$

And substituting $t_{ON}(t)$ and $t_{OFF}(t)$ (respectively (1.45) and (1.46)) into (1.56) gives:

$$i_{IN_{BUCK}}(t) = \frac{\left(\frac{L_A \hat{I}_{PEAK} |\sin(\varpi t)|}{\hat{V}_{IN} |\sin(\varpi t)| - V_{OUT}}\right)^2}{\frac{L_A \hat{I}_{PEAK} |\sin(\varpi t)|}{\hat{V}_{IN} |\sin(\varpi t)| - V_{OUT}} + \frac{L_A \hat{I}_{PEAK} |\sin(\varpi t)|}{V_{OUT}}} \frac{v_{IN}(t) - V_{OUT}}{2L_A} = i_{IN}(t) = \frac{i_{PEAK}(t)}{2} \frac{V_{OUT}}{v_{IN}(t)} . \tag{1.57}$$

Table 3.1 shows the reducing factor of the current for the different modes:

Mode	Reducing factor
Boost	2
Buck Boost	$2\frac{V_{OUT} + v_{IN}(t)}{V_{OUT}}$
Buck	$2\frac{v_{IN}(t)}{V_{OUT}}$

Table 3.1 Reducing factor of the input current for the different modes

3.2.2.6 Steady state reference current for the Buck Boost PFC

In the previous section the average input current for the different modes is determined, in this section the amplitude of the reference current for the steady state situation will be determined.

In steady state situation, the input power must equal the output power (assuming there are no losses in the PFC). Even when operating in different modes, this condition must be satisfied, thus, in terms of energy:

$$E_{IN} = E_{IN_{BOOST}} + E_{IN_{BUCKBOOST}} + E_{IN_{BUCK}} = E_{OUT}\,. \tag{1.58}$$

This is illustrated in Fig. 3.13 (note that Fig. 3.13 is only an illustration, the actual input power is different).

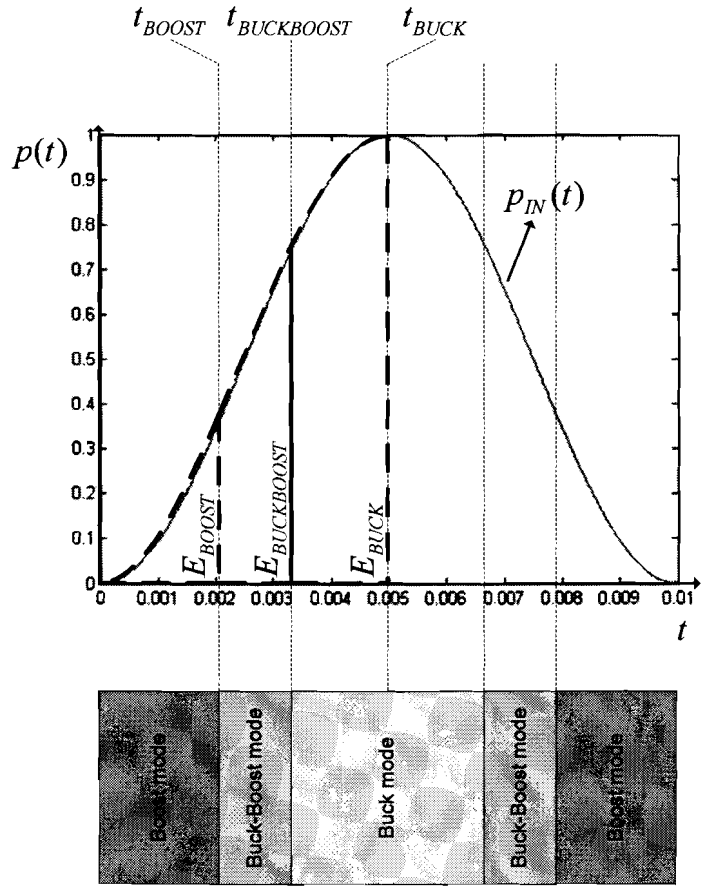


Figure 3.13, Instantaneous input power and input energy for the different modes.

In steady state condition the input power is time-dependent, because both the input voltage and input current are sinusoidal. Since there is only a small ripple on the output voltage, the output voltage will be considered constant.

In the previous section the average input currents are determined, with this information it is possible to determine the energy transferred in the different modes. In general the equation for transferred energy is given by:

$$E_{IN} = \int_T p_{IN}(t)dt = \int_T v_{IN}(t)i_{IN}(t)dt \,. \tag{1.59}$$

The energy transferred in the boost mode equals:

$$E_{IN_{BOOST}} = \int_0^{t_{BOOST}} v_{IN}(t)i_{IN_{BOOST}}(t)dt = \frac{1}{2}\int_0^{t_{BOOST}} v_{IN}(t)i_{PEAK}(t)dt = \frac{\hat{I}_{PEAK}\hat{V}_{IN}}{2}\int_0^{t_{BOOST}} \sin^2(\varpi t)dt \,. \tag{1.60}$$

Solving (1.60) gives:

$$E_{IN_{BOOST}} = \frac{\hat{V}_{IN}\hat{I}_{PEAK}}{4\varpi}\left(\int_0^{\varpi t_{BOOST}} 1du - \int_0^{\varpi t_{BOOST}} \cos(2u)du\right) = \frac{\hat{V}_{IN}\hat{I}_{PEAK}t_{BOOST}}{4} - \frac{\hat{V}_{IN}\hat{I}_{PEAK}}{8\varpi}\sin(2\varpi t_{BOOST}) \,. \tag{1.61}$$

In the buck boost mode (1.59) becomes:

$$E_{IN_{BUCKBOOST}} = \int_{t_{BOOST}}^{t_{BUCKBOOST}} v_{IN}(t)i_{IN_{BUCKBOOST}}(t)dt = \frac{\hat{I}_{PEAK}\hat{V}_{IN}V_{OUT}}{2}\int_{t_{BOOST}}^{t_{BUCKBOOST}} \frac{\sin^2(\varpi t)}{V_{OUT} + \hat{V}_{IN}\sin(\varpi t)}dt \tag{1.62}$$

by substituting $u = \varpi t$ (1.62) becomes:

$$E_{IN_{BUCKBOOST}} = \frac{V_{OUT}\hat{V}_{IN}\hat{I}_{PEAK}}{2\varpi}\overbrace{\int_{\varpi t_{BOOST}}^{\varpi t_{BUCK}} \frac{\sin^2(u)}{V_{OUT} + \hat{V}_{IN}\sin(u)}du}^{\lambda} \tag{1.63}$$

which can be written as:

$$E_{IN_{BUCKBOOST}} = \frac{V_{OUT}\hat{V}_{IN}\hat{I}_{PEAK}}{2\varpi}\lambda \,. \tag{1.64}$$

For derivation of λ see appendix B.4.

For the buck mode the energy transfer equals:

$$E_{IN_{BUCK}} = \int_{t_{BUCKBOOST}}^{t_{BUCK}} v_{IN}(t)i_{IN_{BUCK}}(t)dt = \frac{V_{OUT}\hat{I}_{PEAK}}{2}\int_{t_{BUCKBOOST}}^{t_{BUCK}} \sin(\varpi t)dt \,. \tag{1.65}$$

Solving (1.65) and substituting $t_{BUCK} = \pi/(2\varpi)$ gives:

$$E_{IN_{BUCK}} = \frac{V_{OUT}\hat{I}_{PEAK}}{2\omega}\int_{\varpi t_{BUCKBOOST}}^{\frac{\pi}{2}} \sin(u)du = \frac{V_{OUT}\hat{I}_{PEAK}}{2\varpi}\cos(\varpi t_{BUCKBOOST}). \quad (1.66)$$

Now the energy transfer for the different modes is known, the delivered energy at the output must be determined. Since it is assumed the output power is constant, it is easy to determine the delivered energy during one fourth grid period ($\pi/(2\varpi)$).

$$E_{OUT} = \int_0^{t_{BUCK}} P_{OUT}dt = \int_0^{\pi/(2\varpi)} P_{OUT}dt = \frac{\pi}{2\varpi}P_{OUT} \quad (1.67)$$

Applying (1.58) gives:

$$\frac{P_{OUT}\pi}{2\varpi} = E_{IN_{BOOST}} + E_{IN_{BUCK}} + E_{IN_{BUCKBOOST}} \quad (1.68)$$

By substituting the energies for the different modes into (1.68) it is possible to express $\hat{I}_{PEAK}$ as function of the other parameters:

$$\hat{I}_{PEAK} = \frac{4P_{OUT}\pi}{\left(2\hat{V}_{IN}\varpi t_{BOOST} - \hat{V}_{IN}\sin(2\varpi t_{BOOST}) + 4V_{OUT}\cos(\varpi t_{BUCKBOOST}) + 4V_{OUT}\hat{V}_{IN}\lambda\right)} \quad (1.69)$$

When it is considered the converter is only operating in boost mode, thus $\hat{V}_{IN} < V_{OUT}$, then $t_{BUCKBOOST} = t_{BOOST} = \pi/(2\varpi)$. Substituting these values into (1.69) gives:

$$\hat{I}_{PEAK} = \frac{4P_{OUT}}{\hat{V}_{IN}}. \quad (1.70)$$

Which is exactly the same equation as for the boost PFC.

3.3 LOW STRESS BUCK BOOST

In this section the Low stress Buck Boost topology will be discussed. Since the Low stress Buck Boost topology has its similarities with the Buck Boost topology some parts of the analysis will be discussed only briefly.

3.3.1 Low stress Buck Boost converter

The Low stress Buck Boost converter contains two inductors, two diodes, two switches and one series capacitor as shown in Fig 3.14.

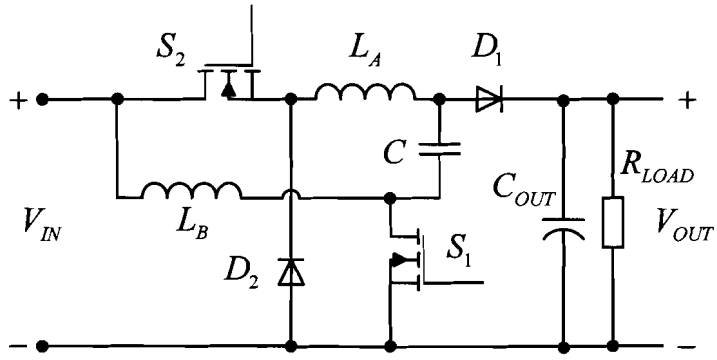


Figure 3.14, Low stress Buck Boost converter.

When operating in the boost mode, the buck switch S_2 is closed and the converter can be simplified as shown in Fig 3.15.

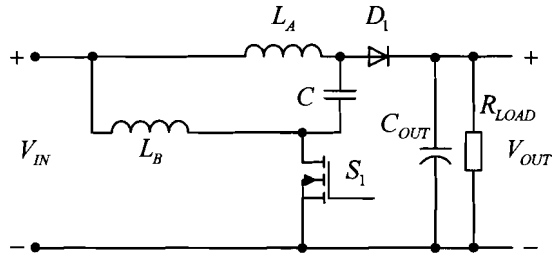


Figure 3.15, Low stress Buck Boost converter in boost mode.

In the first stage the switch is closed, as shown in the left hand picture of Fig 3.16. In this case the current through the switch equals the sum of the inductor currents. In this stage the series capacitor C will be charged with a certain amount of energy because it is connected in series with inductor L_A.

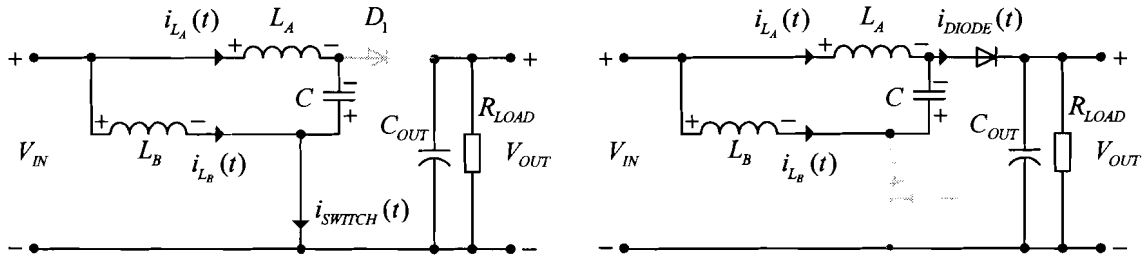


Figure 3.16, Two stages of the Low stress Buck Boost converter in boost mode.

In the second stage, S_1 will be opened and the diode D_1 will conduct. In this stage the C is connected in series with L_B and a certain amount of energy will be taken out of C making the average voltage across C zero. This means that the boost mode of the Low stress Buck Boost converter has the same functionality and voltage transfer as a normal Boost converter, for CCM (or BCM) the voltage transfer equals:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1-\delta} \tag{1.71}$$

In the buck mode the boost switch S_1 is opened and the converter is operated by the buck switch only (S_2) and a filter is formed between the input and the output by the series capacitor and L_B. The equivalent circuit for this situation is shown in Fig. 3.17.

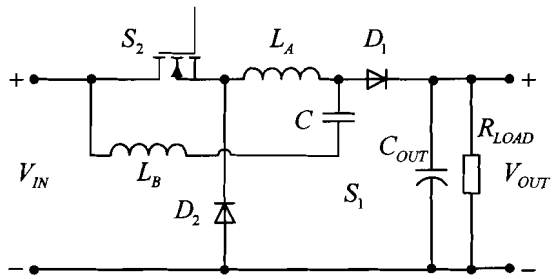


Figure 3.17, Low stress Buck Boost converter in buck mode.

When neglecting the effect of the filter, a real buck converter is formed. With voltage transfer function

$$\frac{V_{OUT}}{V_{IN}} = \delta \tag{1.72}$$

under CCM or BCM conditions.

3.3.2 Low stress Buck Boost converter as PFC

In this section the Low stress Buck Boost converter applied as a PFC will be analyzed. This PFC will be controlled in the same way as the Single inductor Buck Boost PFC and since the modes (except the buck boost mode) are similar, the analysis will be brief. A analysis of the Low stress Buck Boost converter in continuous conduction mode can be found in [5], [6].

3.3.2.1 Boost mode of the Low stress Buck Boost PFC

In the boost mode the switch is closed and the switch current is increasing, which is given by:

$$i_{SWITCH}(t) = i_{L_A}(t) + i_{L_B}(t) = \frac{|v_{IN}(t)|}{L_E} t \qquad (1.73)$$

where $L_E = L_A // L_B$. At $t = T_{ON}$, the reference current $i_{PEAK}(t)$ is reached and the switch is turned off. The current will now flow through the diode which stops conducting after the diode current has become zero at $t = T_{OFF}$.

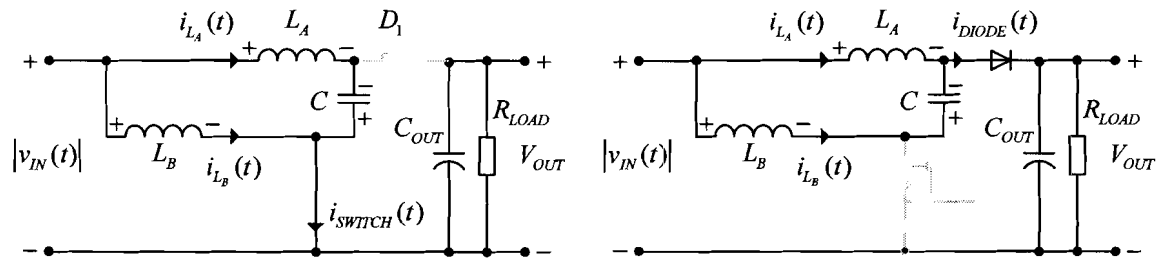


Figure 3.18, Low stress Buck Boost PFC in boost mode.

$$i_{DIODE}(t) = i_{L_A}(t) + i_{L_B}(t) = i_{PEAK}(t) + \frac{|v_{IN}(t)| - V_{OUT}}{L_E} t \qquad \text{for} \qquad |v_{IN}(t)| < V_{OUT} \qquad (1.74)$$

The intervals that the switch is turned on and off can be found in a similar way as done for the Single inductor Buck Boost PFC. By determining this intervals, the switching frequency for the boost mode can be calculated, which equals:

$$f_{BOOST}(t) = \frac{V_{OUT}\hat{V}_{IN}}{L_E \hat{I}_{PEAK}(V_{OUT} + \hat{V}_{IN}|\sin(\varpi t)|)} \qquad (1.75)$$

3.3.2.2 Buck mode of the Low stress Buck Boost PFC

When neglecting the effect of the series connection of L_A and C the buck mode of the Low stress Buck Boost PFC exactly matches the buck mode of the Single inductor Buck Boost PFC. So the properties can be found in section 3.2.2.2.

3.3.2.3 Buck boost mode of the Low stress Buck Boost PFC

When the rectified instantaneous input voltage $|v_{IN}(t)|$ reaches the output voltage V_{OUT}, the switching frequencies become very low, so it is necessary to introduce a third mode:

the buck boost mode. Although it is possible to operate the Low stress Buck Boost converter in the buck boost mode this has its drawbacks which will be discussed later.

When operating in buck boost mode, the switches are turned on and off simultaneously. The situation when both switches are turned on is shown on the left hand side of Fig 3.19. After the reference current is reached, both switches will be turned off and the right hand situation of Fig 3.19 appears.

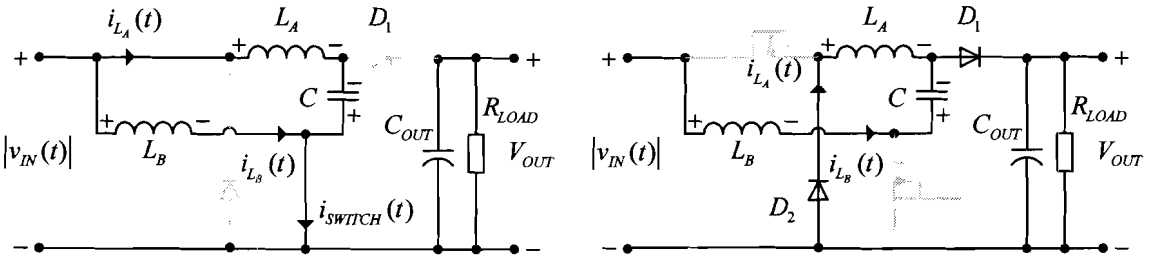


Figure 3.19, Low stress Buck Boost PFC in the buck boost mode.

When operating in the boost mode, the average voltage across the series capacitor is zero. The ripple across it is assumed a few volts. Thus when the PFC is in the right hand situation of Fig 3.19, the current through L_A will decay to zero much faster than the current through L_B because the voltage across L_A is much higher than the voltage across L_B. This implicates that diode D_2 will block earlier than D_1 which is shown in the left hand situation of Fig 3.20. (The right hand situation shows the situation with two blocking diodes).

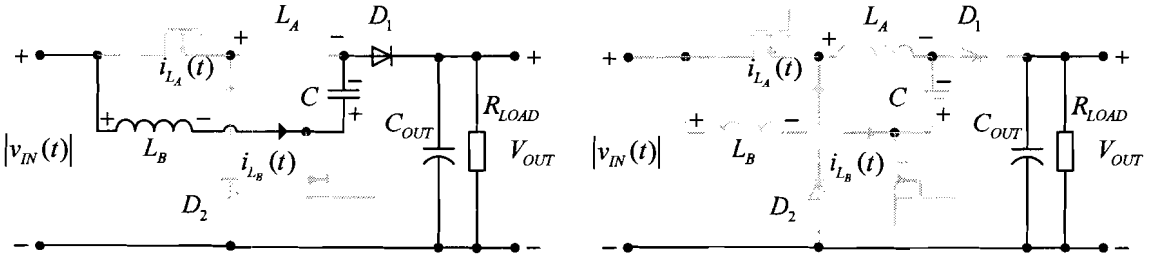


Figure 3.20, Low stress Buck Boost PFC in the buck boost mode.

For gaining more insight in the buck boost mode the waveforms are shown in Fig 3.21

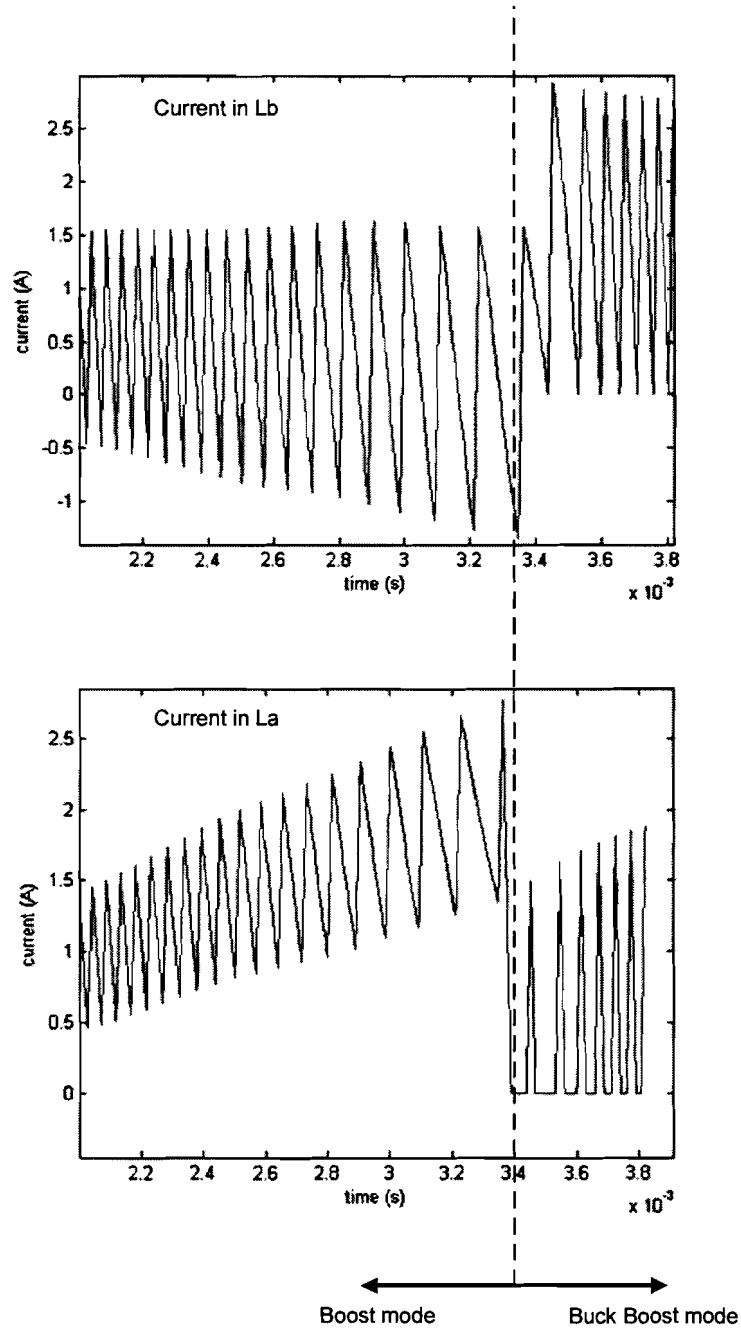


Figure 3.21, Inductor currents at changing mode.

Fig. 3.21 shows the inductor currents when changing mode. Since D_2 will block earlier than D_1, the current through L_A becomes discontinuous because switches are turned on again when the current through L_B has become zero too. The current through to the sum of the inductor currents is shown in Fig. 3.22.

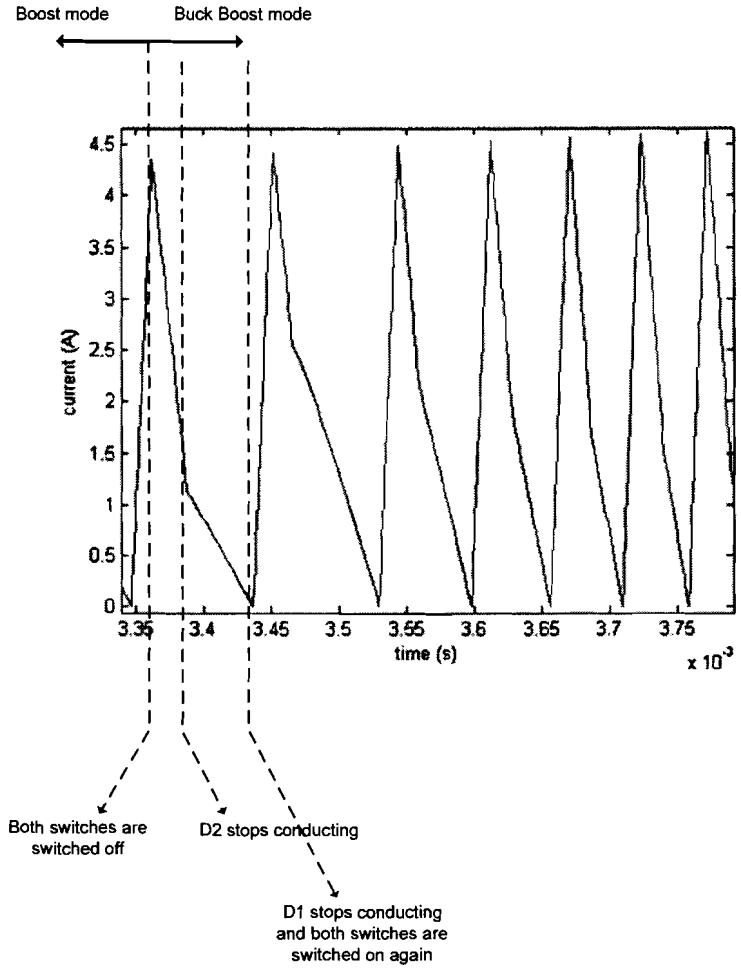


Figure 3.22, Sum of the inductor currents.

A disadvantage of applying buck boost mode for the Low stress Buck Boost PFC is that the series capacitor will be charged, because the charge balance must be satisfied. Fig 3.23 shows the increase of the capacitor voltage in this mode. When the Buck Boost mode ends, the buck mode starts and the capacitor will be discharged. This will lead into a large transient, which will be discussed later.

Now the functionality of the buck boost mode is known, this mode will be analyzed. During the first stage of the buck boost mode, both switches are turned on and the current through the switch starts increasing from zero:

$$i_{SWITCH}(t) = i_{L_A}(t) + i_{L_B}(t) = \frac{v_{IN}(t) + v_C(t)}{L_A} t + \frac{v_{IN}(t)}{L_B} t \qquad (1.76)$$

Where $v_C(t)$ is the voltage across the series capacitor. Assuming the inductors ($L_A = L_B = L$) are equal and $v_C(t)$ is constant during a high frequency cycle. The time needed to reach the reference current equals:

$$t_{ON}(t) = \frac{i_{PEAK}(t)L}{2v_{IN}(t) + v_C(t)}. \tag{1.77}$$

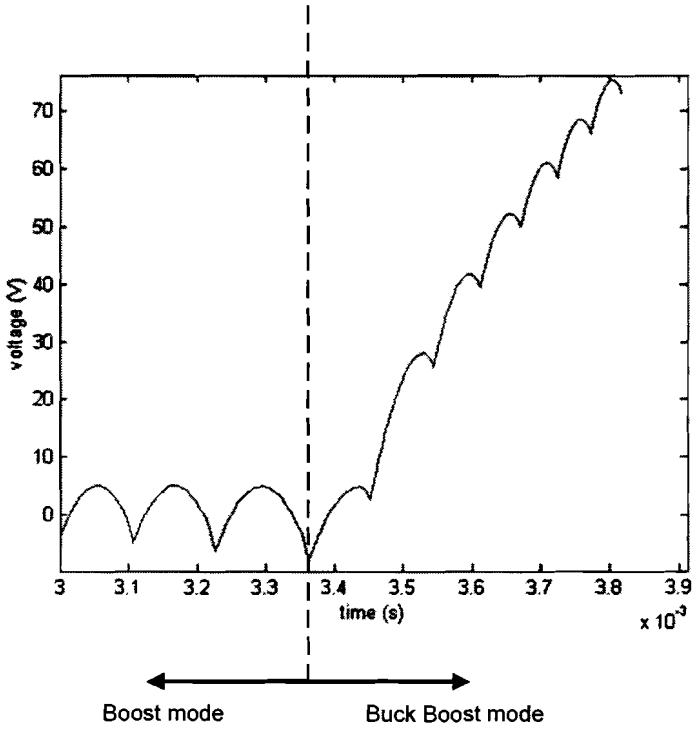


Figure 3.23, Voltage across the series capacitor.

After turning off the switch the current through the inductors will decay to zero, the time needed for becoming zero equals:

$$t_{OFF}(t) = \frac{-v_{IN}(t)T_{ON}}{v_{IN}(t) - (V_{OUT} + v_C(t))}. \tag{1.78}$$

There will be the steady state condition when the average voltage across the capacitor during a high frequency cycle is zero. When the switch is closed, the voltage across the capacitor decreases with:

$$\Delta v_C(t)_{ON} = -\frac{v_{IN}(t) + v_C(t)}{2LC}\left(\frac{I_{PEAK}L}{2v_{IN}(t) + v_C(t)}\right)^2. \tag{1.79}$$

When the switch is turned off, the voltage across the capacitor increases with:

$$\Delta v_C(t)_{OFF} = -\frac{v_{IN}(t)}{LC}\left(\frac{I_{PEAK}L}{2v_{IN}(t) + v_C(t)}\right)\left(\frac{-v_{IN}(t)T_{ON}}{v_{IN}(t) - (V_{OUT} + v_C(t))}\right) - \frac{v_{IN}(t) - (V_{OUT} + v_C(t))}{2LC}\left(\frac{-v_{IN}(t)T_{ON}}{v_{IN}(t) - (V_{OUT} + v_C}\right)$$

. (1.80)

Under steady state conditions the average voltage difference across the capacitor during a high frequency cycle must be zero. This implicates that:

$$\Delta v_C(t)_{ON} + \Delta v_C(t)_{OFF} = 0 . \tag{1.81}$$

When substituting (1.79) and (1.80) into (1.81), the voltage across the capacitor can be expressed as function of the other parameters:

$$v_C(t) = \frac{-V_{OUT} + \sqrt{V_{OUT}^2 + 8v_{IN}^2(t) - 4V_{OUT}v_{IN}(t)}}{2} . \tag{1.82}$$

During the buck boost mode the input voltage approximately equals the output voltage, thus $v_{IN}(t) \approx V_{OUT}$. The steady state voltage across the capacitor can thus be approximated by:

$$v_C(t) \approx \frac{V_{OUT}\left(\sqrt{5}-1\right)}{2} . \tag{1.83}$$

At the end of the buck mode the PFC starts operating in the buck mode, at this moment the series connection of the inductor L_B and C should function as a low pass filter between the input and output as shown in Fig 3.14.

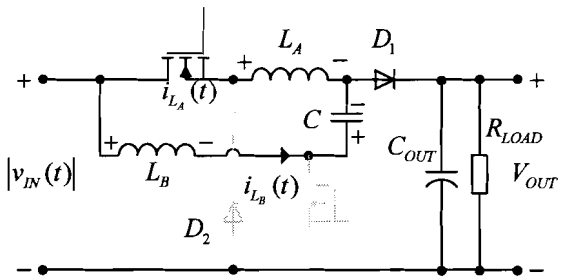


Figure 3.24, Buck situation of the LsBB PFC.

When the switch is closed the voltage across L_A equals $|v_{IN}(t)| - V_{OUT}$. The voltage across L_B, however, equals $|v_{IN}(t)| - (V_{OUT} + v_C(t))$. This voltage difference will be undone by the system and the capacitor will discharge leading in a resonating transient (between C and L_B). Since the PFC is operating in buck mode, the current through L_A is controlled and the transient can not flow entirely through L_A; it will also flow to the input, back into the grid. This will lead into a distorted line current and might also cause problems with the input filter.

3.3.2.4 Switching analysis of the Low stress Buck Boost PFC

In this section the switching characteristics of the switches of the Low stress Buck Boost PFC will be analyzed. MOSFETs (and also other semiconductor switches) are usually containing a parallel parasitic capacitor which can influence the behavior of the PFC's efficiency in a negative way. A simplified model of a MOSFET is shown in Fig. 3.25.

Figure 3.25, Simplified switch.

The LsBB PFC contains two switches, a buck and a boost switch. Both switches will be discussed.

3.3.2.4.1 Switching analysis of the buck switch

In the buck mode the circuit can be simplified as shown below:

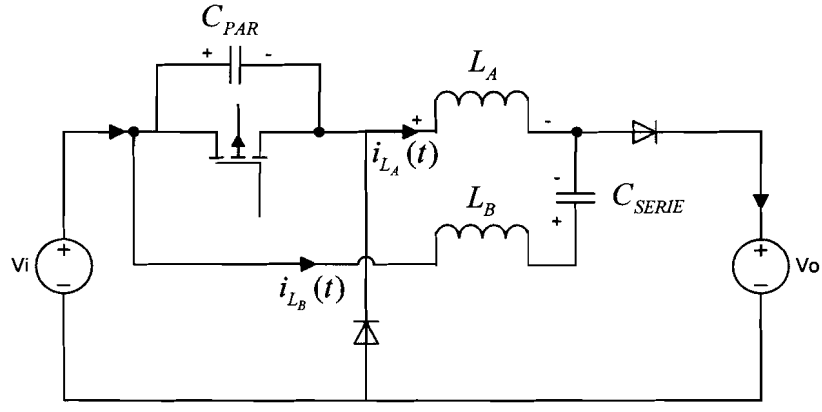


Figure 3.26, Low stress Buck Boost PFC during buck mode.

When the switch is turned on, the current through the inductor (and switch) will increase linearly until the reference current is reached at $t = T_{OFF}$ This situation is shown in Fig. 3.27. At $t = T_{OFF}$ the switch will be turned of and the diodes start conducting, this is shown in Fig 3.28. When the current through the diodes reaches zero, the diodes will block and a resonant path will appear, as shown in Fig. 3.29.

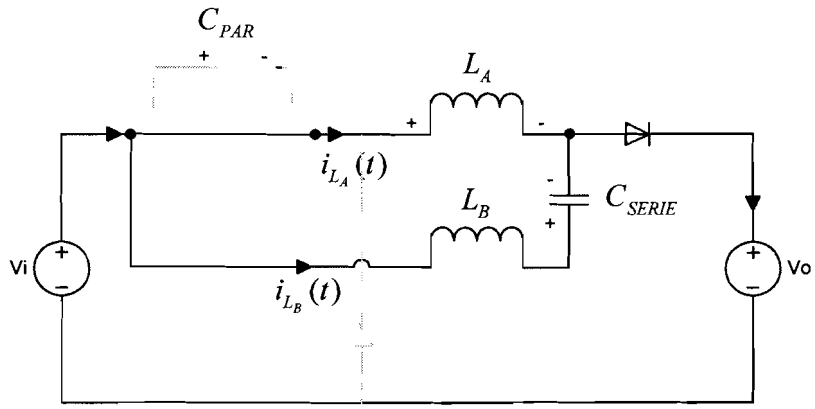


Figure 3.27, Low stress Buck Boost PFC during buck mode with closed switch, the current through the inductor L_A is increasing linearly.

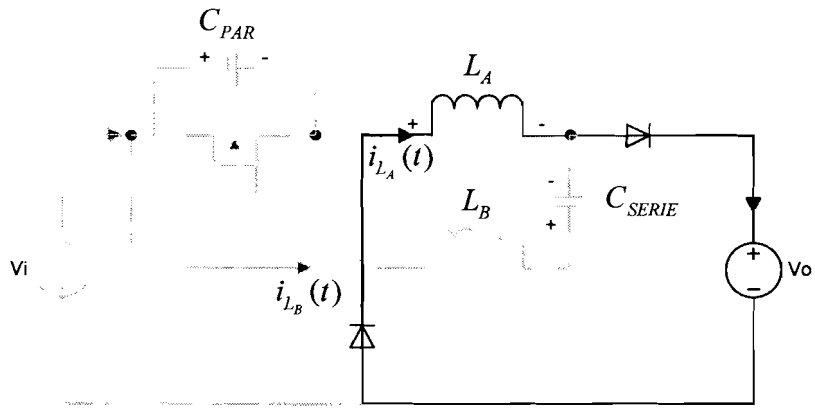


Figure 3.28, Low stress Buck Boost PFC during buck mode with conducting diodes, the current through the inductor L_A is decreasing linearly.

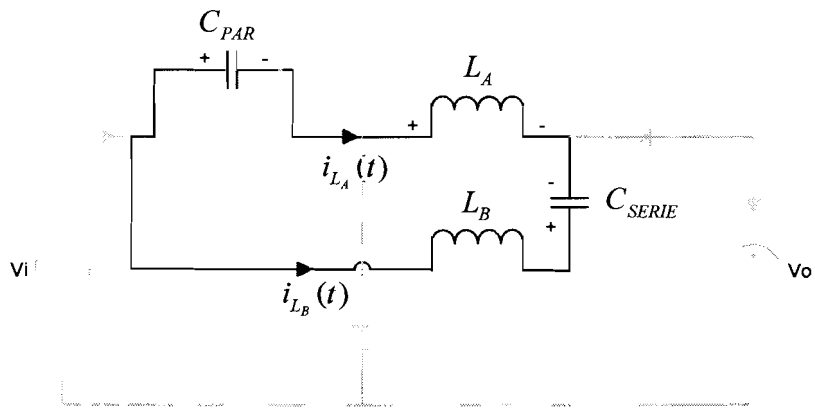


Figure 3.29, Low stress Buck Boost PFC during buck mode with resonating path

When the diode current has become zero a resonating path is formed. Assuming the capacitor $C_{SERIE} >> C_{PAR}$, the general solution of the inductor current $i_{L_A}(t)$ equals:

$$i_{L_A}(t) = A\cos(\varpi_0 t) + B\sin(\varpi_0 t) \tag{1.84}$$

where:

$$\varpi_0 = \frac{1}{\sqrt{C_{PAR} L_E}} \tag{1.85}$$

and

$$L_E = L_A + L_B . \tag{1.86}$$

Defining the moment that the diode current becomes zero as $t = 0$ and substituting the initial conditions;

$$\begin{cases} i_{L_A}(0) = 0 \\ \dfrac{di_{L_A}(0)}{dt} = \dfrac{-V_{OUT}}{L_A} \end{cases} \tag{1.87}$$

into (1.84) gives:

$$i_{L_A}(t) = \frac{-V_{OUT}}{L_E \varpi_0}\sin(\varpi_0 t) . \tag{1.88}$$

The voltage across the inductor L_A is given by

$$v_{L_A}(t) = -\frac{L_A V_{OUT}}{L_E}\cos(\varpi_0 t) . \tag{1.89}$$

And the voltage across the capacitor C_{PAR} equals

$$v_{C_{PAR}}(t) = V_{OUT}\cos(\varpi_0 t) . \tag{1.90}$$

When $\varpi_0 t = \pi/2$ the voltage across the inductor is zero and current detection is triggered but the voltage across the switch is not at its lowest point yet. Switching on at this time would not be the best moment. At the same moment the voltage at the node between L_A and C_{PAR} now equals the output voltage and the diode will starts conducting again. A new resonating circuit is formed as shown in Fig. 3.30.

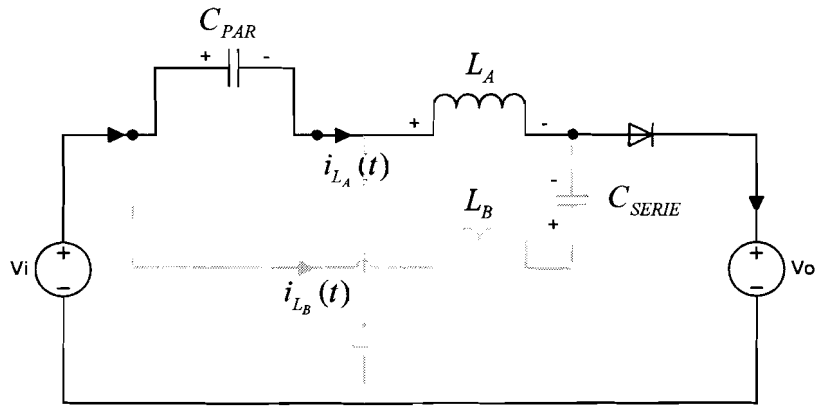


Figure 3.30, Low stress Buck Boost PFC during buck mode in second resonant cycle.

Defining the moment the zero current detection is triggered as $T_{ZCD} = \pi/(2\varpi_0)$, the initial conditions for this circuit are:

$$i_{L_A}(T_{ZCD}) = \frac{-V_{OUT}}{L_E \varpi_0} \tag{1.91}$$

$$v_{L_A}(T_{ZCD}) = 0\,. \tag{1.92}$$

Applying the initial conditions gives:

$$i_{L_A}(t) = \frac{-V_{OUT}}{L_E \varpi_0}\cos(\varpi_1(t - T_{ZCD})) \tag{1.93}$$

$$v_{L_A}(t) = V_{OUT}\frac{L_A \varpi_1}{L_E \varpi_0}\sin(\varpi_1(t - T_{ZCD})) = V_{OUT}\sqrt{\frac{L_A}{L_E}}\sin(\varpi_1(t - T_{ZCD})) \tag{1.94}$$

with

$$\varpi_1 = \frac{1}{\sqrt{C_{PAR} L_A}}\,. \tag{1.95}$$

The voltage across C_{PAR} equals now:

$$v_{C_{PAR}}(t) = v_{IN}(t) - V_{OUT}\left(1 + \sqrt{\frac{L_A}{L_E}}\sin(\varpi_1(t - T_{ZCD}))\right). \tag{1.96}$$

In order to reduce the switching losses as much as possible, the switch must be switched on when $v_{C_{PAR}}(t)$ reaches its minimum, this is at $t = \pi/(2\varpi_1) + T_{ZCD} = T_{SWITCHON}$. In Fig. 3.31

and 3.32 the waveforms of the current through the inductor L_A and the voltage across the capacitor during the switch transition are shown.

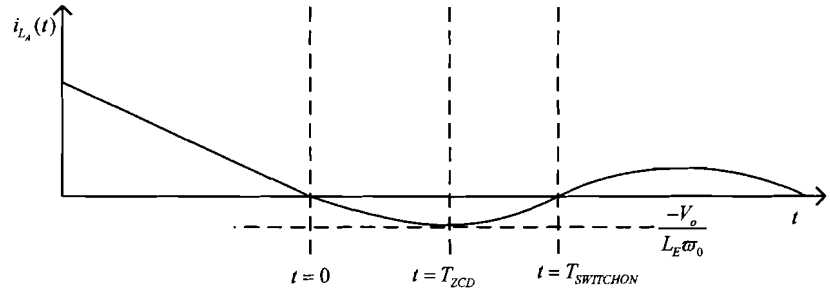


Figure 3.31, Inductor current during switch transition.

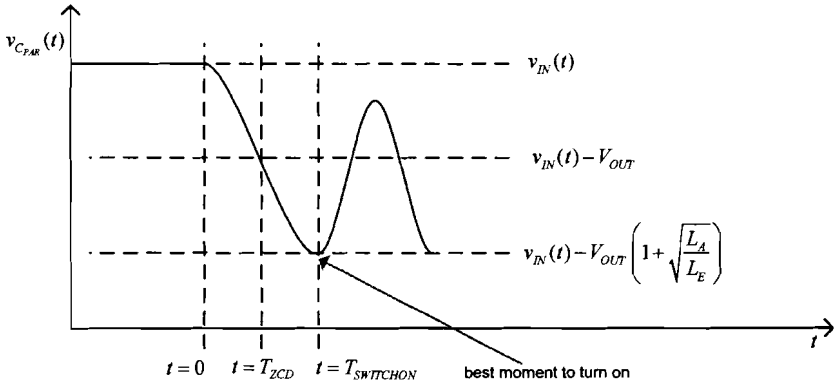


Figure 3.32, Capacitor voltage during switch transition.

3.3.2.4.2 Switching analysis of the boost switch

During the boost mode the boost switch is closed until a certain reference current is reached. At $t=T_{OFF}$ the switch will be turned off, Fig 3.33 shows the situation at $t=T_{OFF}$.

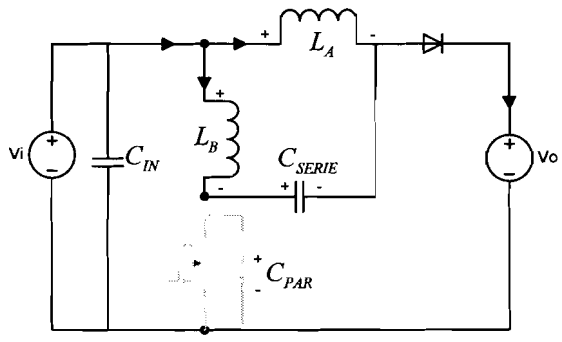


Figure 3.33, Situation after the switch is turned off.

Assuming C_{SERIE} is very large the sum of the currents through the inductors will decrease linearly until it becomes zero and the diode stops conducting. When the diode stops conducting (at $t = 0$) a resonating path is formed with the parasitic capacitor of the switch. This situation is shown in Fig 3.34.

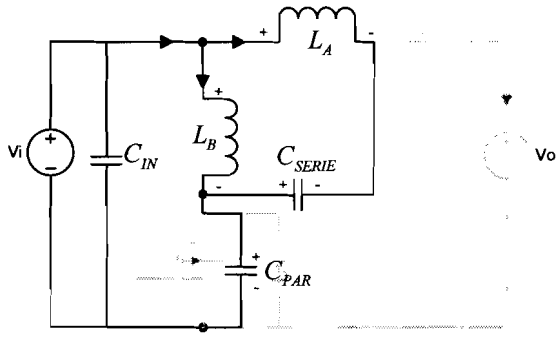


Figure 3.34, Resonating path.

The sum of the inductor currents can be described by the equation:

$$i_{L_E}(t) = \frac{v_{IN}(t) - V_{OUT}}{L_E \varpi_0} \sin(\varpi_0 t) \tag{1.97}$$

and the voltage across the parasitic capacitor:

$$v_{C_{PAR}}(t) = \frac{1}{C_{PAR}} \int i_{LE}(t)dt + v_{C_{PAR}}(0) \tag{1.98}$$

$$v_{C_{PAR}}(t) = v_{IN}(t) - \left(v_{IN}(t) - V_{OUT}\right)\cos(\varpi_0 t) \tag{1.99}$$

with

$$L_E = \frac{L_A L_B}{L_A + L_B} \tag{1.100}$$

and

$$\varpi_0 = \frac{1}{\sqrt{L_E C_{PAR}}}. \tag{1.101}$$

After some time (at $t = T_{SWITCHON}$) the voltage across the parasitic capacitor will be at its minimum. When it becomes negative the internal diode of the switch starts conducting. (Fig. 3.35). The time for switching on, can be calculated by:

$$T_{SWITCHON} = \arccos\left(\frac{v_{IN}(t)}{\left(v_{IN}(t) - V_{OUT}\right)}\right)\frac{1}{\varpi_0}. \qquad (1.102)$$

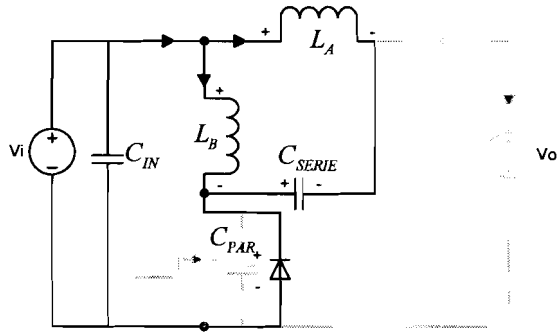


Figure 3.35, Conducting diode.

At $t = T_{SWITCHON}$ the capacitor voltage is at its minimum and the switch can be turned on with minimum switching loss. The complete sequence is shown in Fig. 3.36 and 3.37.

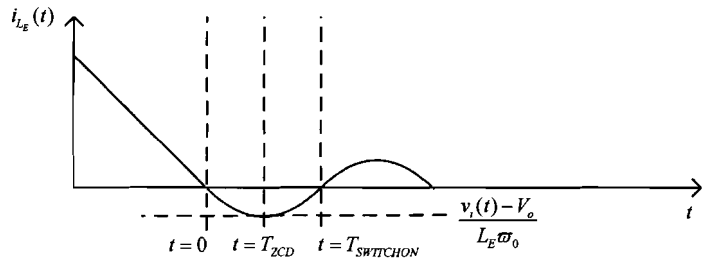


Figure 3.36, Inductor current during switch transition.

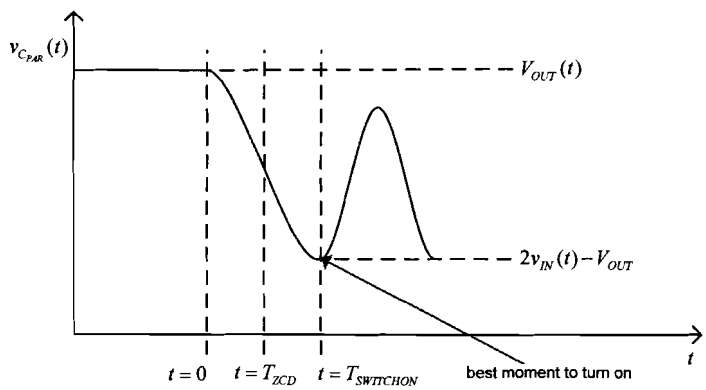


Figure 3.37, Capacitor voltage during switch transition.

3.4 PROPERTIES OF THE PFC'S

In the previous sections three kinds of PFC for universal input application were analyzed. In the next chapters the efficiency of the Low stress Buck Boost PFC will be compared with the SEPIC PFC. Besides the efficiency there are two other interesting items: the Total Harmonic Distortion (THD) of the input current and the switching frequency.

3.4.1 Total Harmonic Distortion (THD) of the input current

All topologies discussed in this chapter cause harmonic distortion of the input current when the amplitude of the input voltage is higher than the output current. When the amplitude of the input voltage is lower than the output voltage, both buck boost derivatives will operate in the boost mode and theoretically there will be no harmonic distortion. For the different topologies, the average input currents determined earlier are summarized in Table 3.2.

PFC topology	Input current
SEPIC	$i_{IN}(t) = \hat{I}_{PEAK} \frac{\lvert\sin(\varpi t)\rvert}{2\left(1+\frac{\hat{V}_{IN}\lvert\sin(\varpi t)\rvert}{V_{OUT}}\right)}$
Single inductor Buck Boost / Low stress Buck Boost	$i_{IN_{BOOST}}(t) = \frac{\hat{I}_{PEAK}\lvert\sin(\varpi t)\rvert}{2}$
	$i_{IN_{BUCKBOOST}}(t) = \frac{\hat{I}_{PEAK}\lvert\sin(\varpi t)\rvert}{2}\frac{V_{OUT}}{V_{OUT}+\hat{V}_{IN}\lvert\sin(\varpi t)\rvert}$
	$i_{IN_{BUCK}}(t) = \frac{\hat{I}_{PEAK}}{2}\frac{V_{OUT}}{\hat{V}_{IN}}$

Table 3.2, Average input currents for the different modes

For simplicity it is assumed that the average input current for the Single inductor Buck Boost PFC and Low stress Buck Boost PFC are the same. The input current only differs slightly in the buck boost mode. The average input currents for both converters are shown in Fig. 3.38 and 3.39 for high line ($\hat{V}_{IN} = 700$, $V_{OUT} = 450$) and low line ($\hat{V}_{IN} = 400$, $V_{OUT} = 450$) conditions respectively.

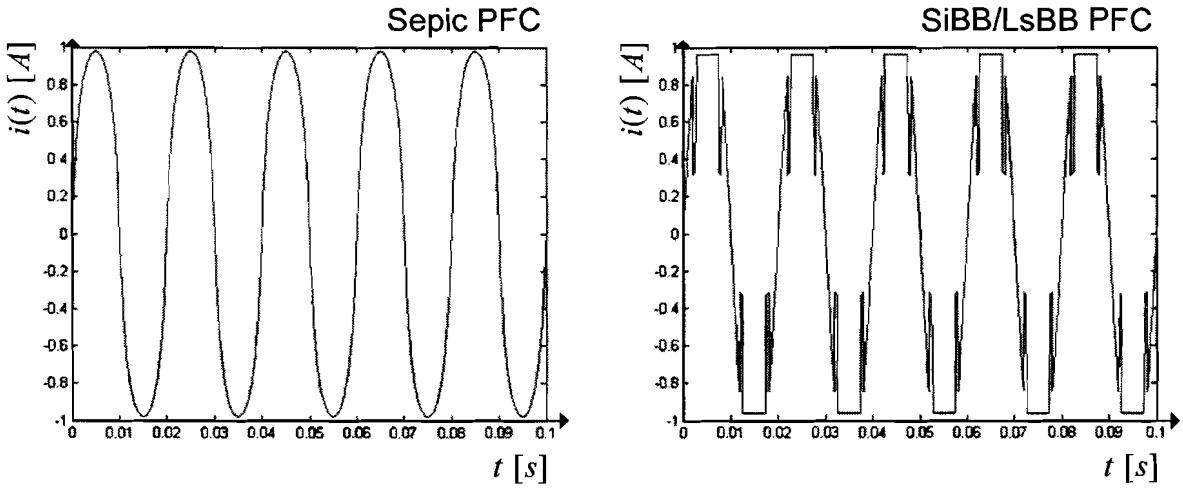


Figure 3.38, Average high line input currents the SEPIC PFC and Single inductor Buck Boost and Low stress Buck Boost PFC.

For high line conditions the input current for both PFC's is distorted with 14.7 % and 21.5 % for respectively the SEPIC PFC and the SiBB/LsBB PFC. Under low line conditions there is in theory no distortion in the SiBB/LsBB PFC, however the distortion in the SEPIC PFC equals: 11.1 %

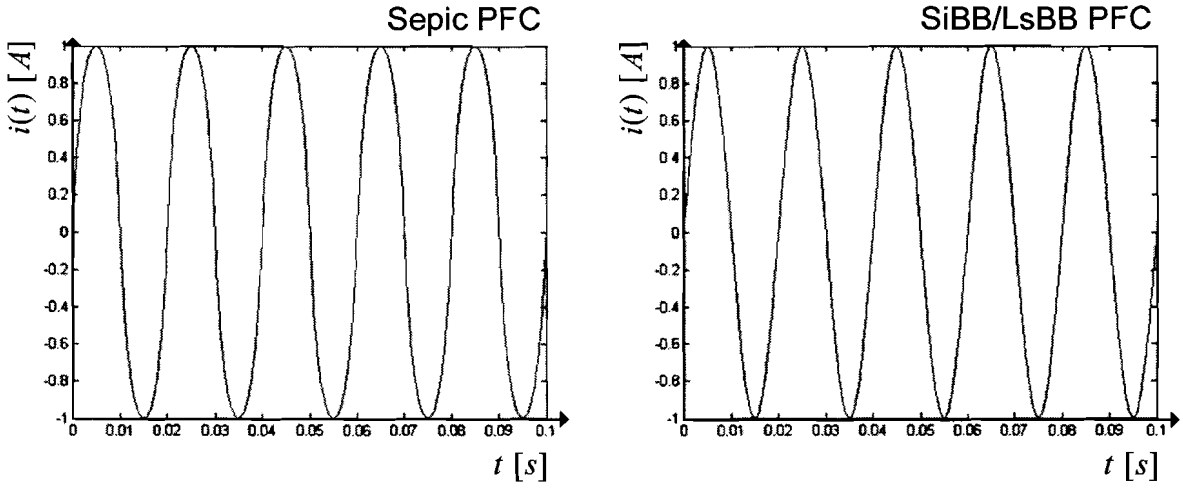


Figure 3.39, Average low line input currents of the SEPIC PFC and Single inductor Buck Boost and the Low stress Buck Boost PFC.

It can be concluded that all three topologies distort the line current. From the results above there it can be concluded that the SEPIC PFC's THD, is for high line conditions, better than the other topologies. Otherwise, for low line conditions there is theoretically no distortion in the LsBB/SiBB PFC but in the SEPIC PFC there still is. In terms of distortion, there can be concluded the SEPIC PFC performs better for high line conditions and the other better for low line conditions, this means that the overall distortion is the approximately equal.

3.4.2 Switching frequencies

Another important aspect of a PFC is the switching frequency. The switching frequency for the different topologies was determined earlier in this chapter. In this section the results are compared.

Assuming there are no losses in the PFC for the SEPIC PFC, the switching frequency is shown in Fig. 3.40 for the high ($\hat{V}_{IN} = 700$, $V_{OUT} = 450$) and low line ($\hat{V}_{IN} = 400$, $V_{OUT} = 450$) situation.

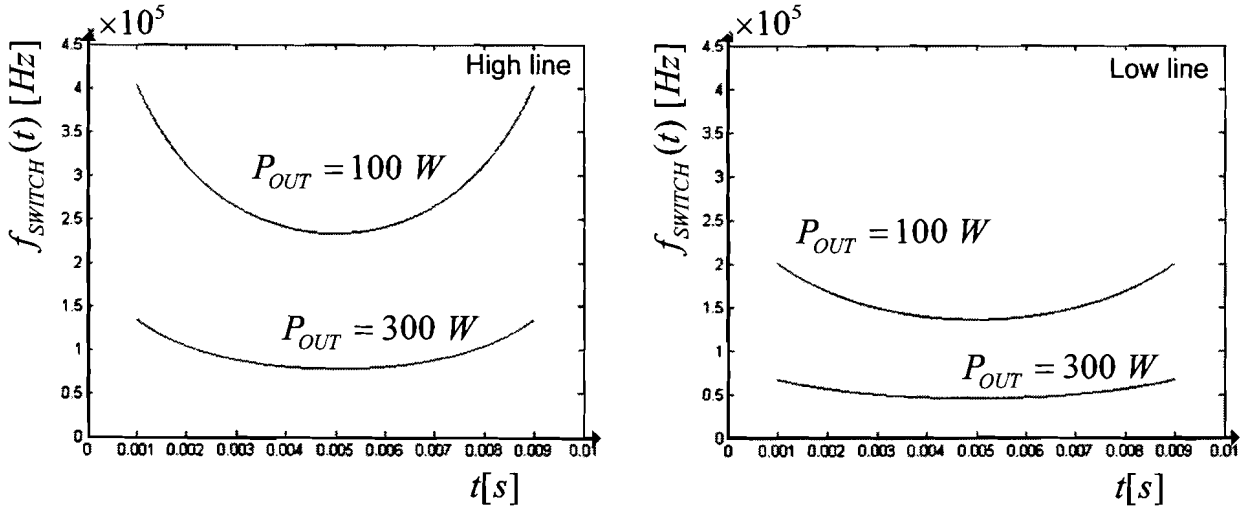


Figure 3.40, Switching frequency of the SEPIC PFC for high line situation (left) and low line situation (right) during a line cycle.

For the SiBB and the LsBB, under high line conditions, the PFC will change of mode during a line cycle. Assuming the same inductors are applied in SiBB and LsBB, the LsBB has two inductors in parallel during the boost mode. This implicates the switching frequency of the LsBB will be twice as high in the boost mode, in comparison with the SiBB. The switching frequencies for both PFC's under different conditions are shown in Fig. 3.41 and 3.42.

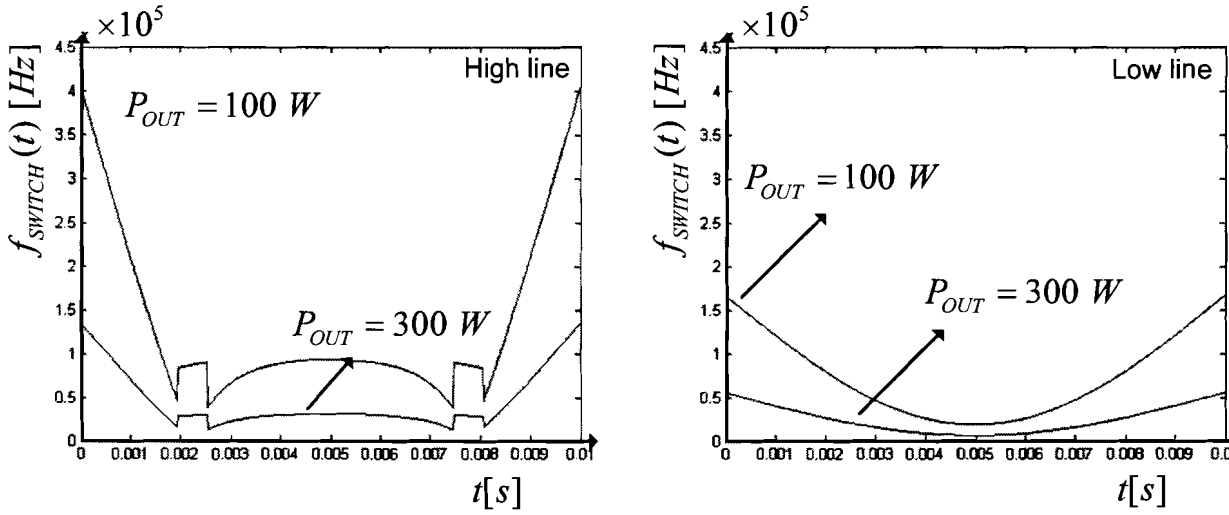


Figure 3.41, Switching frequency of the SiBB PFC for high line situation (left) and low line situation (right) during a line cycle.

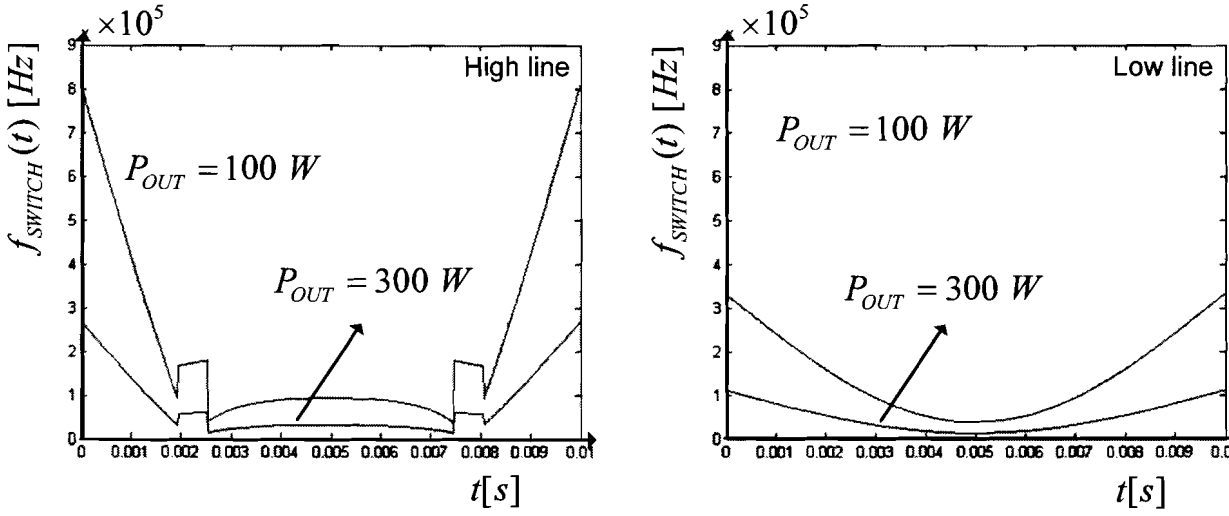


Figure 3.42, Switching frequency of the LsBB PFC for high line situation (left) and low line situation (right) during a line cycle.

It can be concluded that the switching frequency of SEPIC PFC is the most constant. Even when the SiBB and LsBB PFC 's are operating in boost mode only (low line input), the characteristic of the SEPIC PFC is still preferable. Under high line conditions the PFC changes of mode which results in a discontinuous characteristic as shown in the left hand characteristics of Fig. 3.41 and 3.42. The LsBB PFC uses two inductors in the boost mode which results into a very large f_{MAX} / f_{MIN} ratio, this means that the SiBB PFC is more preferable over the LsBB, with regards to this aspect

4 CHAPTER 4 MODELING AND LOSS ANALYSIS

Since a comparison must be made between two topologies, the SEPIC PFC and the Low stress Buck Boost PFC, both topologies must be modeled. First the topologies will be modeled by using state space modeling, after that the component losses will be modeled and implemented into the state space model. Finally the two topologies will be compared and the results are discussed in chapter 5.

4.1 STATE SPACE MODELING FOR CYCLICALLY SWITCHED CONVERTERS

In the first part of this section the mathematical background of state space modeling for cyclically switched converters will be treated [10]. The second part of this section shows how the systems can be formulated in matrix notation.

4.1.1 State space modeling for cyclically switched systems

In this section the state space equations of a cyclically switched converter will be treated. For each mode i a differential equation can be formulated:

$$\frac{d\underline{x}}{dt} = A_i \underline{x} + B_i \underline{u} \tag{1.103}$$

Where A_i and B_i are respectively the system and source matrices describing the system in mode i. The vector $\underline{x}$ is the state vector, usually containing the inductor currents and the capacitor voltages. And finally $\underline{u}$ is the input vector of the system. A solution of equation (1.103) is found in [5], and is equal to:

$$\underline{x}(t_i) = e^{A_i(t_i - t_{i-1})}\underline{x}(t_{i-1}) + \int_{t_{i-1}}^{t_i} e^{A_i(t_i-\tau)} B_i \underline{u} d\tau \tag{1.104}$$

Assuming the matrices are time invariant, the following definitions are introduced to simplify the notation:

$$\Phi_i = \Phi(t_i, t_{i-1}) = e^{A_i t_i} \tag{1.105}$$

$$\Gamma_i = \int_{t_{i-1}}^{t_i} e^{A_i(t_i-\tau)} B_i d\tau = A_i^{-1}(e^{A_i(t_i-\tau)} - I)B_i . \tag{1.106}$$

(For derivation of (1.106) see Appendix B.5)
The cyclic system can now be defined as:

$$\underline{x}(t_i) = \Phi_i \underline{x}(t_{i-1}) + \Gamma_i \tag{1.107}$$

$$\underline{x}(t_2) = \Phi_2(\Phi_1\underline{x}(t_0) + \Gamma_1) + \Gamma_2 = \Phi_2\Phi_1\underline{x}(t_0) + \Phi_2\Gamma_1 + \Gamma_2 \tag{1.108}$$

Since the begin and end conditions must be equal, $\underline{x}(t_0)$ can be written as:

$$\underline{x}(t_0) = (I - \Phi_2\Phi_1)^{-1}(\Phi_2\Gamma_1 + \Gamma_2) \tag{1.109}$$

Although this expression looks simple, it is difficult to calculate, because the matrices might be singular (for the SEPIC converter they are) and so not invert-able. A more attainable approach has been developed in [6], [7]. In this approach the source matrix B_i is included in the system matrix; the A_i and the B_i matrix are eliminated. Note that this method, called vector augmentation, is only valid when the source matrix is time independent or when it hardly changes during a cycle, thus when $B_i \approx B_{i+1}$. When vector augmentation is applied, the system can be described by:

$$\frac{d}{dt}\begin{pmatrix} \vdots \\ x(t) \\ \vdots \\ \vdots \\ 1 \end{pmatrix} = \begin{pmatrix} \ulcorner & & & & \urcorner \\ & A_i & & & B_i \\ & & & & \\ \llcorner & & & & \lrcorner \\ 0 & 0 & 0 & 0 & 0 \end{pmatrix}\begin{pmatrix} \vdots \\ x(t) \\ \vdots \\ \vdots \\ 1 \end{pmatrix} \tag{1.110}$$

The general solution is now:

$$\underline{x}(t_i) = e^{A_i(t_i - t_{i-1})}\underline{x}(t_{i-1}). \tag{1.111}$$

Simplifying by using (1.105) gives:

$$\underline{x}(t_i) = \Phi_i\underline{x}(t_{i-1}). \tag{1.112}$$

Applying (1.112) on a system with respectively two and three modes gives:

$$\underline{x}(t_0) = \Phi_2\Phi_1\underline{x}(t_0) \tag{1.113}$$

$$\underline{x}(t_0) = \Phi_3\Phi_2\Phi_1\underline{x}(t_0) \tag{1.114}$$

The initial state vector can now be found by determining the null space for both equations, thus for finding the initial state vectors for which the equations;

$$(\Phi_2\Phi_1 - I)\underline{x}(t_0) = 0 \tag{1.115}$$

and

$$(\Phi_3\Phi_2\Phi_1 - I)\underline{x}(t_0) = 0 \tag{1.116}$$

are satisfied. The intermediate state vectors can easily be found by applying (1.112).

4.1.2 Describing systems in matrix notation

To apply the techniques treated in the previous section a matrix notation of the system is needed. In this section one matrix will be determined, the other matrices used in this work are determined in a similar way and can be found in APPENDIX D. The matrices for the SEPIC PFC in discontinuous conduction mode can be found in [14].

In Fig. 4.1 a mode of the SEPIC converter is shown.

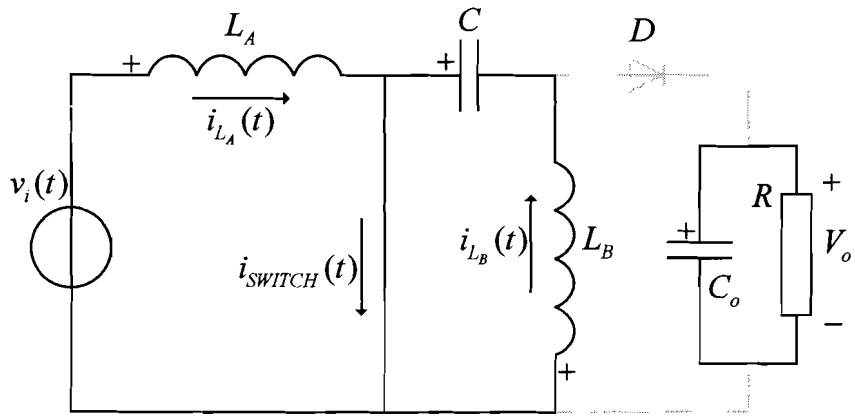


Figure 4.1, First mode of the SEPIC converter.

Since the system contains two inductors and two capacitors it is a fourth order system and it can be described by four differential equations:

$$\frac{di_{L_A}}{dt} = \frac{V_i}{L_A} \qquad (1.117)$$

$$\frac{di_{L_A}}{dt} = \frac{v_C}{L_B} \qquad (1.118)$$

$$\frac{dv_C}{dt} = \frac{-i_{L_B}}{C} \qquad (1.119)$$

$$\frac{dv_{C_o}}{dt} = \frac{-v_{C_o}}{RC_o} \qquad (1.120)$$

Define: $x_1 = i_{LA}$, $x_2 = i_{LB}$, $x_3 = v_C$, and $x_4 = v_{C_o}$ with the derivatives are respectively: $\dot{x}_1$, $\dot{x}_2$, $\dot{x}_3$ and $\dot{x}_4$. For the first stage the equations (1.117) - (1.120) become:

$$\dot{x}_1 = \frac{V_i}{L_A} \qquad (1.121)$$

$$\dot{x}_2 = \frac{x_3}{L_B} \qquad (1.122)$$

$$\dot{x}_3 = \frac{-x_2}{C} \qquad (1.123)$$

$$\dot{x}_4 = \frac{-x_4}{RC_o} \qquad (1.124)$$

Now all equations are known, the converter can be written in the form:

$$\underline{\dot{x}} = A\underline{x} + B\underline{u} \qquad (1.125)$$

For the first mode the A_1 and B_1 matrices are equal to:

$$\begin{pmatrix}\dot{x}_1\\ \dot{x}_2\\ \dot{x}_3\\ \dot{x}_4\end{pmatrix}=\overbrace{\begin{pmatrix}0 & 0 & 0 & 0\\ 0 & 0 & 1/L_B & 0\\ 0 & -1/C & 0 & 0\\ 0 & 0 & 0 & -1/(C_oR)\end{pmatrix}}^{A_1}\begin{pmatrix}x_1\\ x_2\\ x_3\\ x_4\end{pmatrix}+\overbrace{\begin{pmatrix}1/L_A\\ 0\\ 0\\ 0\end{pmatrix}}^{B_1}V_i. \tag{1.126}$$

With the state vector:

$$\underline{x}=\begin{pmatrix}x_1\\ x_2\\ x_3\\ x_4\end{pmatrix}=\begin{pmatrix}i_{LA}(t)\\ i_{LB}(t)\\ v_C(t)\\ v_{C_o}(t)\end{pmatrix}. \tag{1.127}$$

By using the augmentation technique as treated in the previous section, the matrices can be combined:

$$\begin{pmatrix}\dot{x}_1\\ \dot{x}_2\\ \dot{x}_3\\ \dot{x}_4\\ 1\end{pmatrix}=\overbrace{\begin{pmatrix}0 & 0 & 0 & 0 & V_i/L_A\\ 0 & 0 & 1/L_B & 0 & 0\\ 0 & -1/C & 0 & 0 & 0\\ 0 & 0 & 0 & -1/(C_oR) & 0\\ 0 & 0 & 0 & 0 & 0\end{pmatrix}}^{A_1'}\begin{pmatrix}x_1\\ x_2\\ x_3\\ x_4\\ 1\end{pmatrix} \tag{1.128}$$

with the state vector:

$$\underline{x}=\begin{pmatrix}x_1\\ x_2\\ x_3\\ x_4\\ x_5\end{pmatrix}=\begin{pmatrix}i_{LA}(t)\\ i_{LB}(t)\\ v_C(t)\\ v_{C_o}(t)\\ 1\end{pmatrix}. \tag{1.129}$$

4.1.3 State space modeling for Power Factor Corrector circuits

In the previous sections the input voltage of the system was a constant (V_i). In PFC applications the input voltage is time dependent, but since the frequency of the input voltage is much lower than the system frequency, the augmentation technique is still valid. In most PFC applications operating in Boundary Conduction Mode (BCM) switches are kept on until a certain reference input current is reached. After this reference has been reached the switch is turned off. The input current will decrease until it has become zero. This process is shown in Fig 4.2.

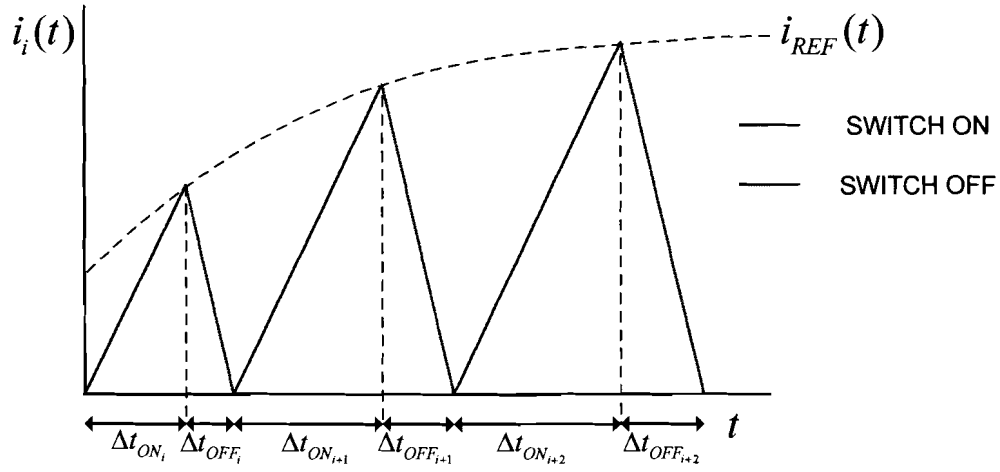


Figure 4.2, Typical input current of a PFC.

In the case of the SEPIC converter the switch must be turned off when the sum of the inductor currents has reached the reference current, thus when $i_{LA}(t)+i_{LB}(t)=i_{REF}(t)$. t_{OFF} can be calculated by solving the following set of equations:

$$\begin{pmatrix} i_{LA}(t_i)=i_{REF}-i_{LB}(t_i) \\ i_{LB}(t_i)=i_{REF}-i_{LA}(t_i) \\ v_C(t_i) \\ v_{C_o}(t_i) \\ 1 \end{pmatrix} = \Phi_1 \begin{pmatrix} i_{LA}(t_{i-1}) \\ i_{LB}(t_{i-1}) \\ v_C(t_{i-1}) \\ v_{C_o}(t_{i-1}) \\ 1 \end{pmatrix} = e^{A_1 t_{OFF}} \begin{pmatrix} i_{LA}(t_{i-1}) \\ i_{LB}(t_{i-1}) \\ v_C(t_{i-1}) \\ v_{C_o}(t_{i-1}) \\ 1 \end{pmatrix} \quad (1.130)$$

After some time, the current has become zero and the switch must be turned on again at $t=t_{ON}$. The time t_{ON} can be calculated in a similar way as t_{OFF}. By using a functional programming language (such as MATLAB) these calculations can be done for numerous times.

The flowchart should look like as shown in Fig 4.3.

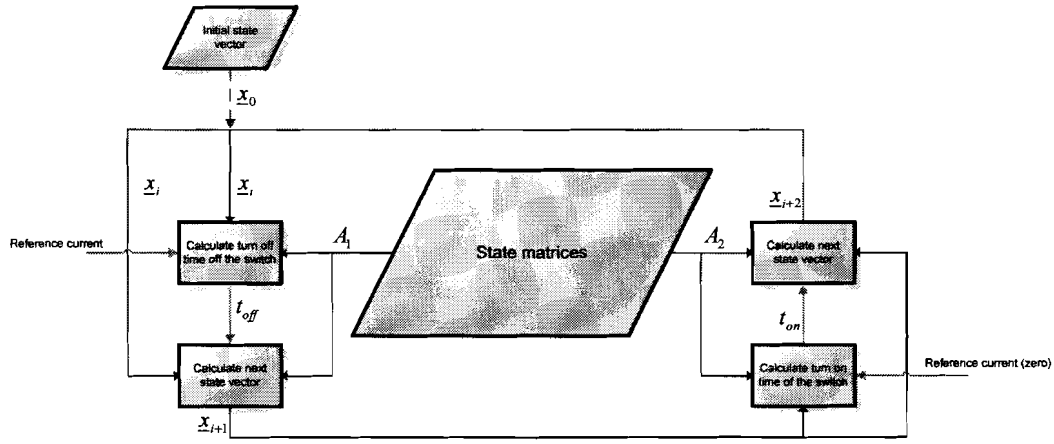


Figure 4.3, Flowchart of a PFC model.

Up till now the state vectors are known only at the moment the system is switched. The voltages and currents between the switching cycles are not known. By adding intermediate time steps the accuracy can be enlarged which will result in a better FFT and losses analysis (which will be treated later). This can simply be done by dividing the time that the switch is on or off by the desired number of intervals (to get additional output vectors). An example is shown in Fig 4.4. At $t = 0$, $t = t_{OFF}$ and $t = t_{ON}$, the system changes mode. The dots within are the additional state vectors.

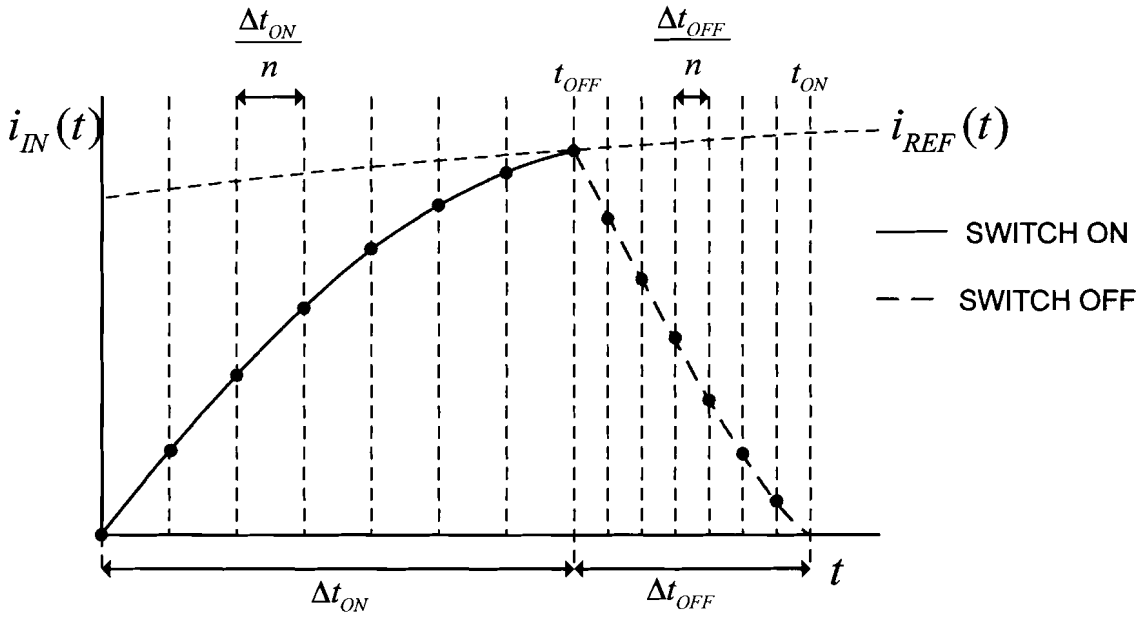


Figure 4.4, Waveform with additional vectors.

4.2 LOSS ANALYSIS

In this section the losses of the different components of a PFC will be analyzed. This can be divided in three main parts:

- Conduction losses
- Switching losses
- Magnetic losses

4.2.1 Conduction losses

Conduction losses can be linear, in the case of a pure resistance, but can also be non-linear, for example in semiconductors. In this analysis the conduction losses in the following components will be considered:

- Capacitors
- Diodes
- Switches (MOSFET/IGBT)

4.2.1.1 Loss in capacitors

The loss in capacitors is mainly characterized by the internal resistance of the capacitor, which can be specified as a loss angle δ or as ESR (Effective Series Resistance). The ESR is simply the internal resistance of the capacitor. The loss angle is the angle between the imaginary and the real part of the capacitor's impedance for a certain frequency. This can be calculated by:

$$\delta = \arctan\left(\frac{R_{ESR}}{X_C}\right) \tag{1.131}$$

which can be written as:

$$R_{ESR} = X_C \tan\delta \tag{1.132}$$

where

$$X_C = \frac{1}{2\pi fC}. \tag{1.133}$$

An graphical representation is given in Fig 4.5:

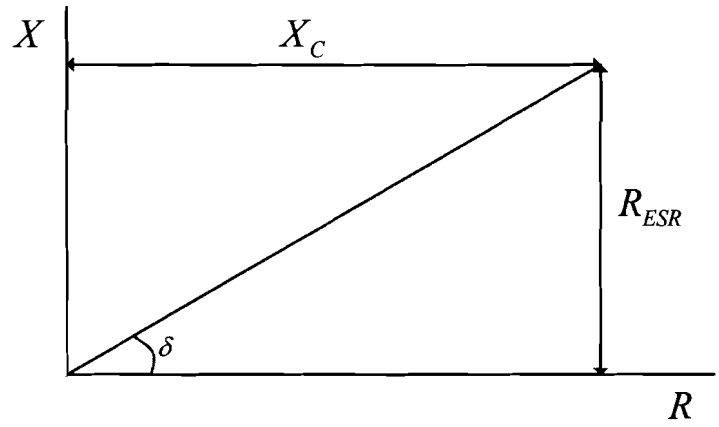


Figure 4.5, Graphical representation of the loss angle.

For small capacitors manufacturers usually specify the losses by the loss angle, for large capacitors (ELCAP's) usually the ESR is given. Now the properties of the capacitors are known, the loss in a capacitor can be calculated:

$$p_{LOSS_{ELCAP}} = R_{ESR} i^2_{CAPACITOR} \tag{1.134}$$

for the ELCAP's and

$$p_{LOSS_{SMALCAP}} = X_C i^2_{CAPACITOR} \tan\delta \tag{1.135}$$

for small capacitors.

4.2.1.2 Conduction loss in diodes

As mentioned earlier, the behavior of a diode is non-linear; the forward voltage across the diode depends on the current in a non-linear way. An typical voltage-current characteristic is shown in Fig 4.6.

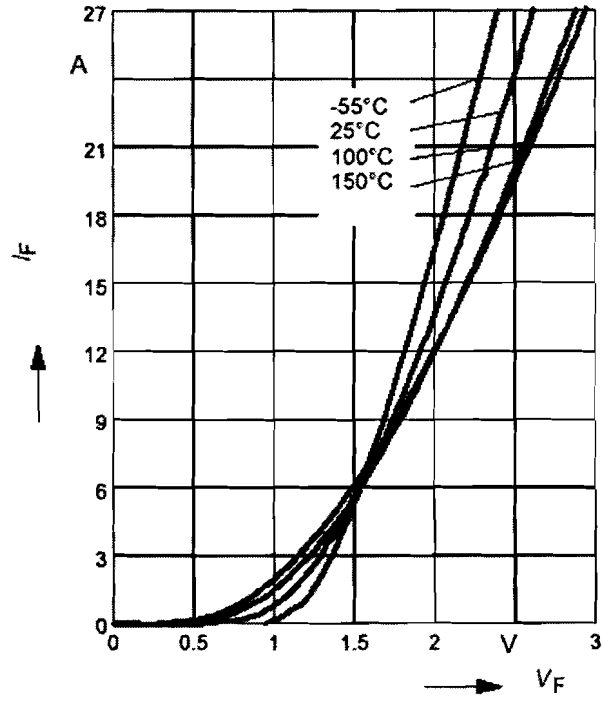


Figure 4.6, typical voltage-current characteristic for an IDB09E120 (Infineon) power diode.

To do an accurate loss calculation for different currents, the voltage-current characteristic can be approximated by a table function which is shown in Fig 4.7.

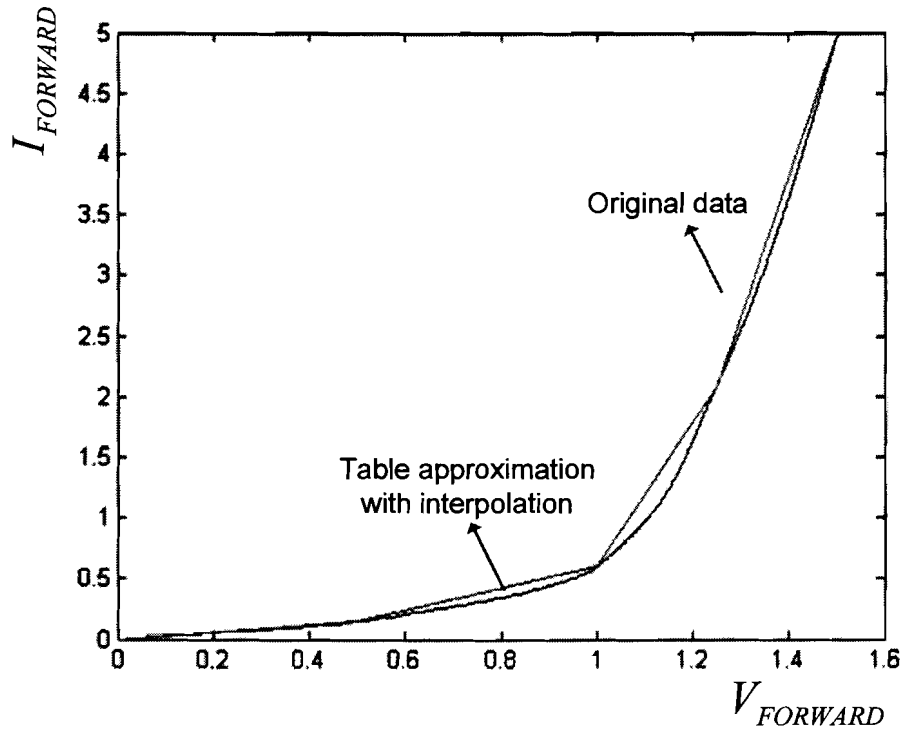


Figure 4.7, Typical voltage-current characteristic for an IDB09E120 (Infineon) power diode.

With this curve fitting method it is possible express the forward voltage as function of the current through the diode. This offers the possibility to calculate the conduction loss of the diode. The expression becomes:

$$p_{LOSS_{DIODE}} = i_{FORWARD} \cdot v_{FORWARD} = i_{FORWARD} \cdot f(i_{FORWARD}) . \quad (1.136)$$

4.2.1.3 Conduction loss in switches

In switched applications usually MOSFET's or IGBT's are applied as switch. Because the structure of both switches differs, also the loss properties are different. The conduction loss in MOSFET's is characterized by the $R_{DS_{ON}}$, an internal resistance between the drain and the source which is constant (for a constant temperature) and hardly depends on the drain-source current. The on resistance as function of the drain-source current is shown in Fig 4.8.

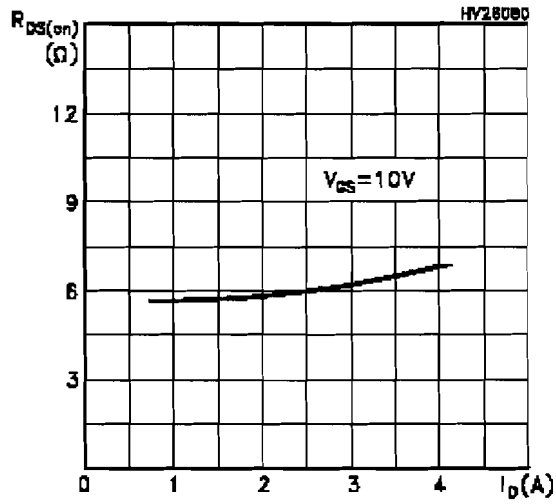


Figure 4.8, $R_{DS_{ON}}$ as function of the drain current for a STP4N150 (ST) power MOSFET.

Assuming $R_{DS_{ON}}$ is constant, which it approximately is in practice (for a constant temperature), the conduction loss in a MOSFET can be calculated by:

$$p_{LOSS_{MOSFET}} = R_{DS_{ON}} i^2_{DRAIN} . \quad (1.137)$$

When applying a IGBT as switch, the voltage across the switch (collector emitter voltage) depends on the current through it in a non-linear way. A typical V_{CE} - I_{CE} characteristic is shown in Fig 4.9.

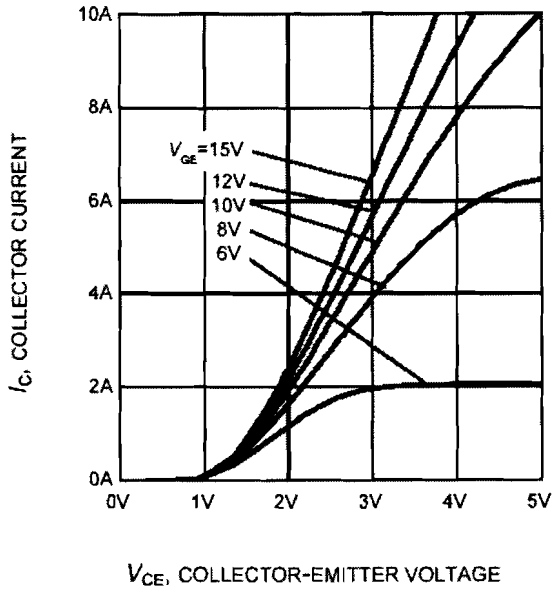


Figure 4.9, V_{CE} as function of the collector current for a IGB03N120 (Infineon) IGBT.

The conduction loss in the switch can be calculated by:

$$p_{LOSS_{IGBT}} = i_C \cdot v_{CE} . \tag{1.138}$$

And since the collector emitter voltage is a function of the collector current (1.138) can be written as:

$$p_{LOSS_{IGBT}} = i_C \cdot f(i_C) . \tag{1.139}$$

To obtain a good indication for the conduction losses of the IGBT, V_{CE} must be approximated. This can be done by using the table function in MATLAB (or in another functional programming language) and is shown in Fig 4.10.

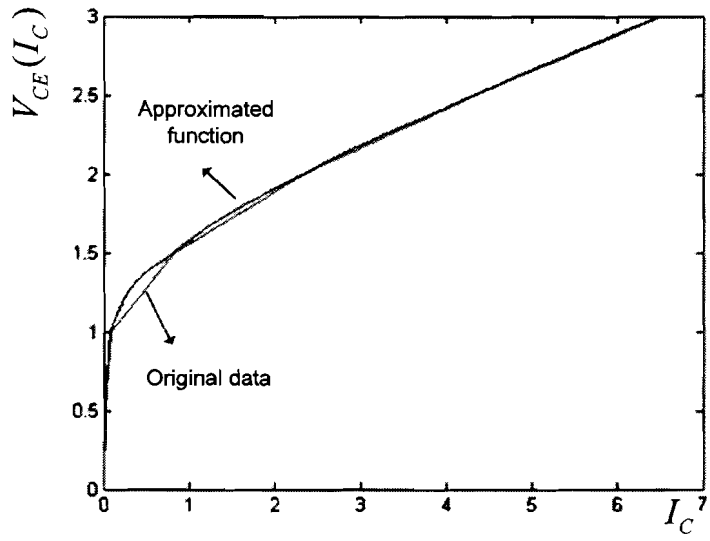


Figure 4.10, typical voltage-current characteristic for an IBG03N120 (Infineon) IGBT.

4.2.2 Switching losses

Switching losses (in the IGBT's or MOSFET's) are caused by the transition time between the on and off time state of the switch. When a switch is opened, there is a certain voltage across the switch but there is no current flowing. When the switch is closed, the voltage across the switch is zero and a certain current is flowing. In an ideal switch the transition time between the on and off state is zero. However in practice the transition time is non-zero and this will cause switching losses. This is shown in Fig 4.11. Although IGBT 's and MOSFET's perform the same function, their switching behavior differs. This will be modeled in the following sections. It must be noted, that it is possible to reduce the switching losses by applying an additional capacitor (reduces switch off loss) or by adding some switch on delay (reduces switch on loss). These opportunities for reducing switching loss are not modeled.

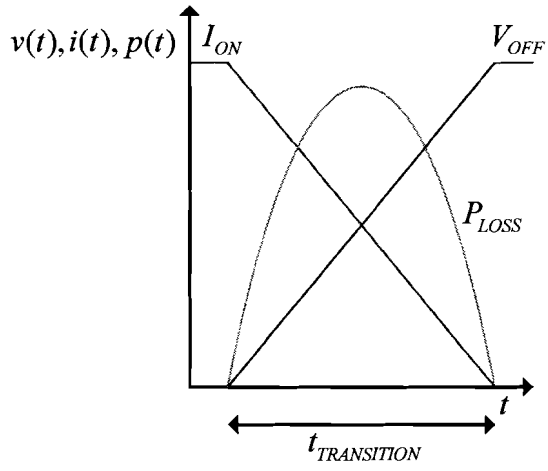


Figure 4.11, Typical switch characteristic.

4.2.2.1 Modeling MOSFET switching losses

As treated in the previous section, a switch takes some time to change state. In the case of a MOSFET this is the fall or/and rise time. When the MOSFET is turned off, the current through it will decrease. Assuming the current decreases linearly, it can be described by:

$$i_{SWITCH}(t) = I_{ON} - \frac{I_{ON}}{t_{FALL}} t \qquad \text{for} \qquad 0 \le t \le t_{FALL}. \tag{1.140}$$

At the moment the current through the switch starts decreasing, the voltage across the switch starts increasing:

$$v_{SWITCH}(t) = \frac{V_{OFF}}{t_{FALL}} t \qquad \text{for} \qquad 0 \le t \le t_{FALL}. \tag{1.141}$$

The power loss as function of the time can now be written as:

$$p_{SWITCH}(t) = \frac{I_{ON} V_{OFF}}{t_{FALL}} t - \frac{V_{OFF} I_{ON}}{t_{FALL}^2} t^2 \qquad \text{for} \qquad 0 \le t \le t_{FALL}. \tag{1.142}$$

Integrating (1.142) gives the total loss by switching off:

$$E_{OFF_{LOSS}} = \int_0^{t_{FALL}} \left(\frac{I_{ON} V_{OFF}}{t_{FALL}} t - \frac{V_{OFF} I_{ON}}{t_{FALL}^2} t^2 \right) dt = \frac{V_{OFF} I_{ON} t_{FALL}}{6}. \tag{1.143}$$

Since t_{FALL} hardly depends on the drain-source voltage or the drain current, equation (1.143) is suitable to calculate the turn-off loss in a MOSFET.

Although the current through the MOSFET starts increasing form zero when switched on, there is also switch on loss. The MOSFET contains a parasitic drain-source capacitor with a certain amount of energy. When switching on, the parasitic capacitor is short circuited and the energy will be dissipated in the MOSFET. The switch on loss is described by:

$$E_{ON_{LOSS}} = \frac{1}{2} C_{PAR} V_{OFF}^2 \tag{1.144}$$

where V_{OFF} is the voltage across the MOSFET before switching on.

4.2.2.2 Modeling IGBT switching losses

Modeling the IGBT's switching loss is more difficult, since the transition time is not constant but depends on the switch current and voltage. Although detailed modeling is

possible [10] - [13], it is easier to use the parameters provided by the IGBT's manufacturers. Most manufacturers provide the switching loss as a function of the current (for a certain voltage). This data can be approximated by a first order function and the loss can be written as a function of the switch current:

$$E_{ON_{LOSS}} = f(I_{ON}) \tag{1.145}$$

$$E_{OFF_{LOSS}} = f(I_{ON}). \tag{1.146}$$

4.2.3 Magnetic losses

Magnetic loss occur in the inductors. For determining these losses a special program is used, MAGTOOL. This program determines the inductor losses for different (current) waveforms. Waveforms from the simulations are imported in MAGTOOL and the losses are determined.

4.3 IMPLEMENTING COMPONENT LOSSES INTO THE STATE SPACE MODEL

In section 4.1 the PFC has been modeled using state space modeling. With this method every current and voltage in the PFC can be determined at any moment. In section 4.2 the loss occurring in the different components has been modeled as function of voltages and/or currents. When combining the results of both sections, which will be done in this section, it is possible to calculate the PFC losses.

4.3.1 Determining PFC losses

The input voltage of the PFC is either $50\ Hz$ or $60\ Hz$ (and the input current is proportional with the input voltage). Therefore the waveforms of the PFC are repetitive with a period time; $T = 1/50\ Hz$ or $T = 1/60\ Hz$. This is called a grid cycle. Thus, with a proper model, it is sufficient to determine the power losses in the PFC for one grid cycle. There are two methods to do this:

- Summing the power loss over n intervals and then calculate the average power loss.
- Dividing the total energy loss in one grid cycle by T_{CYCLE}

The first method can not be applied since the intervals between the state vectors are not time invariant, as can be seen in Fig 4.12.

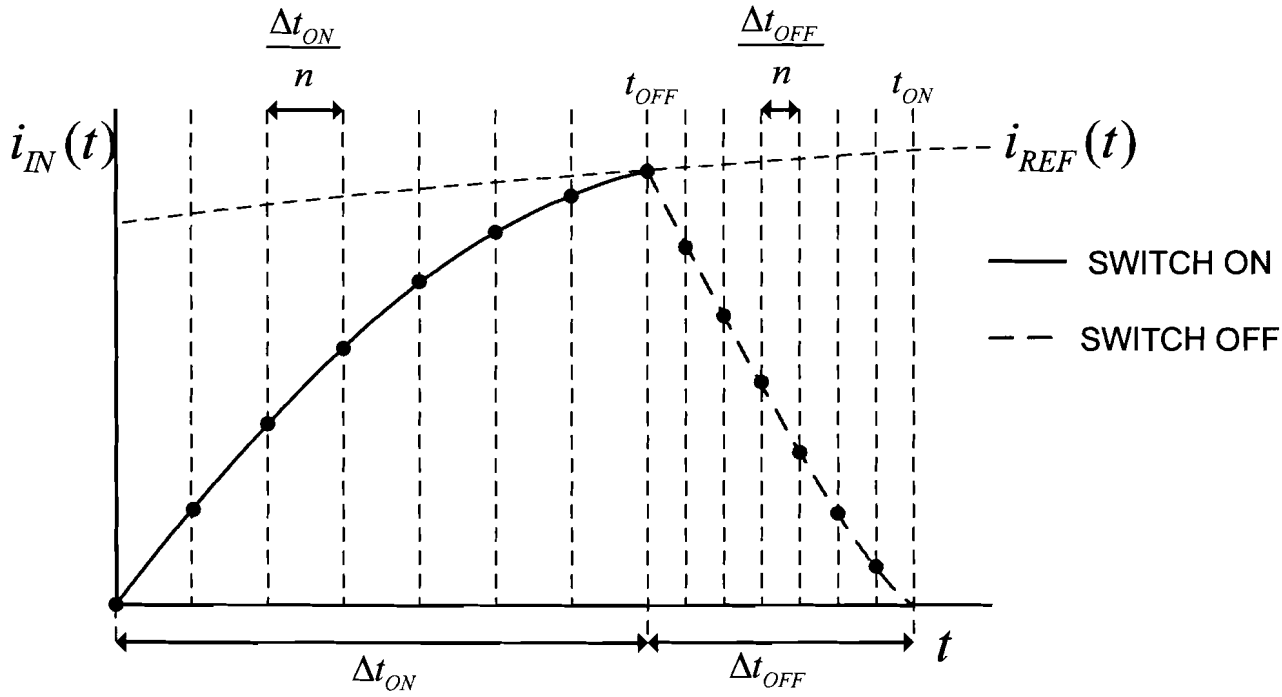


Figure 4.12, Current determined at different times as function of the time.

A better method is to calculate the energy loss at every interval:

$$E_{i_{LOSS}} = p_{i_{LOSS}} T_i \tag{1.147}$$

and sum al these 'loss packets' during a grid cycle

$$E_{LOSS} = \sum_{i=1}^{n} E_i \,. \tag{1.148}$$

When equation (1.148) is divided by the period time of the grid cycle, the PFC's power loss during a grid cycle can be calculated:

$$P_{LOSS} = \frac{1}{T_{CYCLE}} \sum_{i=0}^{n} E_i \,. \tag{1.149}$$

An additional advantage of this method is that it is easy to add switching losses since they do not occur in every interval. For clarity an example will be given; Fig. 4.13 shows successively the current through the MOSFET and the diode. This could be the waveform of a simple boost converter.

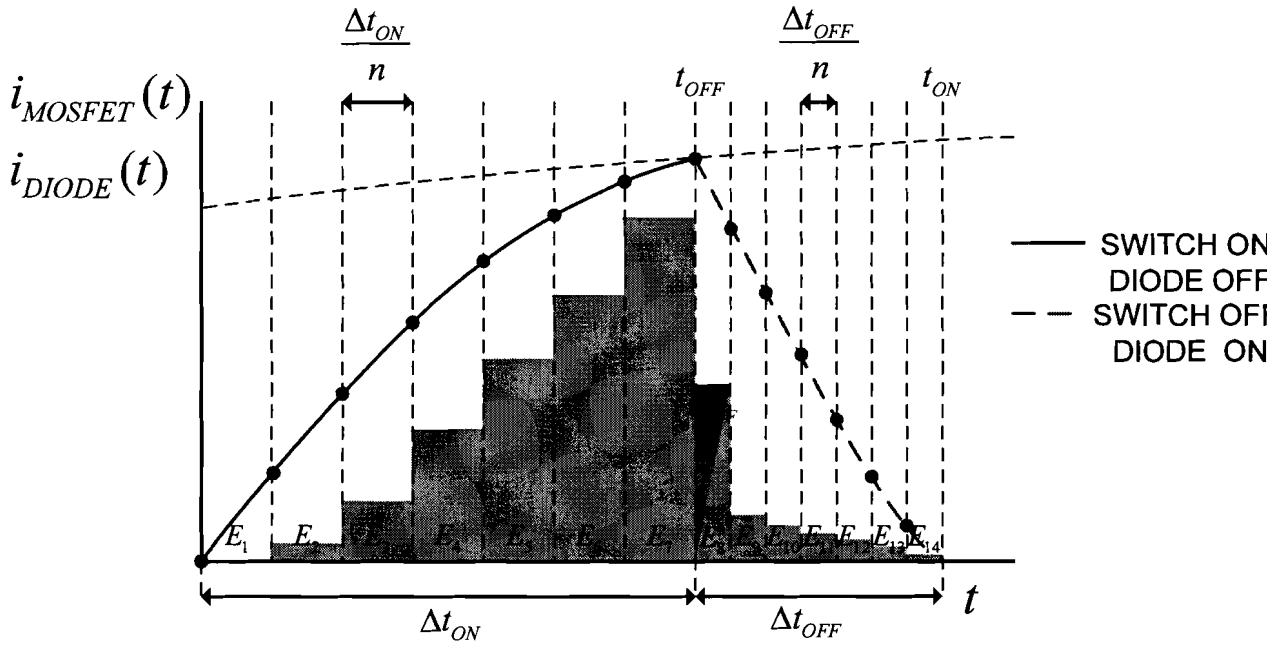


Figure 4.13, MOSFET and diode current.

The non-dotted line represents the current through the MOSFET and the dotted line represents the current through the diode. The square of the green bars represent the conduction loss (energy) in the MOSFET (for $t < t_{OFF}$) and the diode (for $t \geq t_{OFF}$). The square of the dark bar at $t = t_{OFF}$, represents the switch off loss of the MOSFET. The total energy loss is now:

$$E_{LOSS_{TOTAL}} = E_{OFF} + \sum_{i=1}^{n} E_i = E_{OFF} + E_1 + E_2 + ... + E_{14} \tag{1.150}$$

Assuming $T_{CYCLE} = \Delta t_{ON} + \Delta t_{OFF}$, the power loss can be calculated by:

$$P_{LOSS_{TOTAL}} = \frac{E_{OFF} + \sum_{i=1}^{n} E_i}{\Delta t_{ON} + \Delta t_{OFF}} = \frac{E_{OFF} + E_1 + E_2 + ... + E_{14}}{\Delta t_{ON} + \Delta t_{OFF}}. \tag{1.151}$$

The efficiency in percent of the PFC can now be calculated by:

$$\eta = \frac{P_{OUT}}{P_{IN}} \cdot 100 = \frac{P_{OUT}}{P_{OUT} + P_{LOSS_{TOTAL}}} \tag{1.152}$$

4.4 SUMMARY

In this chapter it is discussed how a PFC for losses analysis can be modeled. Both the SEPIC PFC as the LsBB PFC are modeled and simulated. The results are treated in chapter 5.

5 CHAPTER 5 EFFICIENCY COMPARISON

In the previous chapter it was explained how a PFC can be modeled and how the power losses can be calculated. In this chapter the efficiency of the SEPIC and Low stress Buck Boost topologies will be determined and evaluated. This will be done for a power range from $100\ W$ up to $300\ W$ and for both high line ($\hat{V}_{IN} = 700\ V$) as for low line ($\hat{V}_{IN} = 450\ V$) situations.

5.1 POWER LOSS IN THE SEPIC PFC

In this section the used components will be treated briefly and after that simulation results of the SEPIC PFC will be discussed.

5.1.1 Components of the SEPIC PFC

The SEPIC PFC contains seven components; a bridge rectifier, a switch, a diode, two inductors and two capacitors. Since both converters operate in the same power and voltage range, the loss occurring in the buffer capacitor will not be determined. The components used in the SEPIC PFC are:

Switch	Diode	Series capacitor	Inductor A	Inductor B
STP4N150 or IGB03N120H2	IDB09E120	MKP1840 200nF	2 mH	4 mH

Table 5.1, Used components in the SEPIC PFC

For the switch a STP4N150 MOSFET from ST or an IGB03N120H2 IGBT from Infineon is used. The MOSFET can handle voltages up to $1500\ V$ and a continuous currents up to $4\ A$. The drain source resistance is smaller than $7\ \Omega$. The IGBT can handle voltages up to $1200\ V$ and a continuous currents up to $3\ A$. The used components are the best components commercially available.

The collector emitter voltage of the IGBT can be modelled by a table as shown in chapter 4. The switching losses can be approximated by a first order function. The results are shown in the Fig 5.1 and 5.2.

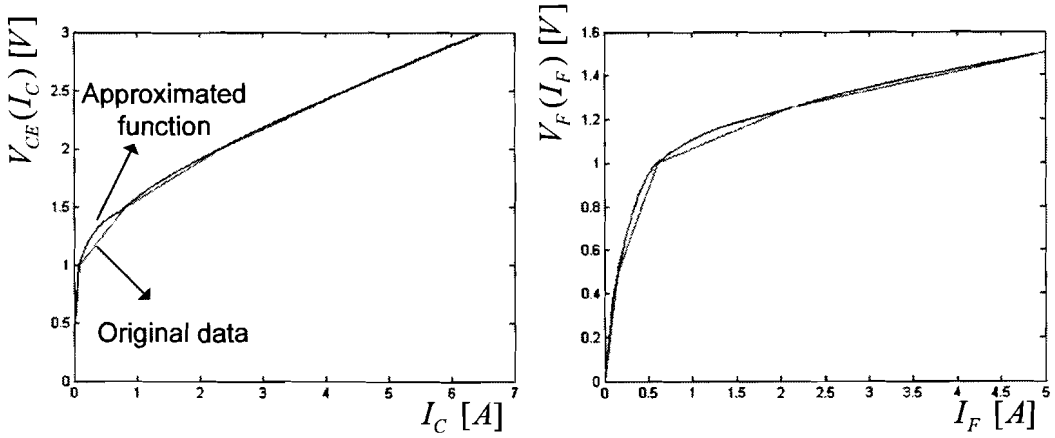


Figure 5.1, Approximated functions and original data for successively; collector emitter voltage of the IGBT, forward voltage of the diode.

The diode is also from Infineon and applicable in circuits with voltages below $1200\ V$ and continuous current smaller than $9\ A$. The approximated current-voltage characteristic is shown on the right hand side of Fig 5.1.

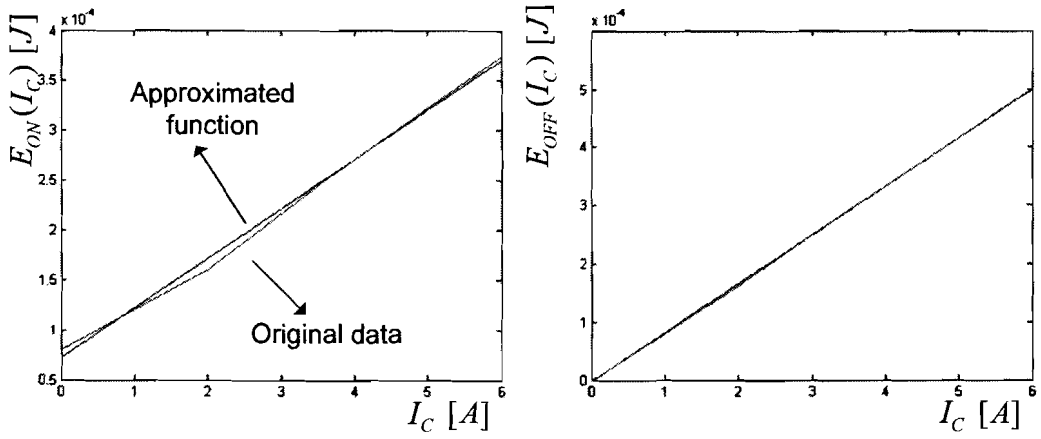


Figure 5.2, switching losses of the IGBT as function of the current.

The series capacitor is $1600\ V$ type from Vishay. The tangent of the loss angle δ at $100\ kHz$ is; $\tan(\delta) \leq 20 \cdot 10^{-4}$ thus the R_{ESR} (by using (1.132)) equals $R_{ESR} = 0.016\ \Omega$.

For both inductors an E36/21/15 core is used with 3C92 as material, however inductor A is wound with 110 turns of $16 \times 0.2\ mm$ litze and inductor B is wounded with 150 turns of $12 \times 0.2\ mm$ litze. The airgaps are $2\ mm$ and $1.75\ mm$ respectively. The inductor values ($2\ mH$ and $4\ mH$) are chosen in that way, the ripple at the series capacitor is at its lowest.

The inductor losses have been calculated for two situations:

1. High line and low power, $\hat{V}_{IN} = 700\ V$, $P_{OUT} = 100\ W$
2. Low line and high power, $\hat{V}_{IN} = 452\ V$, $P_{OUT} = 300\ W$

In the first case the switching frequency is high and the current through the inductors will be low, in this case the power loss will be dominated by 'non conductivity losses' such as core losses. In the second situation, the switching frequency is lower and the inductor currents larger, in this case the inductor losses will be dominated by conductivity losses. The results from the MATLAB/MAGTOOL simulations are shown in the table below.

	High line and low power	Low line and high power
Loss in inductor A	0.964 (W)	2.049 (W)
Loss in inductor B	0.506 (W)	1.285 (W)

Table 5.2, power losses in the inductors

The inductor losses for power levels within these range will be determined by linear interpolation.

5.1.2 Simulation results of the SEPIC PFC

In this section the simulation results will be discussed. Since the minimum input voltages equals $452\ V$ (for low line) the maximum input voltage will be $700\ V$ (for high line). Simulations will be done for both high as low line and for different power ratings. The results are shown in the tables 5.3 - 5.6.

Pout	Rload	Conduction losses (W) Vin = 700 V							Switching loss (W)			Ptot	Pin	Efficiency (%)
		La	Lb	C	Diode	IGBT	Rsense	Total	IGBT on	IGBT off	Total			
100	2025,00	0,92	0,47	0,03	0,20	0,30	0,58	2,50	15,57	12,48	28,05	30,55	130,55	76,60
150	1350,00	1,14	0,63	0,08	0,32	0,49	0,91	3,58	10,39	12,64	23,04	26,62	176,62	84,93
200	1012,50	1,37	0,80	0,14	0,46	0,71	1,26	4,72	7,80	12,73	20,53	25,25	225,25	88,79
250	810,00	1,59	0,96	0,21	0,60	0,94	1,61	5,91	6,25	12,78	19,03	24,95	274,95	90,93
300	675,00	1,81	1,12	0,31	0,75	1,19	1,98	7,16	5,21	12,83	18,04	25,20	325,20	92,25

Table 5.3, Power losses under high line conditions and an IGBT as switch

Pout	Rload	Conduction losses (W) Vin = 700 V							Switching loss (W)			Ptot	Pin	Efficiency (%)
		La	Lb	C	Diode	MOS	Rsense	Total	MOS on	MOS off	Total			
100	2025,00	0,92	0,47	0,03	0,20	0,71	0,58	2,91	1,08	1,13	2,21	5,12	105,12	95,13
150	1350,00	1,14	0,63	0,08	0,32	1,60	0,91	4,69	0,72	1,12	1,84	6,53	156,53	95,83
200	1012,50	1,37	0,80	0,14	0,46	2,84	1,26	6,85	0,54	1,12	1,66	8,51	208,51	95,92
250	810,00	1,59	0,96	0,21	0,60	4,45	1,61	9,42	0,43	1,11	1,55	10,97	260,97	95,80
300	675,00	1,81	1,12	0,31	0,75	6,43	1,98	12,39	0,36	1,11	1,47	13,86	313,86	95,59

Table 5.4, Power losses under high line conditions and a MOSFET as switch

Pout	Rload	Conduction losses (W) Tcase=152 °C							Switching loss (W)					
		La	Lb	Lc	Diode	IGBT	Rectifier	Total	IGBT-on	IGBT-off	Total	Total loss	Pin	Efficiency (%)
100	2025,00	0,92	0,47	0,05	0,21	0,48	0,94	3,08	9,54	9,97	19,51	22,59	122,59	81,57
150	1350,00	1,14	0,63	0,11	0,34	0,80	1,48	4,51	6,37	10,07	16,44	20,95	170,95	87,74
200	1012,50	1,37	0,80	0,20	0,48	1,15	2,05	6,05	4,78	10,13	14,90	20,95	220,95	90,52
250	810,00	1,59	0,96	0,32	0,63	1,55	2,63	7,68	3,82	10,16	13,98	21,65	271,65	92,03
300	675,00	1,81	1,12	0,47	0,79	1,98	3,22	9,39	3,19	10,19	13,38	22,77	322,77	92,95

Table 5.5, Power losses under low line conditions and an IGBT as switch

Pout	Rload	Conduction losses (W) Tcase=152 °C							Switching loss (W)					
		La	Lb	Lc	Diode	MOS	Rectifier	Total	MOS-on	MOS-off	Total	Total loss	Pin	Efficiency (%)
100	2025,00	0,92	0,47	0,05	0,21	1,37	0,94	3,96	0,29	0,72	1,02	4,98	104,98	95,26
150	1350,00	1,14	0,63	0,11	0,34	3,08	1,48	6,80	0,19	0,72	0,91	7,71	157,71	95,11
200	1012,50	1,37	0,80	0,20	0,48	5,50	2,05	10,40	0,15	0,71	0,86	11,25	211,25	94,67
250	810,00	1,59	0,96	0,32	0,63	8,63	2,63	14,76	0,12	0,70	0,82	15,58	265,58	94,13
300	675,00	1,81	1,12	0,47	0,79	12,50	3,22	19,91	0,10	0,69	0,79	20,70	320,70	93,54

Table 5.6, Power losses under low line conditions and a MOSFET as switch

The two graphs below show the overall efficiency for high and low line conditions and with an IGBT or MOSFET as switch.

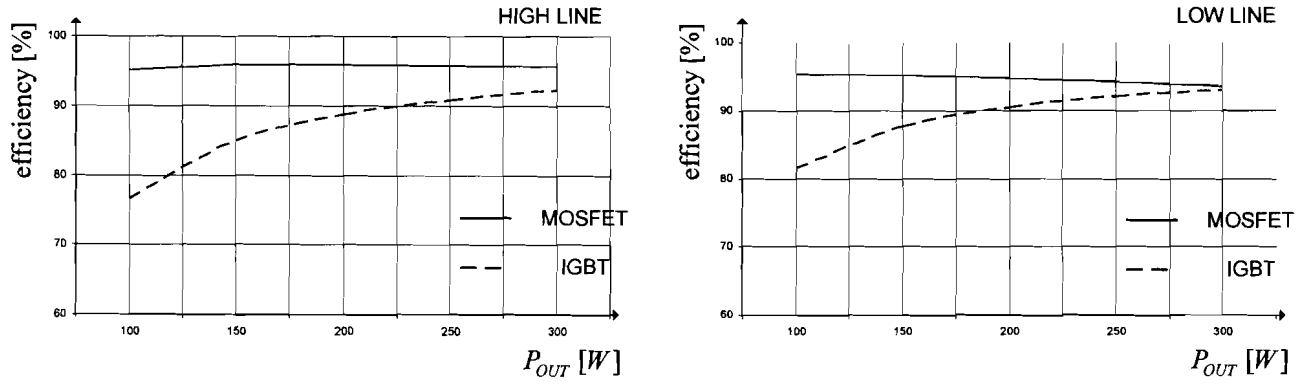
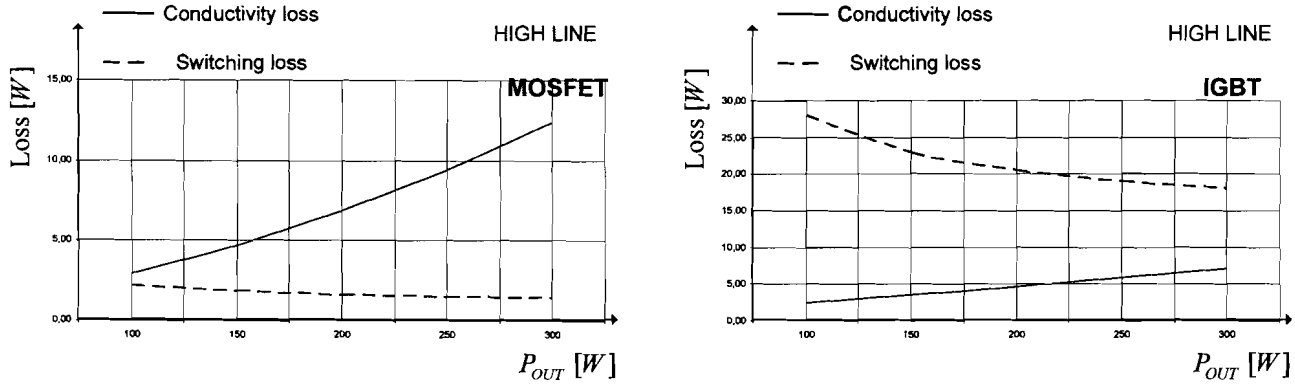


Figure 5.3, Efficiency as function of the output power for high line (left hand) and low line (right hand) conditions.

In Fig 5.4 are the conduction (including the magnetic losses) losses versus the switching losses shown for high line conditions.



5.4, Conduction loss versus switching loss for high line conditions with an MOSFET (left hand) or IGBT (right hand) as switch.

It can be observed from the tables and the graphs, that the efficiency of the SEPIC PFC with an IGBT as switch is low at low power ratings. This is caused by the high switching losses of the IGBT, especially under low power and high line conditions when the switching frequency is very high.

The switching losses of the MOSFET are acceptable and way lower than the IGBT's switching losses. For high output power and low line conditions however, the switching losses for both switches decrease and the conduction losses become more significant. Under these conditions the current stress becomes larger and since the conduction loss for the MOSFET increases with the square of the current while the conduction loss of the IGBT increases almost linear with the current, the difference in efficiency becomes smaller.

Although the efficiency of the SEPIC PFC with an IGBT switch becomes better at higher power levels in the specified power range the MOSFET will perform better and is thus preferable above the IGBT.

5.1.3 Components of the Low stress Buck Boost PFC

The Low stress Buck Boost PFC contains nine components; a bridge rectifier, two switches, two diodes, two inductors and two capacitors. As in the case of the SEPIC PFC, the buffer capacitor will not be modelled.

For simplicity, the same inductors and series capacitor are used, the components used in the LsBB PFC are:

Switches	Diode	Series capacitor	Inductor A	Inductor B
STP5NK80 or IGB03N120H2	MUR480	MKP1840 200nF	2 mH	4 mH

Table 5.7, used components in the LsBB PFC

Since the voltage stress of the switches and diodes is lower, other devices are applied. For the switch a STP5NK80 MOSFET from ST is used or an IGB03N120H2 from Infineon. The MOSFET can handle voltages up to $800\ V$ and a continuous currents up to $4.3\ A$. The typical drain source resistance equals $1.9\ \Omega$. The IGBT can handle voltages up to $1200\ V$ and a continuous currents up to $3\ A$. For the diode an MUR480 from MCC is used which is capable for average currents up to $4\ A$ and voltages of $800\ V$. The used components are the better components commercially available.

Since the $R_{DS_{ON}}$ of the MOSFET can be considered constant (for a constant temperature) and the fall time of the MOSFET will be considered constant, it is not necessary to model the switching and conduction losses by tables or curve fitting procedures as done for the

IGBT. For the diode however, another device is used (MUR480) and its voltage-current characteristic is shown below:

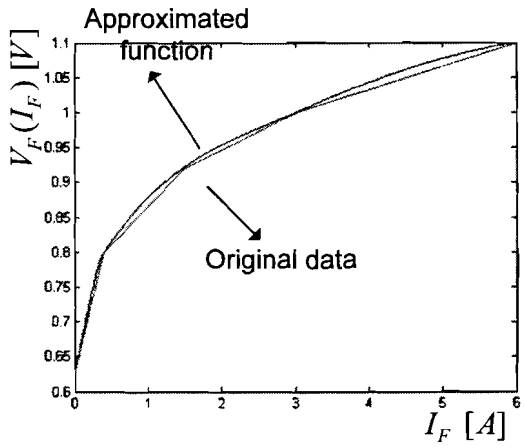


Figure 5.5, Approximated function and original data of voltage-current characteristic of the MUR480.

Although it is not the most optimal choice, the same inductors as in the SEPIC PFC are also used in the LsBB PFC. The loss in the inductors is determined in the same way as for the SEPIC PFC, both the high line and low line inductor loss is determined by MATLAB/MAGTOOL simulations. The results are shown below:

	High line and low power	Low line and high power
Loss in inductor A	0.334 (W)	1.205 (W)
Loss in inductor B	0.077 (W)	0.545 (W)

Table 5.8, power losses in the inductors.

5.1.4 Simulation results of the Low stress Buck Boost PFC

In this section the simulation results of the Low stress Buck Boost PFC will be discussed. This will be done in the same manner as done for the SEPIC PFC. For both high line and low line conditions the results are shown in the tables 5.9 - 5.12.

Pout	Pload	Conduction losses (W)							Switching loss (W)			Total loss	Efficiency	
		Boost	Lb	Buck	Diode	IGBT	Snubber	Total	Diode	IGBT/FET	Total			
100	2025,00	0,33	0,08	0,00	0,11	0,20	0,58	1,31	10,86	4,71	15,56	16,87	116,87	85,56
150	1350,00	0,55	0,20	0,01	0,18	0,37	0,91	2,21	7,23	4,85	12,09	14,30	164,30	91,30
200	1012,50	0,77	0,32	0,01	0,25	0,68	1,26	3,17	5,39	4,92	10,32	13,49	213,49	93,68
250	810,00	0,99	0,43	0,01	0,29	0,74	1,61	4,07	4,31	4,93	9,23	13,30	263,30	94,95
300	675,00	1,21	0,55	0,02	0,39	1,09	1,98	5,23	3,58	4,98	8,56	13,78	313,78	95,61

Table 5.9, Power losses under high line conditions and an IGBT as switch.

Pout	Rload	Conduction losses (W) Vlow=700 V							Switching loss (W)			Total loss	Pin	Performance (%)
		La	Lb	C	Diode	MOS	Rectifier	Total	MOS on	MOS off	Total			
100	2025,00	0,33	0,08	0,00	0,11	0,17	0,58	1,28	1,33	0,09	1,42	2,70	102,70	97,37
150	1350,00	0,55	0,20	0,01	0,18	0,37	0,91	2,22	0,91	0,09	1,00	3,22	153,22	97,90
200	1012,50	0,77	0,32	0,01	0,25	0,66	1,26	3,26	0,69	0,09	0,79	4,05	204,05	98,02
250	810,00	0,99	0,43	0,01	0,29	0,93	1,61	4,26	0,51	0,08	0,60	4,86	254,86	98,09
300	675,00	1,21	0,55	0,02	0,39	1,48	1,98	5,62	0,48	0,09	0,58	6,19	306,19	97,98

Table 5.10, Power losses under high line conditions and a MOSFET as switch.

Pout	Rload	Conduction losses (W) Vlow=452 V							Switching loss (W)			Total loss	Pin	Performance (%)
		La	Lb	C	Diode	IGBT	Rectifier	Total	IGBT on	IGBT off	Total			
100	2025,00	0,33	0,08	0,03	0,20	0,20	0,94	1,78	6,83	7,43	14,26	16,04	116,04	86,17
150	1350,00	0,55	0,20	0,06	0,32	0,37	1,48	2,98	4,53	7,53	12,06	15,04	165,04	90,89
200	1012,50	0,77	0,32	0,10	0,44	0,58	2,05	4,25	3,39	7,57	10,96	15,21	215,21	92,93
250	810,00	0,99	0,43	0,17	0,57	0,82	2,63	5,60	2,70	7,42	10,13	15,73	265,73	94,08
300	675,00	1,21	0,55	0,25	0,69	1,09	3,22	7,01	2,24	7,41	9,66	16,66	316,66	94,74

Table 5.11, Power losses under low line conditions and an IGBT as switch

Pout	Rload	Conduction losses (W) Vlow=452 V							Switching loss (W)			Total loss	Pin	Performance (%)
		La	Lb	C	Diode	MOS	Rectifier	Total	MOS on	MOS off	Total			
100	2025,00	0,33	0,08	0,03	0,20	0,31	0,94	1,89	0,15	0,31	0,46	2,35	102,35	97,70
150	1350,00	0,55	0,20	0,06	0,32	0,69	1,48	3,30	0,15	0,31	0,46	3,75	153,75	97,56
200	1012,50	0,77	0,32	0,10	0,44	1,23	2,05	4,90	0,14	0,31	0,45	5,36	205,36	97,39
250	810,00	0,99	0,43	0,17	0,57	1,98	2,63	6,76	0,14	0,30	0,45	7,21	257,21	97,20
300	675,00	1,21	0,55	0,25	0,69	2,86	3,22	8,78	0,14	0,30	0,44	9,22	309,22	97,02

Table 5.12, Power losses under low line conditions and a MOSFET as switch

A graphical representation of the overall efficiency is shown in Fig 5.5.

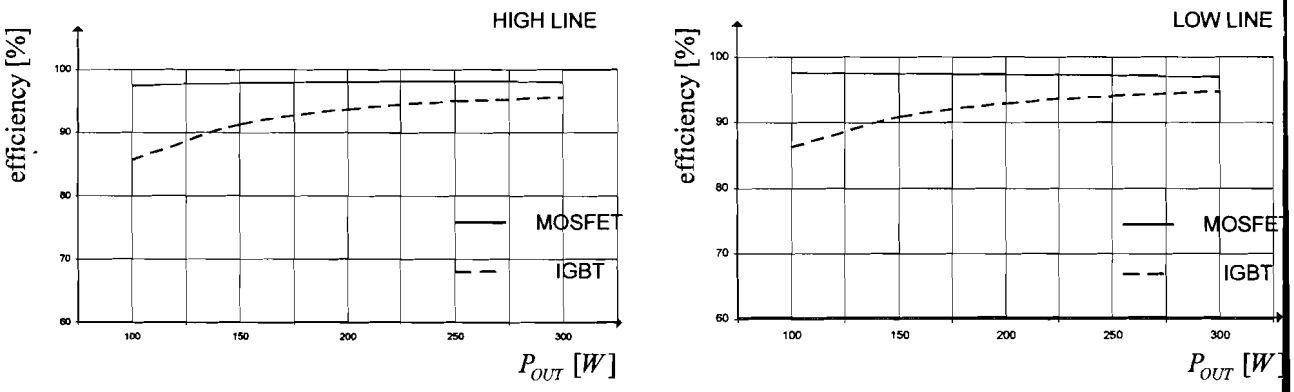


Figure 5.5, Efficiency as function of the output power for high line (left hand) and low line (right hand) conditions.

In Fig 5.6 are the conduction (including the magnetic losses) losses versus the switching losses shown for high line conditions only.

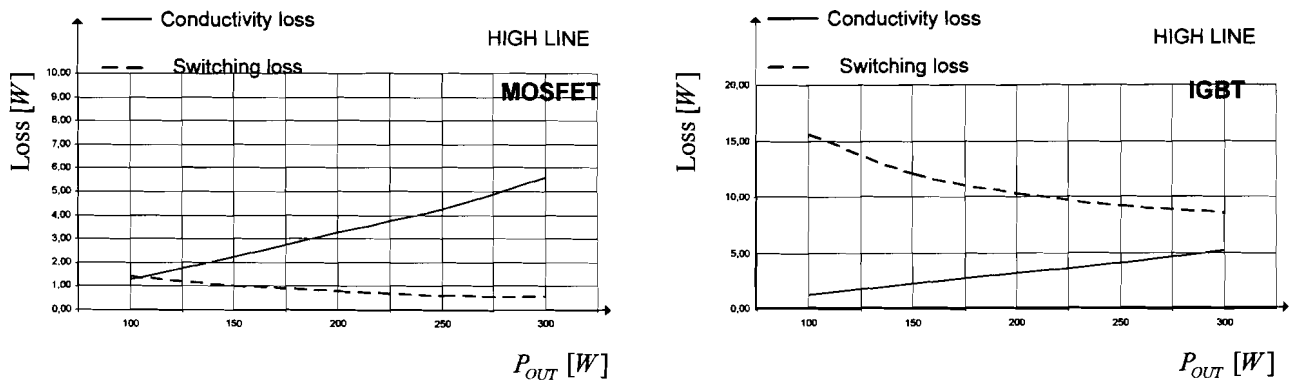


Figure 5.6, Conduction loss versus switching loss for high line conditions with an MOSFET (left hand) or IGBT (right hand) as switch.

As can be observed from the tables and figures, applying a IGBT as switch in the Low stress Buck Boost PFC will result into a low efficiency at low power ratings. Similar as with the SEPIC PFC, under low load conditions the switching frequency increases, which will result in IGBT switching losses. Although, the conductivity loss of a MOSFET increases at higher power levels, the overall efficiency of a LsBB with a MOSFET as switch is still better.

5.1.5 The SEPIC PFC versus the Low stress Buck Boost PFC

In the previous sections the efficiency of the SEPIC PFC and Low stress Buck Boost PFC is discussed. From those results it can be concluded that an IGBT is not suitable in this power range. In this section the efficiency of the SEPIC PFC and Low stress Buck Boost PFC will be compared with each other.

In the figure below the efficiency for both the high line as the low line situation is shown.

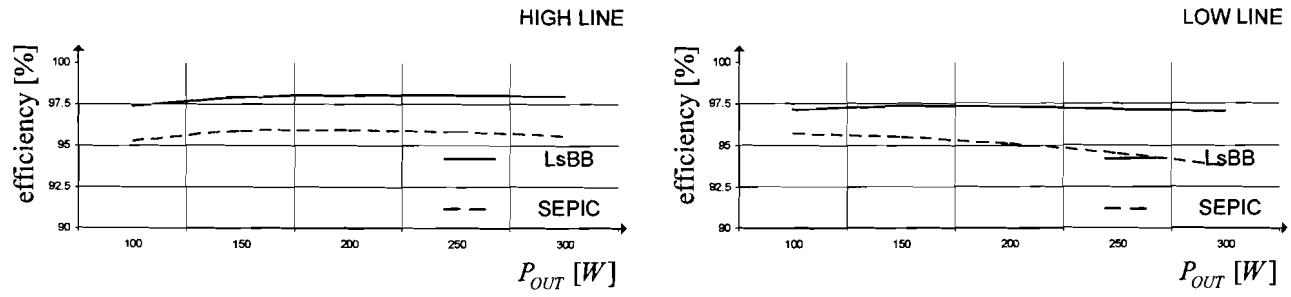


Figure 5.7, The efficiency of the Low stress Buck Boost PFC versus the SEPIC PFC.

As can be observed from the Fig 5.7, the efficiency of the Low stress Buck Boost PFC is around the 97.5 % while the efficiency of the SEPIC PFC is around the 95 %.

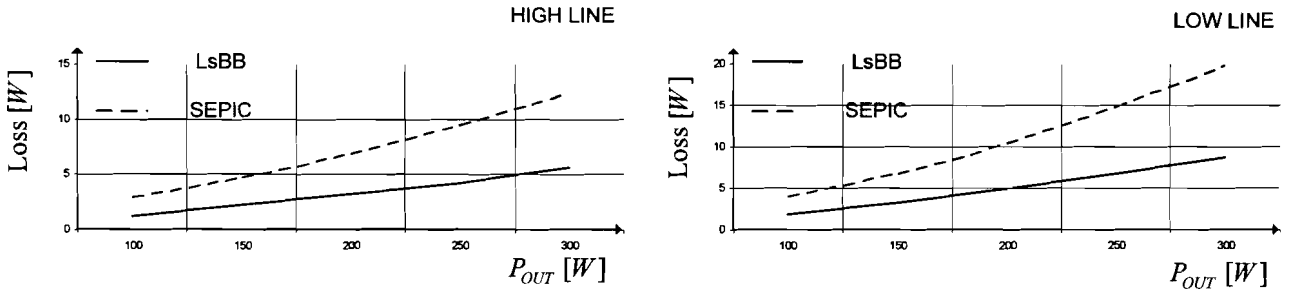


Figure 5.8, Conduction losses for high and low line conditions.

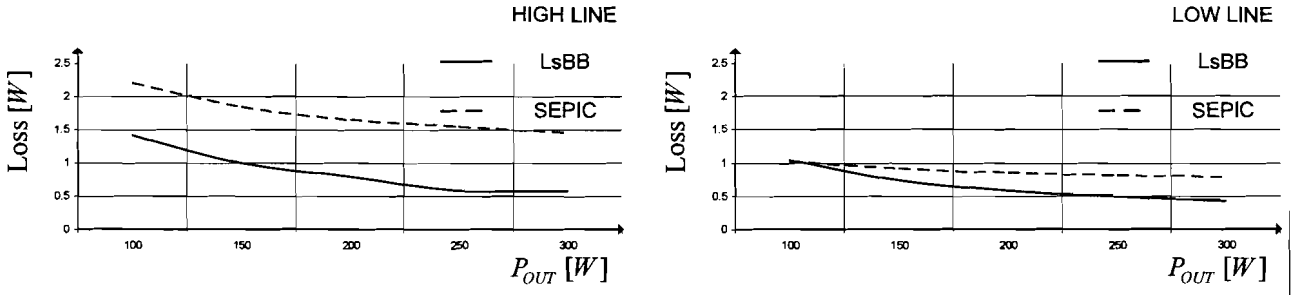


Figure 5.9, Switching losses for high and low line conditions.

As can be observed from Fig. 5.8, the conduction losses increase when the output power increases. At high power levels, the drain source resistance is dominating which causes a power loss increasing with the square of the current. The conduction loss of the LsBB is lower than the conduction loss of the SEPIC across the whole power range and under both conditions. This can be explained by the larger drain source resistance of the MOSFET used in the SEPIC PFC and the large current stresses in the SEPIC PFC.

Fig 5.9 shows that the switching loss decreases when the desired output power increases. At low power levels, the switching frequency is high which causes more switching loss. Fig. 5.9 also shows that the switching loss in the SEPIC PFC is higher when comparing it with the LsBB PFC. This can be explained by the higher stress and switching frequency in the SEPIC PFC.

It can be concluded that the efficiency of the LsBB PFC is better than the SEPIC PFC. In both topologies the efficiency is dominated by the switch (MOSFET). The voltage stress of the switches in the LsBB is lower which makes its possible to apply medium voltage (about 700 V) MOSFETs with a lower drain source resistance. The lower voltage stress also reduces the switching losses. The SEPIC PFC has a worse efficiency than the LsBB PFC, but the difference is not that large. The main problem of the SEPIC PFC is that under worst case conditions the switch will dissipate more than 13 W which is more than one half of the total amount of power dissipated. This also means that future improvements of MOSFET's (or other semiconductor switches) will lead into a significantly better efficiency of the SEPIC PFC.

6 CHAPTER 6 DESIGN OF THE LOW STRESS BUCK BOOST PFC

In this chapter the circuit of the Low stress Buck Boost PFC will be discussed. The first part explains the control circuit, in the second part the selected components for the 'power' stage are discussed.

6.1 CONTROLLING THE LOW STRESS BUCK BOOST PFC

Before treating the details of the PFC (see APPENDIX D for the complete schematic), for simplicity the PFC first will be discussed on a functional level. It can be subdivided in eight parts:

- Power converter
- Mode selector
- Zero current detecting circuit
- Current sensing circuit
- Voltage regulator circuit
- Current shaper circuit
- PWM modulator
- Gate driver

A semi-functional block schematic is shown in Fig 6.1.

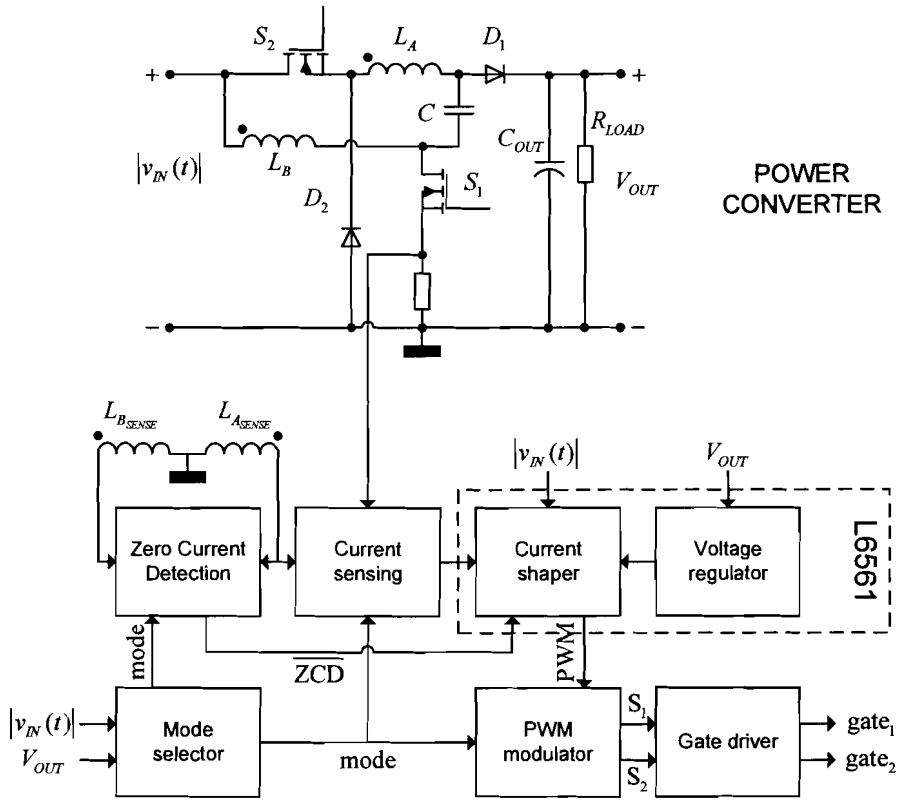


Figure 6.1, Functional schematic of the LsBB PFC.

Note that the inductors L_A and $L_{A_{SENSE}}$ and L_B and $L_{B_{SENSE}}$ are coupled with a high coupling ratio (approximately unity).

6.1.1 Mode selector circuit

The mode selector measures the actual input and output voltage of the PFC and decides in which mode the PFC should operate.

Mode	Condition
Boost	$v_{IN}(t) < V_{OUT} - V_{OFFSET}$
Buck Boost	$V_{OUT} - V_{OFFSET} \le v_{IN}(t) \le V_{OUT} + V_{OFFSET}$
Buck	$V_{OUT} + V_{OFFSET} < v_{IN}(t)$

Table 6.1 Average input currents for the different modes

Where the buck boost mode is in fact introduced by V_{OFFSET}. The (simplified) circuit is shown in Fig 6.2.

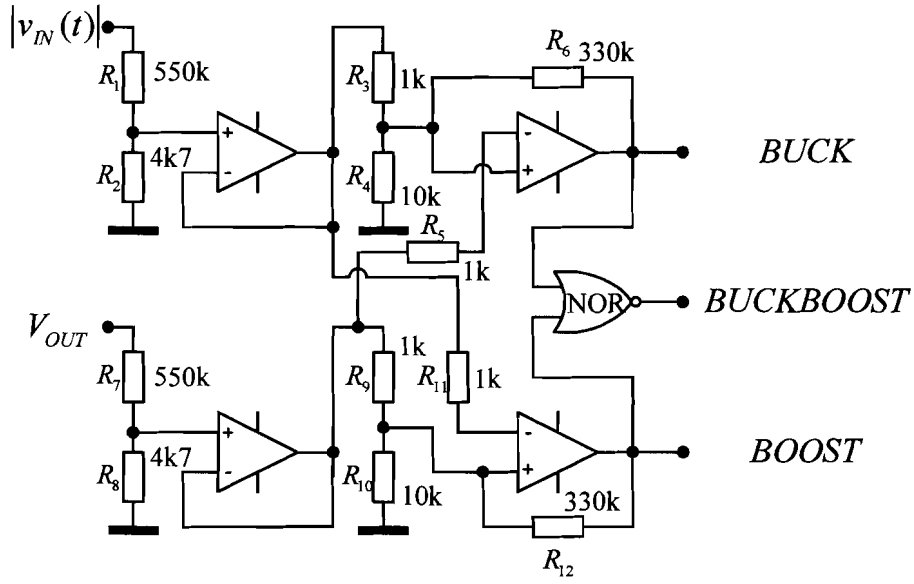


Figure 6.2, Mode selector circuit.

First, the high voltages are scaled downwards to voltages below five volts by a simple resistive divider, then both voltages are buffered. In the second stage an offset voltage is introduced by R_3 and R_4 for the buck mode and R_9 and R_{10} for the boost mode. The function off R_6 and R_{12} is to add some hysteresis. When the PFC is not operating in the boost mode or in the buck mode, the PFC must operate in the buck boost mode, this is realised by the NOR gate.

6.1.2 Zero current detection circuit

The zero current detection detects when the current through the inductors has become zero, When the current has become zero, the ZCD 'pin' becomes high. In the buck mode, only the zero crossing of the buck inductor needs to be detected. In the boost and buck boost mode both inductor current must be zero before the ZCD 'pin' becomes high. Since there are two inductors two detectors are needed. One of them is shown on the left hand of Fig. 6.2.

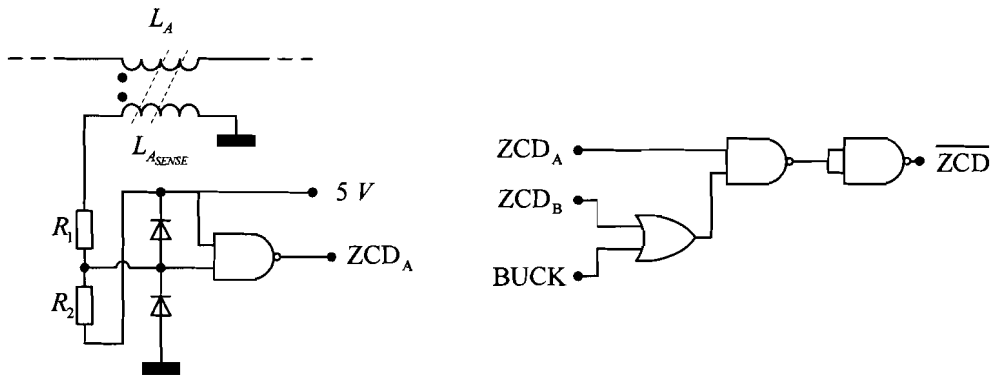


Figure 6.2, Zero current detection circuit.

If the voltage across L_A is positive, the voltage across $L_{A_{SENSE}}$ is positive too and vice versa. The resistors R_1 and R_2 are dimensioned in such way the ZCD_A is low when the inductor voltages are positive and high when the voltages are negative. Over voltage protection for the NAND gate is provided by the clamping diodes.

As mentioned earlier, only L_A is used during the buck mode this implicates that the zero current information of L_A may not be used (this would lead to instability). This will be done by the circuit shown on the right hand side of Fig. 6.2.

6.1.3 Current sensing circuit

To shape the input current properly, the input current must be sensed. In the boost and buck-boost mode this can be done by simply placing a resistor between the ground and the source of the MOSFET. However in the buck mode, high side current sensing is necessary, which will be done by an integrator.

When the PFC is operating in the boost mode, the boost-switch will be turned off after the current through the inductors has reached $\hat{I}_{PEAK}$ (which is determined by the controller). A shunt resistor between the ground and the source is providing a voltage which is proportional to the inductor current. This is shown in Fig. 6.1.

In the buck mode it is hard to sense the current with a shunt resistor since it must be done at the high side. An advantage of the BCM is that the current through the inductor is always zero when the MOSFET is turned on. The inductor current is in fact the integrated input voltage, thus a integrator circuit as shown in Fig. 6.3 can emulate a voltage which is proportional with the current through the inductor.

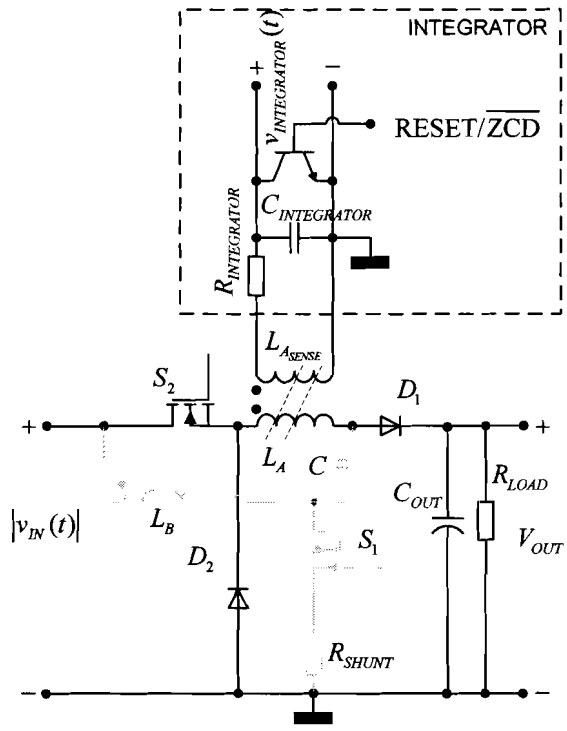


Figure 6.3, Current sensing by a integrator circuit.

When the MOSFET is switched off, the RESET/$\overline{\text{ZCD}}$ pin is high, so $v_{INTEGRATOR} = 0$. When the MOSFET is switched on, the current through the inductor starts increasing from 0:

$$i_{L_A}(t) = \frac{1}{L_A}\int_0^t v_{L_A}(t)d\tau = \frac{v_{L_A}(t)}{L_A}t \tag{1.153}$$

At the same moment the RESET/ZCD pin has become low and the $v_{INTEGRATOR}(t)$ starts increasing. Assuming the voltage across the secondary winding is much larger than $v_{INTEGRATOR}(t)$, $v_{INTEGRATOR}(t)$ can be described by:

$$v_{INTEGRATOR}(t) = \frac{1}{C_{INTEGRATOR}}\int_0^t \frac{kv_{L_A}(t)}{\alpha R_{INTEGRATOR}}d\tau = \frac{kv_{L_A}(t)}{\alpha C_{INTEGRATOR}R_{INTEGRATOR}}t\,. \tag{1.154}$$

Where $\alpha = N_A / N_{A_{SENSE}} = \sqrt{L_A / L_{A_{SENSE}}}$ is the winding ratio and k the coupling factor. By dividing (1.153) by (1.154) and assuming $k = 1$, the ratio between the actual current and the integrator voltage can be determined:

$$\frac{i_{L_A}(t)}{v_{INTEGRATOR}(t)} = \frac{\alpha C_{INTEGRATOR} R_{INTEGRATOR}}{L_A} = \zeta . \tag{1.155}$$

Now the inductor current can be written as function of the integrator voltage:

$$i_{L_A}(t) = \frac{\alpha C_{INTEGRATOR} R_{INTEGRATOR}}{L_A} v_{INTEGRATOR}(t) = \zeta v_{INTEGRATOR}(t) . \tag{1.156}$$

In the boost and buck boost mode, the control current is sensed by a shunt resistor and in the buck mode it is emulated by an integrator. To obtain a smooth transition from the buck boost to the buck mode and vice versa, the sensed voltage across the shunt resistor at the end of the boost mode must approximate the integrator voltage at the beginning of the buck mode. The voltage across the shunt at that moment equals:

$$v_{SHUNT}(t) = R_{SHUNT} i_{SWITCH}(t) \tag{1.157}$$

and the integrator voltage equals:

$$v_{INTEGRATOR}(t) = \frac{L_A}{\alpha C_{INTEGRATOR} R_{INTEGRATOR}} i_{L_A}(t) . \tag{1.158}$$

To obtain a smooth transition between the modes, equation (1.159):

$$\frac{v_{SHUNT}(t)}{i_{L_A}(t)} = R_{SHUNT} = \frac{v_{INTEGRATOR}(t)}{i_{L_A}(t)} = \frac{L_A}{\alpha C_{INTEGRATOR} R_{INTEGRATOR}} \Rightarrow R_{SHUNT} = \frac{L_A}{\alpha C_{INTEGRATOR} R_{INTEGRATOR}} \tag{1.159}$$

must be satisfied.

6.1.4 Voltage regulator / current shaper circuit

These circuits are constructed around a dedicated PFC controller, the L6561. The simplified interior of the L6561 with some external components is shown in Fig 6.4.

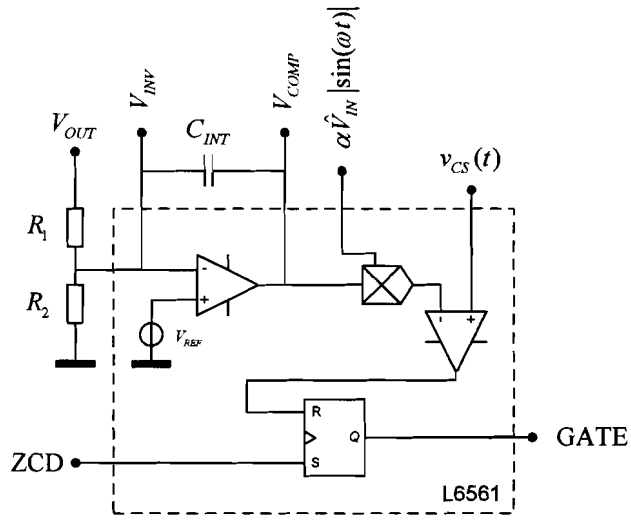


Figure 6.4, Simplified L6561.

On the left hand side of Fig. 6.4, a PI controller is shown which is configured by C_{INT}, R_1 and R_2.

On the right hand side the current shape controller is shown, which only contains a comparator and a set-reset flip flop. As long as $v_{CS}(t)$ is smaller than the low frequency signal applied at the '–' pin of the comparator, the flip flop will not reset. When it becomes larger, the flip flop will reset and will be turned on again after ZCD has been triggered.

The signal applied at the '–' pin of the comparator is a multiplication of the rectified input voltage and the output of the PI controller. When the load of the PFC is increased, the output voltage will decrease. As a result the PI controller will increase the voltage at the $COMP$ pin and the (average) input current will increase. Finally a new equilibrium will be established.

In order to maintain an unity power factor, the controller may not compensate for 100 Hz ripple at the output. So the bandwidth from the output to the output must be far below the 100 Hz (in other words, the regulator may not compensate for a 100 Hz ripple at the output).

First an attempt was made for modelling the regulator in MATLAB. Although the bode-diagram of the MATLAB model had was similar with the bode-diagram of the (behavioural) Spice simulations, the bode-diagrams didn't match perfectly and it seemed the MATLAB model was not valid. In the end the right values for C_{INT} and R_1 were found by some Spice simulations.

6.1.5 PWM Modulator

The PFC control ic, the L6561, contains only one gate driver. Since the LsBB has two switches which must be driven independently, the output of the L6561 must be multiplexed. In the boost mode, one switch must be closed (the buck switch) and the other is driven by a PWM signal. In the buck boost mode, both switches are driven simultaneously and in the buck mode only the buck switch is PWM driven and the boost switch is turned off. These conditions are summarized in Table 6.2.

Mode	Buck switch	Boost switch
Boost	ON	PWM
Buck boost	PWM	PWM
Buck	PWM	OFF

Table 6.2 Multiplexing scheme for the different modes

This can easily be done by the logic devices which are shown in Fig. 6.9.

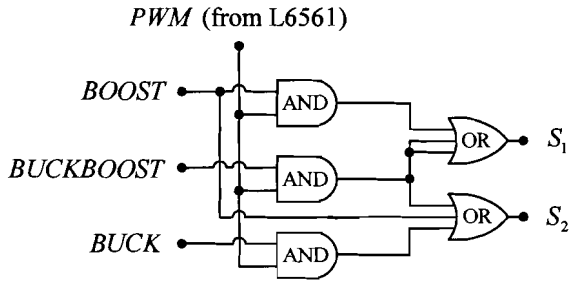


Figure 6.9, PWM modulator circuit.

6.1.6 Gate driver

The gates are driven by the IR2113. This ic contains a low and a high side gate driver. For the high side driver, a so called bootstrap is needed which is floating with respect to the source of the buck switch and so must be separated from ground. For this application a very small flyback converter is designed.

6.2 COMPONENTS OF THE LOW STRESS BUCK BOOST PFC

In this section the component choice of the PFC will be explained briefly.

6.2.1 Inductors

The LsBB PFC contains two inductors, L_A and L_B. In the boost mode, the inductors are connected in parallel. To reduce the conductivity losses in the boost mode as much as

possible, the inductance of both inductors must be the same. As mentioned in chapter 3, the switching frequency will be at its lowest in the buck mode. The inductors are designed in such a way, the switching frequency will never be lower than $30\ kHz$ this results in an inductance of $1.8\ mH$. The maximum current through the buck inductor equals $2.5\ A$, the inductors should not saturate at this value.

Combining these demands result in a inductor constructed around an E-core. The design parameters of the inductors are summarized below.

- E25/13/11
- 120 turns with $6 \times 0.2\ mm$ litze
- Inductance $1.8\ mH$
- Airgap $3\ mm$
- 3C92 core material

6.2.2 Series capacitor

As mentioned in chapter three, there is a ripple voltage across this capacitor in the boost mode which depends on its size. The larger the capacitor, the smaller the ripple. However, in the transition from the buck boost mode to the buck mode, a transient occurs. The 'size' of the transient can be reduced by making the capacitor as small as possible. To satisfy both demands, a compromise must be found. If maximum allowed ripple across the capacitor equals $25\ V$ a capacitor with a capacity $42\ nF$ is sufficient.

6.2.3 Diodes

For the diodes in the PFC two MUR480 diodes are chosen. These diodes can handle average currents up to $4\ A$ and voltages up to $800\ V$. For the bridge rectifier four BYR29X types are used.

6.2.4 Switches

Two STP5NK80 MOSFETS are applied as switch, this types can handle voltages up to $800\ V$ and average currents up to $4.3\ A$. The typical drain-source resistance of these devices is $1.9\ \Omega\ @25^{o}C$.

6.2.5 Output capacitor

Two $33\ \mu\mathrm{F}$ elcap's are applied as output capacitor. The value of these capacitors is based on other designs in the same power range.

7 MEASUREMENT RESULTS

In this chapter the measurement results will be discussed. First the efficiency will be discussed. After that the details will be discussed.

7.1 EFFICIENCY MEASUREMENT

For the efficiency measurements both high and low line situations are measured. The output power is measured by two ordinary multimeters. The input power however, is independently measured by a Power Analyzer and oscilloscope (in combination with MATLAB). The THD is determined by the Power Analyzer.

For high line conditions the results are shown in Table 7.1.

Pout	Rload	Pin		Vout	Iout	Pout	efficiency (%)	THD (%)
		Power Analyzer	Oscilloscope					
150	500 Ohm	150.92	-	268.22	0.54	145.38	96.33	16.44
		-	150.25	268.20	0.54	145.10	96.57	
75	1000 Ohm	75.30	-	268.24	0.27	72.69	96.54	22.69
		-	75.88	268.25	0.27	72.96	96.15	

Table 7.1 High line results ($V_{IN_{RMS}} = 305\ V$)

For the low line conditions the results are shown in Table 7.2.

Pout	Rload	Pin		Vout	Iout	Pout	efficiency (%)	THD (%)
		Power Analyzer	Oscilloscope					
150	500 Ohm	153.42	-	268.23	0.54	145.38	94.76	9.57
		-	153.18	268.22	0.54	145.11	94.73	
75	1000 Ohm	76.30	-	268.24	0.27	72.69	95.27	7.47
		-	77.13	268.23	0.27	72.96	94.60	

Table 7.2 Low line results ($V_{IN_{RMS}} = 220\ V$)

As can be observed from the tables, the high line efficiency is better than the low line. Under low line conditions the PFC is only operating in two modes; the boost and buck boost. The buck boost mode causes large stresses and is therefore not efficient. Under high line conditions the PFC also operates in buck mode which is more efficient but also introduces a large amount of harmonic distortion.

7.2 CURRENT WAVEFORMS

In Fig. 7.1 high frequency current for high line conditions is shown.

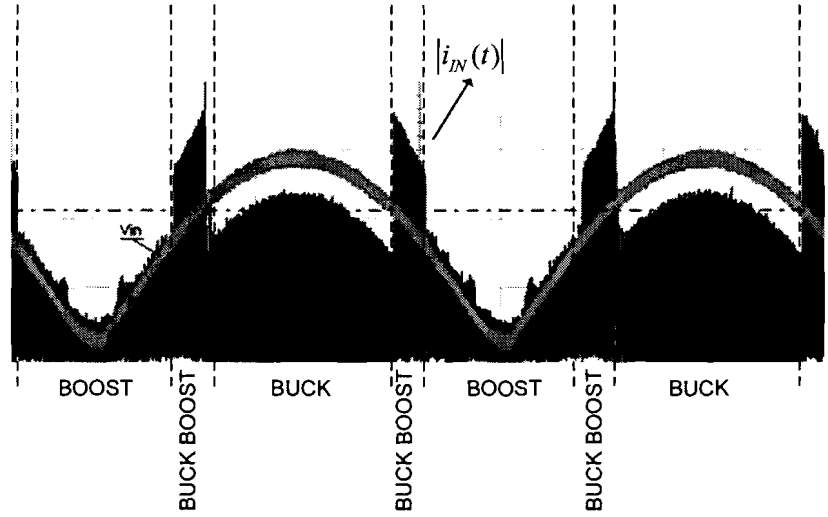


Figure 7.1, High frequency current under high line conditions.

In the buck boost mode the controller is pre-compensated (this is not done in the analysis in chapter 3) to reduce distortion. This results in the higher peak currents shown. During the buck mode, the peak current is somewhat lower than in the boost mode. This is caused by delays of the circuit; in the boost mode the switching frequency is much higher than in the buck mode. Small delays will have more effect in the boost mode than in the buck mode.

For low line conditions the high frequency current is shown in Fig 7.2.

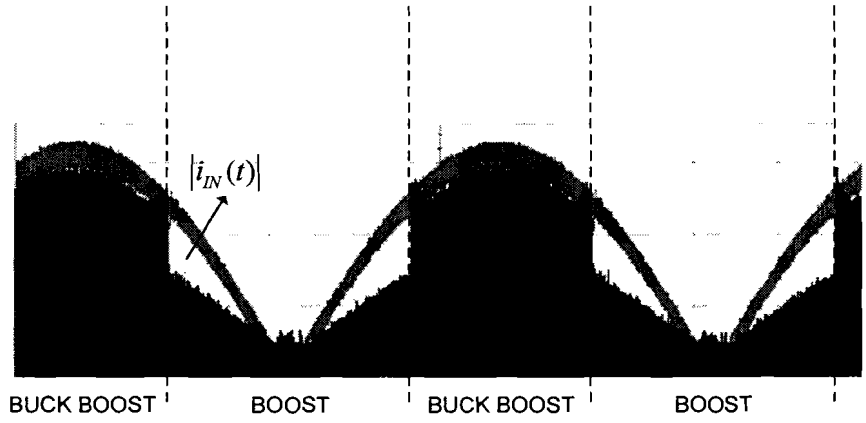


Figure 7.2, High frequency current for high low conditions.

As can be observed from Fig 7.2, the peak current during the buck boost mode is much higher than during the boost mode. This will cause more losses.

The average (filtered) input current for high line conditions is shown in Fig 7.3.

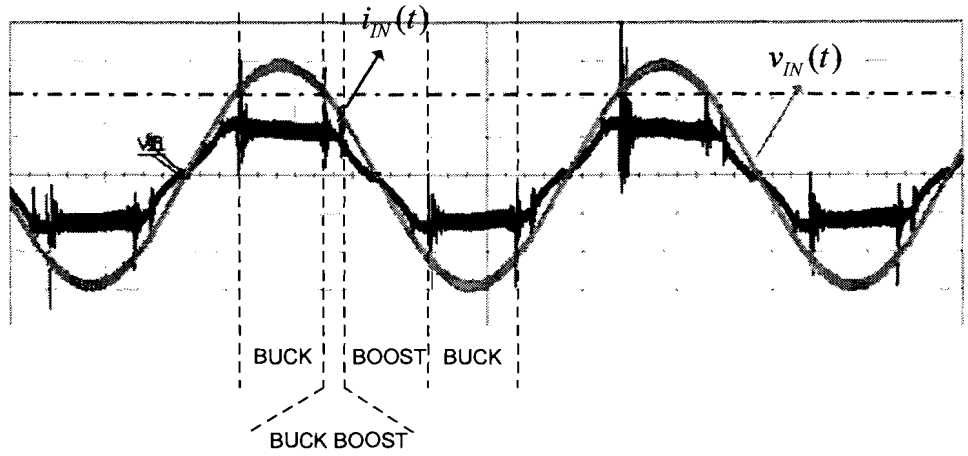


Figure 7.3, Input current for high line conditions, $V_{IN_{RMS}} = 305\ V$, $P_{OUT} = 150\ \text{W}$.

The input current is 'knotted'. This is expected and described in section 3.4. Note that the peak current during the buck boost mode is multiplied (compensated) by a factor of 2 (this is not done in section 3.4) for obtaining a smooth transition between the modes.

Also two transients are visible between the transition form the buck boost to the buck mode and vice versa. During the buck boost mode, the series capacitor (C) is charged as discussed in section 3.3.2.3. In the buck mode the capacitor will be discharged and resonate with L_B and probably the input filter. This is because in Fig 7.1 (the high frequency input current) there is are no transients or other resonances visible.

For low line situations however, the input current is more sinusoidal and shown in Fig 7.4.

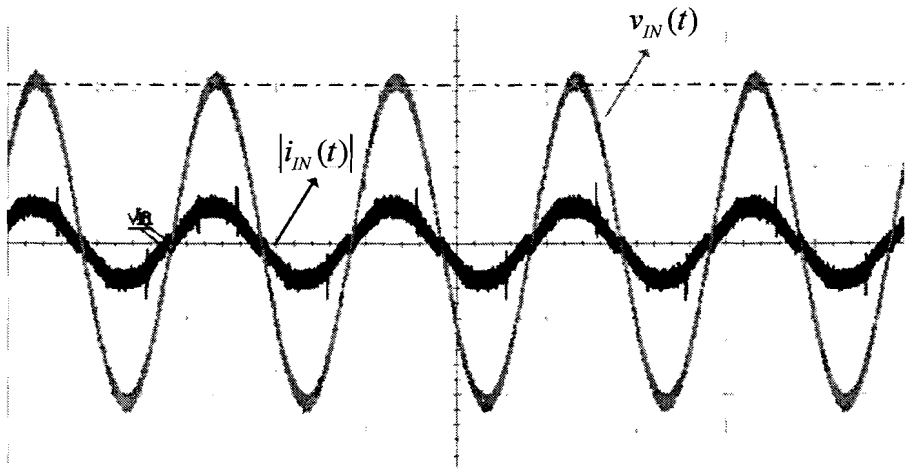


Figure 7.4, Input current under low line conditions $V_{IN_{RMS}} = 220\ V$, $P_{OUT} = 75\ \text{W}$.

This explains why the THD of the PFC is much better under low line conditions than under high line conditions. Even since there is no transition from buck boost to buck mode and vice versa, there is no transient.

7.3 CAPACITOR VOLTAGE

As mentioned in the previous section (and in section 3.3.2.3) the series capacitor is charged during the buck boost mode, resulting in a transient in the buck mode. This charging process (in a line cycle) is shown in Fig 7.5.

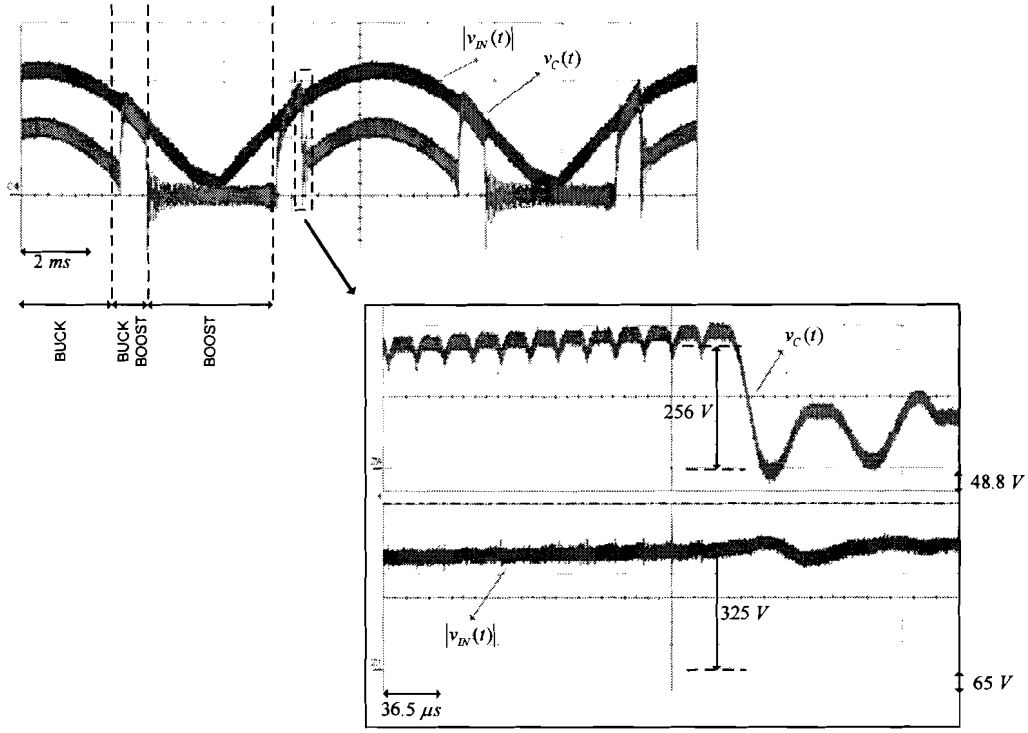


Figure 7.5, Capacitor voltage ($V_{OUT} = 268\ V$).

As can be observed in Fig 7.5 the average voltage across the capacitor is zero during the boost mode. During the buck boost mode however, the voltage starts increasing. The steady state of the voltage across the capacitor can be calculated by (1.82). Substituting the instantaneous in –and output voltage into (1.82) gives a capacitor voltage of $236\ V$. However there is small difference, equation (1.82) gives a good indication of the (steady state) capacitor voltage.

7.4 HIGH FREQUENCY CYCLES

In this section the high frequency cycles of the different modes will be discussed. After that the switching characteristics of both the boost as the buck switch will be explained.

In Fig 7.6 some high frequency cycles of the input current during the buck boost mode are shown.

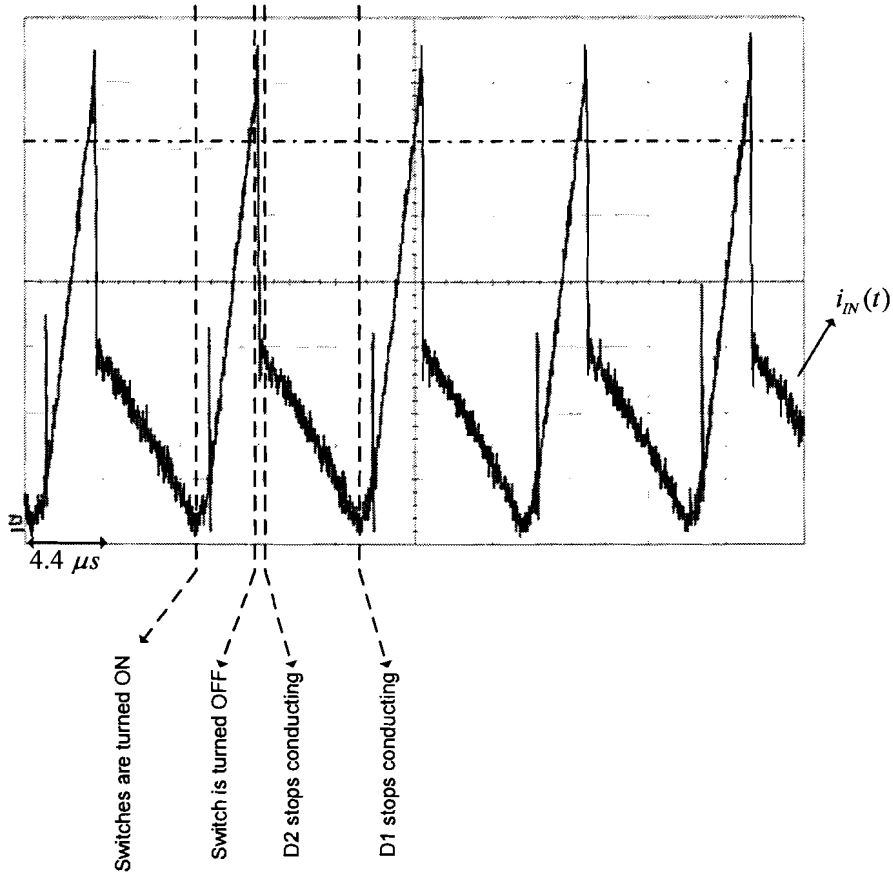


Figure 7.6, High frequency cycles during the buck boost mode.

Fig 7.6 is similar to the expected waveform shown in Fig 3.22.

The high frequency cycles for the boost and buck mode are shown in Fig 7.7 and 7.8. In this case some switch-on delay is applied making a resonance between the inductor and the parasitic drain source capacitance possible. The characteristic for the boost switch is shown in Fig 7.7

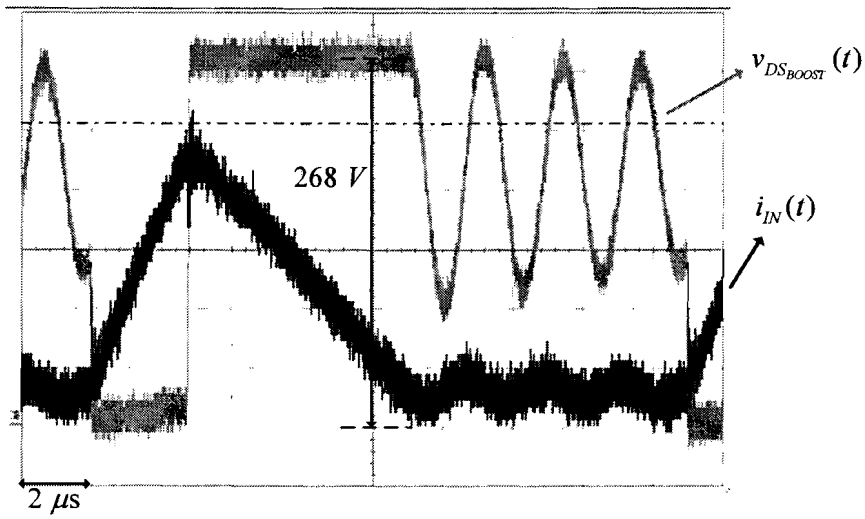


Figure 7.7, Switching characteristic for the boost switch in boost mode.

Fig 7.7 shows that the switch characteristic of the boost switch in the LsBB PFC is similar with the switch characteristic of the boost PFC. This means that ZVS is possible when the instantaneous input voltage is low ($v_{IN}(t) < V_{OUT}/2$).

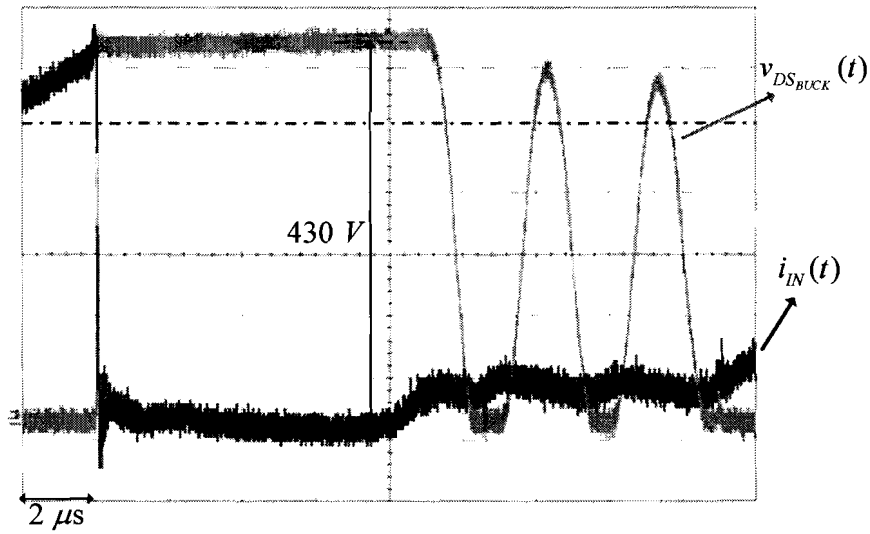


Figure 7.8, Switching characteristic for the buck switch in buck mode.

Fig 7.8 shows that ZVS for the buck switch is possible. Contrary to the boost switch there are no restrictions (except some switching delay) for ZVS.

These switching effects are discussed theoretically in section 3.3.2.4.

8 CONCLUSIONS AND DISCUSSIONS

In this report a efficiency comparison between a SEPIC PFC and a Low stress Buck Boost (LsBB) PFC is done. The first conclusion is that applying an IGBT as switch in low power applications is not recommend. The currents through the switches are too low and the switching frequency to high.

From the simulation results can be concluded that the efficiency of the LsBB PFC is better than the SEPIC PFC. The efficiency of the SEPIC PFC is around the 94.5 % while the LsBB PFC's efficiency is above 97 % . Although the difference is not very large, most of the SEPIC's PFC loss is dissipated in switch. This makes placing more switches in parallel and/or heat sinking necessary. On the other hand, since the efficiency of the SEPIC PFC is dominated by the MOSFET, the efficiency can be improved by applying a better switch only. Although the SEPIC PFC in the future can be improved by applying better switches it will not be better than the LsBB PFC. The stresses in the LsBB PFC are much lower so the losses will always be lower.

After the efficiency comparison an prototype of a LsBB PFC is build and its low stress behavior is validated. From the measurements it can be concluded that an efficiency of 96.5 % is approachable. A disadvantage of the LsBB PFC is that it contains many components and also requires a complex control circuit. However, the main disadvantage of the LsBB PFC is the transient which occurs during the transition from the buck boost to the buck mode. This transient distorts the input current and makes the THD worse. There is also a large difference in the switching frequencies during the different modes. During the boost and buck boost mode the frequency is (very) high. In the buck mode however, the switching frequency is low. This requires a large (and expensive) input filter.

Although a Singe inductor Buck Boost PFC's efficiency will be lower than the efficiency of the LsBB PFC the SiBB has many advantages in comparison to the LsBB. The LsBB PFC only needs one inductor and no series capacitor. There are no transients during changing modes, which improves the THD and makes low line current sensing possible. Also the difference between the switching frequencies of the different modes, is smaller.

In terms of efficiency it can be concluded that the LsBB is the best choice. The difference with the SiBB, however, is small. The SiBB however has some advantages which the LsBB has not, this makes the overall performance of the SiBB better than the LsBB. Only in applications where the PFC has to operate in buck mode for a short time, is the LsBB PFC a better choice.

Despite the simplicity of the SEPIC PFC, the current semiconductor switches are not good enough to make the SEPIC PFC competitive with the SiBB or LsBB PFC's. However, future improvements of the semiconductors will increase the efficiency of this topology and will make the efficiency acceptable.

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APPENDIX A LIST OF USED CONSTANTS

$C_{IN}\ [F]$	value of input capacitor after the bridge rectifier
$C_{INT}\ [F]$	value of the capacitor in the voltage regulator
$C_{INTEGRATOR}\ [F]$	value of the capacitor in the high side current sensing circuit
$C_{OUT}\ [F]$	value of the output buffer capacitor
$C_{PAR}\ [F]$	value of the output buffer capacitor
$E_{BOOST}\ [J]$	total amount of energy transferred in the boost mode
$E_{BUCK}\ [J]$	total amount of energy transferred in the buck mode
$E_{BUCKBOOST}\ [J]$	total amount of energy transferred in the buck-boost mode
$f_{SEPIC}\ [Hz]$	switching frequency of the SEPIC PFC
$f_{BUCK}\ [Hz]$	switching frequency in the buck mode
$f_{BOOST}\ [Hz]$	switching frequency in the boost mode
$f_{BUCKBOOST}\ [Hz]$	switching frequency in the buck-boost mode
$L\ [H]$	inductance of the inductor in the SiBB PFC
$L_A\ [H]$	inductance of the buck inductor LsBB PFC
$L_B\ [H]$	inductance of the boost inductor LsBB PFC
$L_E\ [H]$	parallel or series inductance of L_A and L_B
$T\ [t]$	period of one high frequency switching cycle
$T_{ON}\ [t]$	time that the switch is turned on
$T_{OFF}\ [t]$	time that the switch is turned off
$i_{IN}(t)\ [V]$	input current
$i_{IN_{AVG}}(t)\ [V]$	average (filtered) input current
$i_{L_A}(t)\ [V]$	current through L_A
$i_{L_B}(t)\ [V]$	current through L_B
$R_{INTEGRATOR}\ [\Omega]$	value of the resistor in the high side current sensing circuit
$R_{LOAD}\ [\Omega]$	load resistance
$v_{IN}(t)\ [V]$	input voltage
$\lvert v_{IN}(t)\rvert\ [V]$	rectified input voltage
$V_{IN}\ [V]$	effective input voltage
$V_C\ [V]$	steady state capacitor voltage
$\hat{V}_{IN}\ [V]$	peak input voltage
$V_{OUT}\ [V]$	output voltage

APPENDIX B DERIVATION OF DIFFERENT FUNCTIONS

B.1

$$\left(\Delta i_{L_B}(t) - i_{SHIFT}(t)\right)T_{ON} = \left(\Delta i_{L_A}(t) + i_{SHIFT}(t)\right)T_{OFF} \Rightarrow i_{SHIFT}(t) = \frac{\Delta i_{L_B}(t)T_{ON}}{T_{ON}+T_{OFF}} - \frac{\Delta i_{L_A}(t)T_{OFF}}{T_{ON}+T_{OFF}} \quad (1.160)$$

$$i_{SHIFT}(t) = \frac{\Delta i_{L_B}(t)T_{ON}}{T_{ON}+\frac{T_{ON}v_{IN}(t)}{V_{OUT}}} - \frac{\Delta i_{L_A}(t)\frac{T_{ON}v_{IN}(t)}{V_{OUT}}}{T_{ON}+\frac{T_{ON}v_{IN}(t)}{V_{OUT}}} = \frac{v_{IN}(t)T_{ON}}{2}\left(\frac{V_{OUT}}{\left(V_{OUT}+v_{IN}(t)\right)L_B} - \frac{v_{IN}(t)}{\left(V_{OUT}+v_{IN}(t)\right)L_A}\right) \quad (1.161)$$

B.2

$$i_{IN}(t) = \frac{v_{IN}(t)T_{ON}}{2L_A} + \frac{v_{IN}(t)T_{ON}}{2}\left(\frac{V_{OUT}}{\left(V_{OUT}+v_{IN}(t)\right)L_B} - \frac{v_{IN}(t)}{\left(V_{OUT}+v_{IN}(t)\right)L_A}\right) = \frac{V_{OUT}v_{IN}(t)T_{ON}}{2\left(V_{OUT}+v_{IN}(t)\right)L_E} \quad (1.162)$$

$$i_{IN}(t) = \frac{V_{OUT}v_{IN}(t)T_{ON}}{2\left(V_{OUT}+v_{IN}(t)\right)L_E} = \hat{I}_{PEAK}\frac{\left|\sin(\varpi t)\right|}{2\left(1+\frac{\hat{V}_{IN}\left|\sin(\varpi t)\right|}{V_{OUT}}\right)} \quad (1.163)$$

B.3

$$\mu(\hat{V}_{IN}, V_{OUT}) = \int_0^{\pi/2\varpi} \frac{\varpi \sin^2(\varpi t)}{\left(1+\frac{\hat{V}_{IN}\left|\sin(\varpi t)\right|}{V_{OUT}}\right)}dt = \frac{2}{\pi}\frac{\pi}{2}\int_0^{\pi/2} \frac{\sin^2(u)}{\left(1+\frac{\hat{V}_{IN}\left|\sin(u)\right|}{V_{OUT}}\right)}du \quad (1.164)$$

$$\mu(\hat{V}_{IN}, V_{OUT}) = \frac{1}{2\left(\frac{\hat{V}_{IN}}{V_{OUT}}\right)^2}\left(2\left(\frac{\hat{V}_{IN}}{V_{OUT}}\right) - \pi + \frac{4\sin^{-1}\left(-\frac{\hat{V}_{IN}}{V_{OUT}}\right) + 2\cos^{-1}\left(-\frac{\hat{V}_{IN}}{V_{OUT}}\right)}{\sqrt{1-\left(\frac{\hat{V}_{IN}}{V_{OUT}}\right)^2}}\right) \quad (1.165)$$

B.4

$$\lambda = \int_{\varpi t_{BOOST}}^{\varpi t_{BUCKBOOST}} \frac{\sin^2(u)}{V_{OUT} + \hat{V}_{IN}\sin(u)} du \tag{1.166}$$

$$\lambda = \left[\frac{uV_{OUT} + \hat{V}_{IN}\cos(u) - 2\arctan\left(\frac{\hat{V}_{IN} + V_{OUT}\tan\left(\frac{u}{2}\right)}{\sqrt{V_{OUT}^2 - \hat{V}_{IN}^2}} \right) V_{OUT}^2}{\hat{V}_{IN}^2} \right]_{\varpi t_{BOOST}}^{\varpi t_{BUCKBOOST}} \tag{1.167}$$

$$\lambda = \frac{\varpi V_{OUT}\left(t_{BOOST} - t_{BUCKBOOST}\right) + \hat{V}_{IN}\left(\cos(\varpi t_{BOOST}) - \cos(\varpi t_{BUCKBOOST})\right) + \frac{2V_{OUT}^2}{\sqrt{V_{OUT}^2 - \hat{V}_{IN}^2}}\left(\arctan\left(\frac{\hat{V}_{IN} + V_{OUT}\tan\left(\frac{\varpi t_{BUCKBOOST}}{2}\right)}{\sqrt{V_{OUT}^2 - \hat{V}_{IN}^2}} \right) - \arctan\left(\frac{\hat{V}_{IN} + V_{OUT}\tan\left(\frac{\varpi t_{BOOST}}{2}\right)}{\sqrt{V_{OUT}^2 - \hat{V}_{IN}^2}} \right) \right.}{\hat{V}_{IN}^2} \tag{1.168}$$

B.5

$$\Gamma_i = \int_{t_{i-1}}^{t_i} e^{A_i(t_i-\tau)} B_i d\tau = \int_{t_{i-1}}^{t_i} e^{-\tau A_i} e^{A_i t_i} B_i d\tau = \left(\int_{t_{i-1}}^{t_i} e^{-\tau A_i} d\tau \right) e^{A_i t_i} B_i \tag{1.169}$$

$$\Gamma_i = \left[-e^{-\tau A_i} A_i^{-1} \right]_{t_{i-1}}^{t_i} e^{t_i} B_i = \left(-e^{-t_i A_i} A_i^{-1} + e^{-t_{i-1} A_i} A_i^{-1} \right) e^{A_i t_i} B_i \tag{1.170}$$

$$\Gamma_i = \left(-A_i^{-1} + A_i^{-1} e^{A_i t_i - A_i t_{i-1}} \right) B_i = \left(e^{A_i(t_i - t_{i-1})} - I \right) A_i^{-1} B_i = \left(e^{A_i(t_i - t_{i-1})} - I \right) A_i^{-1} B_i \tag{1.171}$$

APPENDIX C STATE SPACE MATRICES

C.1

SEPIC state space matrices with closed switch (A_1) and opened switch (A_2).

$$\begin{pmatrix} \dot{i}_{L_A} \\ \dot{i}_{L_B} \\ \dot{v}_C \\ \dot{v}_{C_{OUT}} \\ 1 \end{pmatrix} = \overbrace{\begin{pmatrix} 0 & 0 & 0 & 0 & v_{IN}/L_A \\ 0 & 0 & 1/L_B & 0 & 0 \\ 0 & -1/C & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/(C_{OUT}R) & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}}^{A_1} \begin{pmatrix} i_{L_A} \\ i_{L_B} \\ v_C \\ v_{C_{OUT}} \\ 1 \end{pmatrix} \tag{1.172}$$

$$\begin{pmatrix} \dot{i}_{L_A} \\ \dot{i}_{L_B} \\ \dot{v}_C \\ \dot{v}_{C_{OUT}} \\ 1 \end{pmatrix} = \overbrace{\begin{pmatrix} 0 & 0 & -1/L_A & -1/L_A & v_{IN}/L_A \\ 0 & 0 & 0 & -1/L_B & 0 \\ 1/C & 0 & 0 & 0 & 0 \\ 1/C_{OUT} & 1/C_{OUT} & 0 & -1/(C_{OUT}R) & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}}^{A_2} \begin{pmatrix} i_{L_A} \\ i_{L_B} \\ v_C \\ v_{C_{OUT}} \\ 1 \end{pmatrix} \tag{1.173}$$

C.2

State space matrices for the Low stress Buck Boost in boost mode with closed switch (A_1) and opened switch (A_2).

$$\begin{pmatrix} \dot{i}_{L_A} \\ \dot{i}_{L_B} \\ \dot{v}_C \\ \dot{v}_{C_{OUT}} \\ 1 \end{pmatrix} = \overbrace{\begin{pmatrix} 0 & 0 & 1/L_A & 0 & v_{IN}/L_A \\ 0 & 0 & 0 & 0 & v_{IN}/L_B \\ -1/C & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/(C_{OUT}R_{LOAD}) & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}}^{A_1} \begin{pmatrix} i_{L_A} \\ i_{L_B} \\ v_C \\ v_{C_{OUT}} \\ 1 \end{pmatrix} \tag{1.174}$$

$$\begin{pmatrix} \dot{i}_{L_A} \\ \dot{i}_{L_B} \\ \dot{v}_C \\ \dot{v}_{C_{OUT}} \\ 1 \end{pmatrix} = \overbrace{\begin{pmatrix} 0 & 0 & 0 & -1/L_A & v_{IN}/L_A \\ 0 & 0 & -1/L_B & -1/L_B & v_{IN}/L_B \\ 0 & 1/C & 0 & 0 & 0 \\ 1/C_{OUT} & 1/C_{OUT} & 0 & -1/(C_{OUT}R_{LOAD}) & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}}^{A_2} \begin{pmatrix} i_{L_A} \\ i_{L_B} \\ v_C \\ v_{C_{OUT}} \\ 1 \end{pmatrix} \tag{1.175}$$

C.3

State space matrices for the Low stress Buck Boost in buck mode boost mode with closed switch (A_1), two conducting diodes (A_2) and one conducting diode (A_3).

$$\begin{pmatrix} \dot{i}_{L_A} \\ \dot{i}_{L_B} \\ \dot{v}_C \\ \dot{v}_{C_{OUT}} \\ 1 \end{pmatrix} = \overbrace{\begin{pmatrix} 0 & 0 & 1/L_A & 0 & v_{IN}/L_A \\ 0 & 0 & 0 & 0 & v_{IN}/L_B \\ -1/C & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1/(C_{OUT}R_{LOAD}) & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}}^{A_1} \begin{pmatrix} i_{L_A} \\ i_{L_B} \\ v_C \\ v_{C_{OUT}} \\ 1 \end{pmatrix} \quad (1.176)$$

$$\begin{pmatrix} \dot{i}_{L_A} \\ \dot{i}_{L_B} \\ \dot{v}_C \\ \dot{v}_{C_{OUT}} \\ 1 \end{pmatrix} = \overbrace{\begin{pmatrix} 0 & 0 & 0 & -1/L_A & 0 \\ 0 & 0 & -1/L_B & -1/L_B & v_{IN}/L_B \\ 0 & 1/C & 0 & 0 & 0 \\ 1/C_{OUT} & 1/C_{OUT} & 0 & -1/(C_{OUT}R_{LOAD}) & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}}^{A_2} \begin{pmatrix} i_{L_A} \\ i_{L_B} \\ v_C \\ v_{C_{OUT}} \\ 1 \end{pmatrix} \quad (1.177)$$

$$\begin{pmatrix} \dot{i}_{L_A} \\ \dot{i}_{L_B} \\ \dot{v}_C \\ \dot{v}_{C_{OUT}} \\ 1 \end{pmatrix} = \overbrace{\begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1/L_B & -1/L_B & v_{IN}/L_B \\ 0 & 1/C & 0 & 0 & 0 \\ 0 & 1/C_{OUT} & 0 & -1/(C_{OUT}R_{LOAD}) & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}}^{A_3} \begin{pmatrix} i_{L_A} \\ i_{L_B} \\ v_C \\ v_{C_{OUT}} \\ 1 \end{pmatrix} \quad (1.178)$$

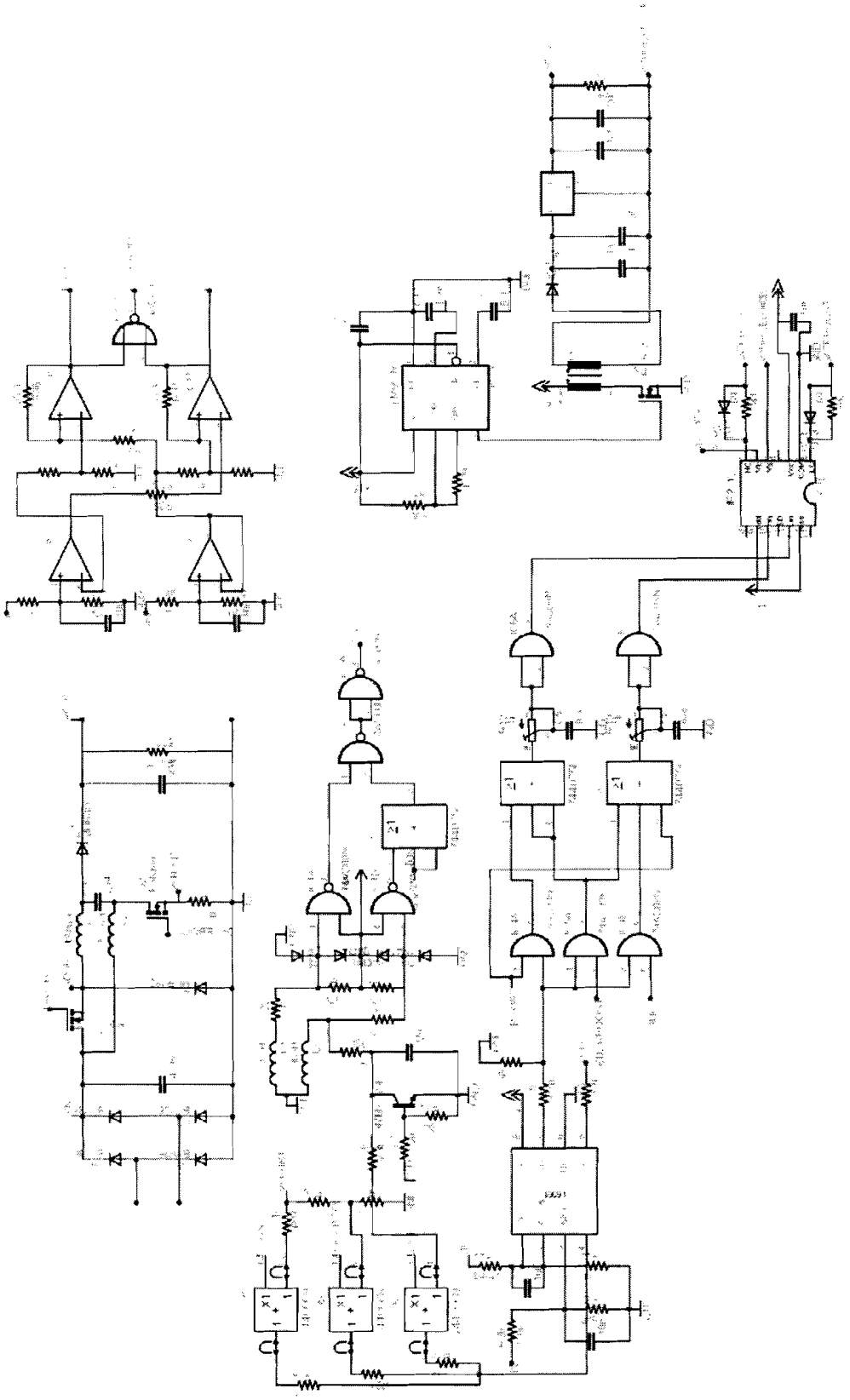
C.4

State space matrices for the Low stress Buck Boost in buck mode with closed switch (A_1) and opened switch (A_2).

$$\begin{pmatrix} \dot{i}_{L_A} \\ \dot{i}_{L_B} \\ \dot{v}_C \\ \dot{v}_{C_{OUT}} \\ 1 \end{pmatrix} = \overbrace{\begin{pmatrix} 0 & 0 & 0 & -1/L_A & v_{IN}/L_A \\ 0 & 0 & -1/L_B & -1/L_B & v_{IN}/L_B \\ 0 & 1/C & 0 & 0 & 0 \\ 1/C_{OUT} & 1/C_{OUT} & 0 & -1/(C_{OUT}R_{LOAD}) & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}}^{A_1} \begin{pmatrix} i_{L_A} \\ i_{L_B} \\ v_C \\ v_{C_{OUT}} \\ 1 \end{pmatrix} \quad (1.179)$$

$$\begin{pmatrix} \dot{i}_{L_A} \\ \dot{i}_{L_B} \\ \dot{v}_C \\ \dot{v}_{C_{OUT}} \\ 1 \end{pmatrix} = \overbrace{\begin{pmatrix} 0 & 0 & 0 & -1/L_A & 0 \\ 0 & 0 & -1/L_B & -1/L_B & v_{IN}/L_B \\ 0 & 1/C & 0 & 0 & 0 \\ 1/C_{OUT} & 1/C_{OUT} & 0 & -1/(C_{OUT}R_{LOAD}) & 0 \\ 0 & 0 & 0 & 0 & 1 \end{pmatrix}}^{A_2} \begin{pmatrix} i_{L_A} \\ i_{L_B} \\ v_C \\ v_{C_{OUT}} \\ 1 \end{pmatrix} \quad (1.180)$$

APPENDIX D SCHEMATIC



Note that all integrated circuits are bypassed by small capacitors