Design of a bipolar variable gain amplifier with a high gain range and low distortion

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Design of a bipolar Variable Gain Amplifier with a high gain range and low distortion

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Abstract

In this report the design of a variable gain amplifier for use in an automatic gain control (AGC) circuit is described. The AGC will be used in radio and television receivers. Because a very large gain range is needed, together with a high linearity, the existing Gilbert cell was found to be unable to meet the specifications. A completely new principle was applied to achieve a high gain range together with low distortion.

By putting a number of differential pairs in parallel and supplying offset voltages to them, different transfer characteristics can be composed. When no offsets are applied, all differential pairs operate in the same region. In this case, the gain is very high but the linearity is the same as for a single differential pair. When the offset is increased, the regions of operation of the various differential pairs are juxtaposed. The gain decreases but the linearity increases.

The realized variable gain amplifier consists of three stages, each with 32 parallel differential pairs and a combined input buffer and reference ladder for the offset voltages. Each stage has a gain range of $25dB$, so the complete three-stage amplifier has a gain range of $75dB$. The amplifier can operate on signals with a frequency up to $60MHz$. Total power consumption is about $40mW$ per stage with a $5V$ supply.

The circuit has been realized in the Philips QUBiC1 process. The active chip area for the three-stage amplifier measures about $0.4mm^2$. This report is based on simulation results. When this report was written, no chips were available yet, so no measurements have been performed. Besides the three-stage amplifier, a one-stage and two-stage as well as a three-stage version with separate supplies have been designed for test purposes.

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Chapter 1

Introduction

From the introduction of wireless communication up to the present, there has been a continuous improvement in receiver technology. Most of the receivers that are used nowadays are however still mainly analog. Usually the incoming antenna signal (RF signal) is first roughly filtered to limit the spectrum and mixed to some intermediate frequency (IF) before the desired frequency is selected, amplified and demodulated.
At Philips, a new receiver architecture is being studied in which the filtering and demodulation of the IF signal are performed digitally. However, before an antenna signal can be fed to an A/D-converter, some analog preprocessing has to be performed. In figure 1.1 the new receiver architecture is shown.

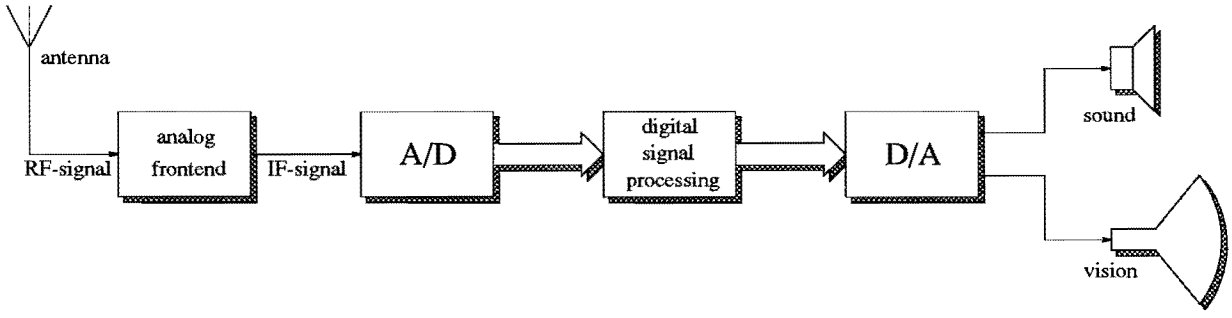

Figure 1.1: *Basic architecture of a digital receiver*

Advantages of this architecture are:

- The filtering functions of the analog frontend can remain much simpler.
- A large part of the receiver can be integrated on one chip. This will reduce the number of devices and the printed circuit board size of receiver equipment, and thus the cost, the size and the power consumption.

- The quality of the receiver will increase because digital circuits are less sensitive to mismatch, offset, temperature variation and so forth.
- It is easier to implement special features, such as Picture in Picture (PIP), Teletext and multi-channel reception on digital hardware.
- A receiver can be designed to adapt automatically to the various standards throughout the world.

The analog frontend has to perform several functions to prepare the signal for conversion by the A/D-converter. These functions are:

- **Filtering.** From the incoming spectrum, only the frequency band of interest has to be passed. This limits the incoming power to prevent overload and makes sure no aliasing will occur in the digital part of the system.
- **Mixing.** To reduce signal frequency, it is convenient to mix the high-frequency RF-signal to an intermediate frequency (IF) of about 30 to $60MHz$, depending on the used standard.
- **Amplification.** Because of the insertion loss of the filter section, some amplification has to be performed to restore the original signal levels. This is necessary because of noise considerations.
- **Dynamics compression.** Antenna signal levels can vary a lot due to external factors like mobility of the receiver, weather influences and interference of different transmitters. An Automatic Gain Control (AGC) circuit has to take care of supplying the A/D-converter with a signal of constant amplitude, typically close to the full scale level of the A/D-converter.

In figure 1.2 the frontend has been expanded to show its different components in more detail.

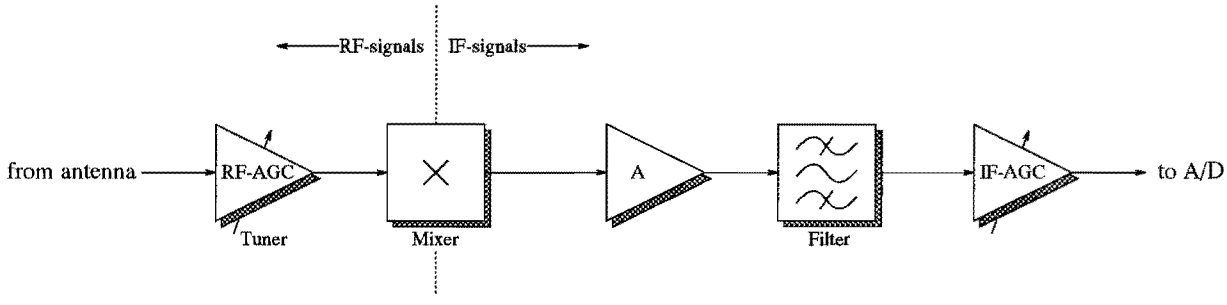

Figure 1.2: *The analog frontend of the digital receiver*

In this report, the design, implementation and realization of the IF-AGC will be described. For this block, some initial demands will be formulated now.

The used A/D-converter will have a resolution of 10 bits and a differential input with a full scale value of $1.5V_{p-p}$. This implies that the IF-AGC has to be able to produce a differential output signal of $1.5V_{p-p}$ with harmonic distortion better than $-62dB$. Furthermore, the output of the filter is also differential, which means that the IF-AGC must have a differential input. The amplitude range of the filtered signal is about $70dB$. The gain range of the IF-AGC has to be at least $70dB$ to be able to cope with all signal levels. The whole system, including the IF-AGC, has to operate from a single $5V$ supply. The IF-AGC has to be realized in the bipolar QUBiC1 process. All these demands are put together in table 1.1.

Table 1.1: *Initial demands on the IF-AGC*

Property	Value
Input	differential
Output	differential
Harmonic distortion	$\leq -62dB$ (10 bits)
Input signal bandwidth	$\geq 60MHz$
Supply voltage	$5V \pm 10\%$
Gain range	$\geq 70dB$
Output signal level	$1.5V_{p-p}$
Technology	bipolar (QUBiC1)

In chapter 2 an overview of the system will be given and some more detailed specifications will be derived. In chapter 3 the theory of operation of the IF-AGC will be described. Chapter 4 deals with the implementation of the circuits in QUBiC1. Some layout aspects will be presented in chapter 5. Finally, in chapter 6 conclusions about the project will be stated. At the time this report was written, no test chips were available. All the results in this report are therefore simulation results.

Chapter 2

System overview and AGC specifications

In this chapter, the specifications of the analog frontend will be summarized. After this, the demands on the IF-AGC will be derived from its context. These demands will impose limits on noise and distortion level. Also, gain and gain range requirements will be laid down.

2.1 The complete analog frontend

2.1.1 Block diagram

In figure 2.1 the block diagram of the complete analog frontend is depicted. As can be seen in this picture, the input of the receiver is an RF signal from an antenna (or a local cable system) in the frequency range of about $50MHz$ to about $850MHz$. First, the function of each of the blocks will be explained.

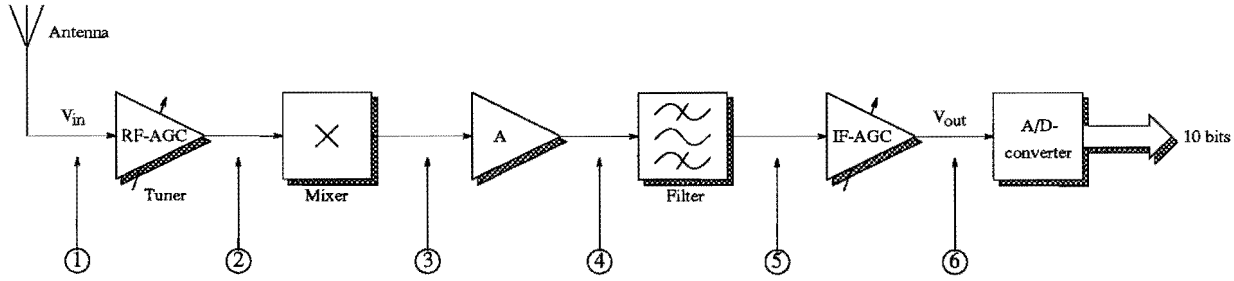

Figure 2.1: *The complete analog frontend from antenna to A/D-converter*

The first block, the tuner, takes care of roughly selecting a band from the incoming spectrum. For large signals, the tuner also functions as an AGC. This only occurs when the IF-AGC is already at its minimum gain. Otherwise, the tuner AGC is adjusted to maximum gain to improve signal to noise ratio (SNR).

The second block, the mixer, mixes the RF signal to an intermediate frequency (IF) of about $30MHz$ to $60MHz$, depending on the used transmission standard.
The third block, an amplifier, compensates for the insertion loss of the next block, the filter. Its gain is about $20dB$.
The fourth block, a bandpass filter, limits the spectrum of the IF signal to reduce the risk of overloading the rest of the system and also to reduce out of band noise.
The fifth block, the IF-AGC, compresses the amplitude range of the incoming IF signal. For very small signals, it is adjusted to maximum gain. When the signal amplitude increases, it stays at maximum gain until the amplitude of the outgoing signal reaches a value of $1.5V_{p-p}$, which is the full scale input value of the A/D-converter. It then decreases its gain such that the outgoing signal stays at an amplitude of $1.5V_{p-p}$. When the IF-AGC is at minimum gain, the RF-AGC in the tuner takes over. Both AGC circuits are controlled by feedback loops (not drawn in figure 2.1).
The next block is a 10-bits analog-to-digital converter. After the IF signal is converted to a digital signal, it is processed to become a digital baseband signal containing audio and video. This signal is then converted to an analog signal again by a digital-to-analog converter.

2.1.2 Signal levels

For each of the interconnect nodes (numbered 1 to 6) in the frontend, the range of amplitudes is shown in figure 2.2. As can be seen, the amplitude range is compressed from over $100dB$ at the input node of the frontend to ideally $0dB$ at the output. For this compression, the two AGC's are responsible.

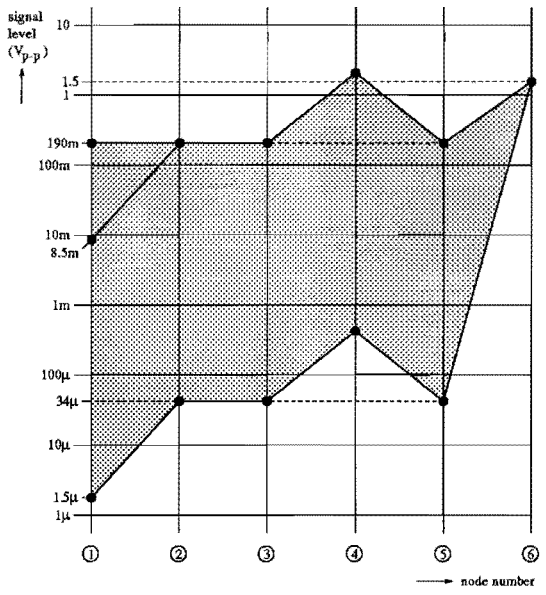

Figure 2.2: *Amplitude levels for all nodes in the frontend*

2.1.3 Signal frequencies

For signal frequencies, the same graph as in figure 2.2 for signal amplitudes, can be constructed. This is shown in figure 2.3. The solid line represents the channel which has been tuned to. The gray area represents the bandwidth of the signal. As can be seen, the bandwidth of the incoming signal is also compressed before it reaches the A/D-converter. The digital part of the receiver takes care of reducing the bandwidth to exactly one channel, separating sound from vision and demodulating these signals to baseband.

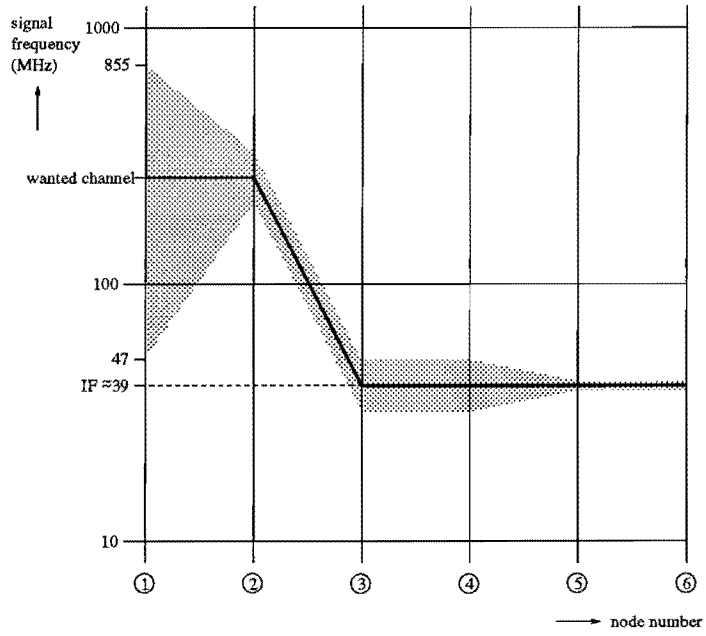

Figure 2.3: *Signal frequencies for all nodes in the frontend*

2.1.4 Transfer functions

The signals in the receiver consist of three basic components: wanted signal, noise and harmonics. The wanted signal at the output of the frontend should remain at a constant level equal to the full scale value of the A/D-converter, which is $1.5V_{p-p}$. Harmonic distortion and noise signals should be small compared to the wanted signal, ideally less than the quantization noise of the 10-bits A/D-converter. For the signal to quantization noise ratio in decibels of an n-bits converter, the following equation holds:

$$S/N = n \times 6.02 + 1.76dB. \tag{2.1}$$

For a 10-bits A/D-converter, this yields $S/N \approx 62dB$. Distortion and noise signals of the frontend thus should be at least $62dB$ down compared to the wanted signal to remain outside the dynamic range of the A/D-converter. However, in extreme situations, such as very high or very low input signal levels, higher distortion and noise levels are tolerable.

The input level at which the signal to noise ratio is $26dB$, is called the selectivity and is typically $10 \ldots 30\mu V_{p-p}$. In figure 2.4 the transfer curves for the complete frontend are shown. As can be seen, the output level of the wanted signal becomes constant when the input level exceeds the sensitivity level. The SNR will increase to about $62dB$. The distortion level will have its optimum for medium gain. Distortion will increase for high gains (left hand side in the graph) and for high input levels (right hand side).

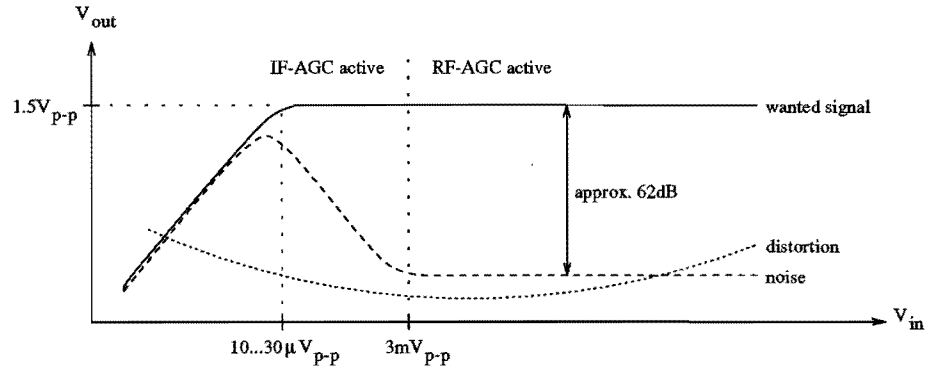

Figure 2.4: *Frontend transfer curves for wanted signal, distortion and noise*

2.2 The IF-AGC

2.2.1 Block diagram

The IF-AGC itself consists of four main blocks, three of which have a variable gain factor. In figure 2.5 the block diagram is shown, with node numbering. The three variable gain amplifiers (stage 1 to stage 3) have a gain range of about $25dB$ each. Their gain can be varied between $0dB$ and approximately $25dB$. The last block, a fixed amplifier A, has a gain of about $18dB$. The complete IF-AGC thus has a gain which is variable between $18 + (3 \times 0) = 18dB$ and $18 + (3 \times 25) = 93dB$, which yields a gain range of $75dB$. Blocks stage 1, stage 2 and stage 3 are identical with respect to circuit implementation. The IF-AGC has both a differential input and a differential output.

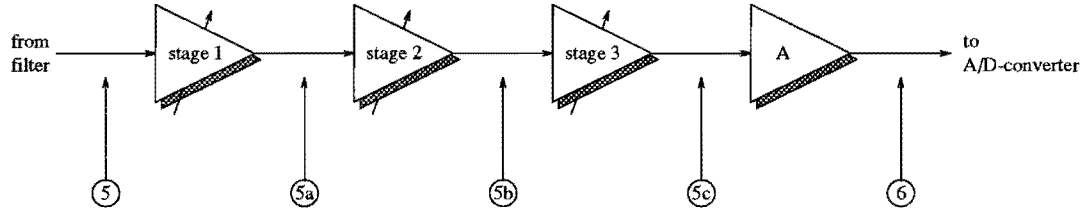

Figure 2.5: *Block diagram of the IF-AGC*

2.2.2 Signal levels

From figure 2.2 we can determine the signal levels on the input and output nodes of the IF-AGC (node 5 and 6). In figure 2.6 the amplitude levels of the internal nodes (5a, 5b and 5c) are also depicted. Because stage 1, stage 2 and stage 3 are identical, gain and gain range is distributed equally among these stages. In the situation where the gain is minimal, all three variable stages will get the same input level. Because of this, these stages will have to meet the same worst case demands.

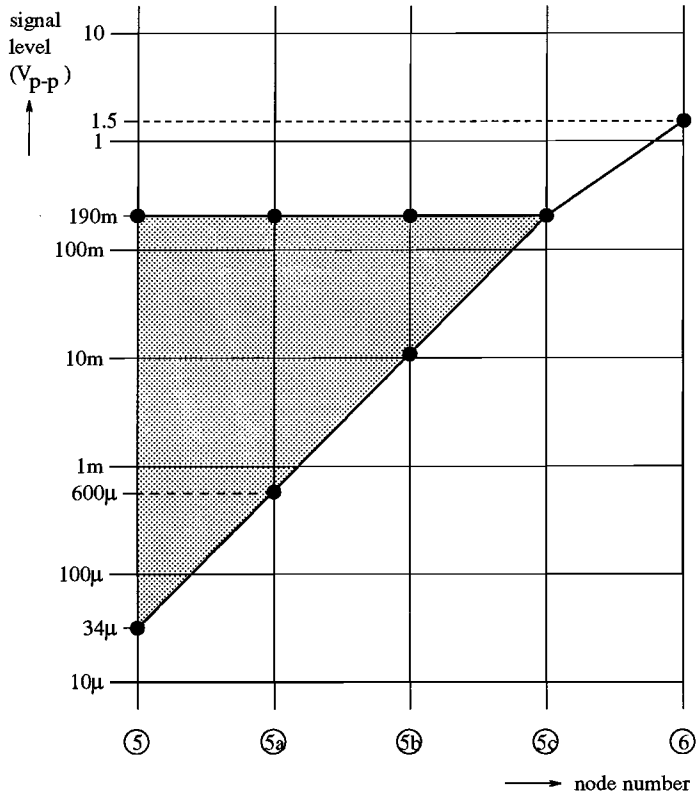

Figure 2.6: *Signal levels inside the IF-AGC*

2.2.3 Distortion

With equation (2.1) the limit for the harmonic distortion of the complete frontend was determined. Each block in the frontend has to perform at least as good as the complete frontend. For the IF-AGC this means that distortion has to be at least $62dB$ down compared to the wanted signal. Because the IF-AGC is differential and thus completely symmetrical, odd order harmonics are more important than even order harmonics.
To specify the maximum allowable distortion of the IF-AGC, the output IP3 will be calculated now. Refer to appendix A for details about IP3 and related subjects. For all gain factors between $18dB$ and $93dB$, the output voltage will ideally be $1.5V_{p-p}$. Everywhere in

this operating region, the third order distortion HD3 has to be $62dB$ or better. In decibels, the output voltage comes to $3.5dBV_{p-p}$ and this means the output IP3 has to be at least $3.5dBV_{p-p} + \frac{1}{2} \times 62dB = 34.5dBV_{p-p}$ for all gain factors, which means $V_{IP3_{out}} \geq 52.2V_{p-p}$. When we consider the variable gain stages stage 1 to stage 3, we have an output voltage of $190mV_{p-p}$ $(-14.4dBV_{p-p})$. The output IP3 for the variable gain part has to be at least $-14.4dBV_{p-p} + \frac{1}{2} \times 62dB = 16.6dBV_{p-p}$ $(6.8V_{p-p})$. In figure 2.7 the relation between IP3 and HD3 is made clear.

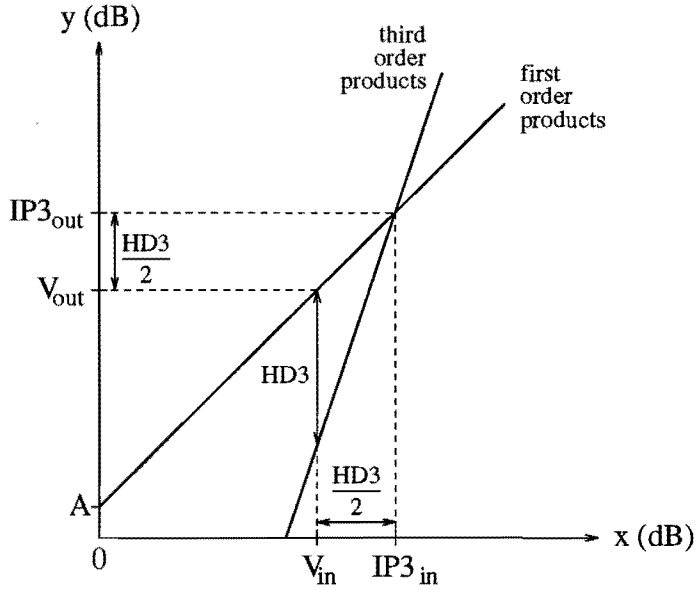

Figure 2.7: *Demands on IP3 for the IF-AGC*

2.2.4 Noise

As stated in section 2.1.4, the signal to noise ratio (SNR) at the output of the frontend should ideally be $62dB$. In extreme situations, such as very small signal levels, this will not be reachable, because the incoming antenna signal will have an SNR which is already lower. To function optimally under all conditions, the noise contribution of the IF-AGC should be as small as possible.

To express the noise contribution of a twoport, the noise figure F is commonly used. It is defined as the ratio of input SNR and output SNR, or in formula

$$F = \frac{\left(\frac{S_{in}}{N_{in}}\right)}{\left(\frac{S_{out}}{N_{out}}\right)} \text{ at } T = 300K. \tag{2.2}$$

When F is expressed in decibels, it is called the noise figure, and when not in decibels, it is called the noise factor. For an ideal noiseless circuit, F will be 1 $(0dB)$. The output SNR then is equal to the input SNR because the circuit itself contributes no noise.

The noise factor F of n cascaded networks is

$$F = F_1 + \frac{F_2 - 1}{A_1} + \frac{F_3 - 1}{A_1 A_2} + \ldots + \frac{F_n - 1}{A_1 A_2 \ldots A_{n-1}}, \tag{2.3}$$

where F_i, $i = 1 \ldots n$ and A_i, $i = 1 \ldots n-1$ are the noise factors, respectively the gains of the networks. Equation (2.3) shows that when A_1, A_2, ..., A_{n-1} are large enough, the noise factor of the total network will be almost equal to the noise factor of the first network. It also shows that, because the frontend has a variable gain, the noise factor will not be constant for all gain settings. It will increase with decreasing gain. Therefore, the situation in which the frontend is set to minimal gain, is considered worst case for noise performance.
Now assume that the first four blocks of the frontend together have a noise figure of $6dB$ ($4\times$) for an input impedance R_g of 50Ω. This situation is depicted in figure 2.8.

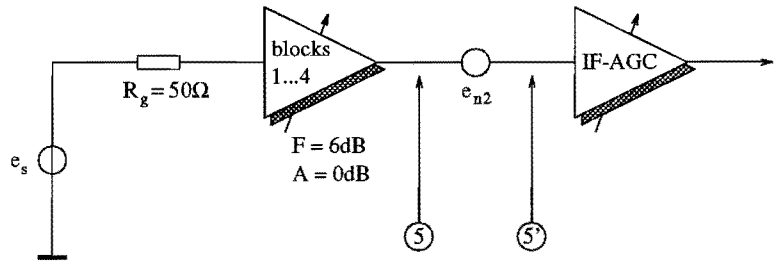

Figure 2.8: *Noise model of the frontend*

With input source e_s and a gain of $0dB$, the signal to noise ratio on node 5 will be $\frac{e_s^2}{e_{n1}^2}$, where e_{n1} is the noise generated by R_g. If the noise figure of the complete frontend, including IF-AGC, is allowed to be at most $3dB$ worse than the noise figure of the first four blocks, the IF-AGC contributes at most the same amount of noise as the rest of the frontend. The signal to noise ratio on node 5'[1]is $\frac{e_s^2}{e_{n1}^2+e_{n2}^2}$. With the above stated demands, this yields $e_{n2}^2 \leq e_{n1}^2$, where e_{n1}^2 can be calculated as follows:

$$\begin{aligned} \frac{e_{n2}^2}{\Delta f} &= 4kTR_gF \\ &= 4 \cdot 1.38 \cdot 10^{-23} \cdot 300 \cdot 50 \cdot 4 \cdot \\ &= 3.3 \cdot 10^{-18} \cdot \ [V^2/Hz]. \end{aligned}$$

From this, the maximum value of the noise voltage contribution of the IF-AGC follows easy: $e_{n2} \leq e_{n1} = 1.82\ nV/\sqrt{Hz}$. The noise current contribution is neglected, because the output impedance from which the IF-AGC is driven is assumed to be small.

[1]Node 5' is a virtual node inside the IF-AGC. It is obtained by transforming all internal noise sources of the IF-AGC to equivalent noise sources at the input and joining them to one single noise source e_{n2}.

2.2.5 Transfer function

For small signals ($\leq 34\mu V_{p-p}$), the IF-AGC will be adjusted to maximum gain ($93dB$). At an input level of $34\mu V_{p-p}$, the output signal will reach the wanted level of $1.5V_{p-p}$. This level can be maintained until the input level reaches $190mV_{p-p}$. The IF-AGC is at minimum gain then. When the input level increases to more than $190mV_{p-p}$, the output level will exceed $1.5V_{p-p}$. In figure 2.9 this is illustrated.

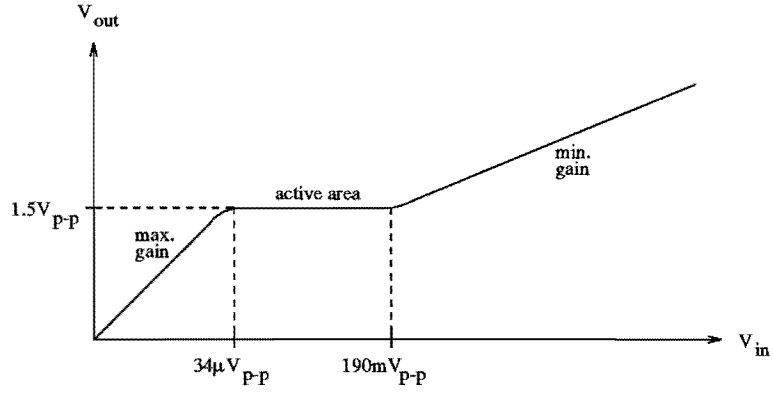

Figure 2.9: *Transfer function of the IF-AGC*

2.3 Final specifications

In table 2.1 the final specifications of the complete IF-AGC, derived in the previous sections, are stated. They will serve as a base for the next chapters.

Table 2.1: *Final demands on the IF-AGC*

Property	Value
Input	differential
Active input range	$34\mu V_{p-p} \ldots 190mV_{p-p}$
Output	differential
Typical output voltage	$1.5V_{p-p}$
Gain range	$18dB \ldots 93dB$
Input signal bandwidth	$\geq 60MHz$
Output IP3 (total IF-AGC)	$\geq 52.2V_{p-p}$
(variable part)	$\geq 6.8V_{p-p}$
Equiv. input noise voltage	$\leq 1.82\ nV/\sqrt{Hz}$
Supply voltage	$5V \pm 10\%$
Technology	bipolar (QUBiC1)

Chapter 3

Theory of operation

This chapter will deal with the theoretical backgrounds of multi-tanh structures. The multi-tanh structure is very suitable for making extremely linear transconductance amplifiers with, as will be shown, variable gain capabilities. First, some basics about bipolar transistors and differential pairs will be explained, after which the multi-tanh structure itself will be introduced.

3.1 Basic bipolar building blocks

3.1.1 Model of the bipolar NPN-transistor

In figure 3.1(a) the symbol for a bipolar NPN-transistor, together with current and voltage naming conventions, are given. For large signals, this transistor can be modeled by the Ebers-Moll model [1] of figure 3.1(b).

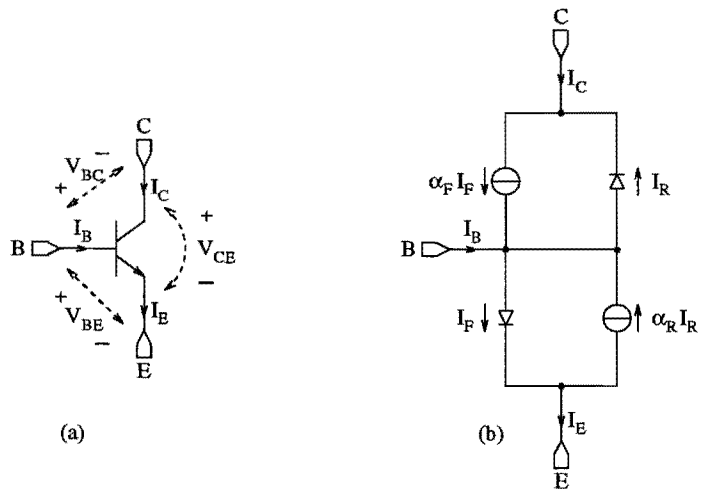

Figure 3.1: (a) *Bipolar NPN-transistor,* (b) *Ebers-Moll model*

As can be observed directly from the model in figure 3.1(b),

$$I_E = I_C + I_B, \text{ with} \tag{3.1}$$
$$I_E = I_F - \alpha_R I_R \text{ and} \tag{3.2}$$
$$I_C = \alpha_F I_F - I_R. \tag{3.3}$$

The forward and reverse currents I_F and I_R can be expressed in the clamp voltages of the transistor by

$$I_F = I_{ES}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) \text{ and} \tag{3.4}$$
$$I_R = I_{CS}\left(e^{\frac{V_{BC}}{V_T}} - 1\right), \tag{3.5}$$

where $V_T = \frac{kT}{q}$ is the so called thermal voltage, which has a value of about $26mV$ at a temperature of $300K$. Device parameters α_F and α_R are dependent on forward and reverse current gain β_F and β_R:

$$\alpha_F = \frac{\beta_F}{1+\beta_F} \text{ and} \tag{3.6}$$
$$\alpha_R = \frac{\beta_R}{1+\beta_R}, \text{ where} \tag{3.7}$$
$$\beta_F = \frac{I_C}{I_B} \text{ and} \tag{3.8}$$
$$\beta_R = \frac{-I_E}{I_B}. \tag{3.9}$$

The terminal currents can now be described by two variables (V_{BE} and V_{BC}) and four parameters (α_F, α_R, I_{ES} and I_{CS}). For the ideal transistor, the four parameters are related by the reciprocity theorem as

$$\alpha_F I_{ES} = \alpha_R I_{CS} = I_S. \tag{3.10}$$

The above calculations can be summarized by the general large-signal Ebers-Moll model for the NPN-transistor as

$$I_E = I_{ES}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - \alpha_R I_{CS}\left(e^{\frac{V_{BC}}{V_T}} - 1\right) \text{ and} \tag{3.11}$$
$$I_C = \alpha_F I_{ES}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - I_{CS}\left(e^{\frac{V_{BC}}{V_T}} - 1\right). \tag{3.12}$$

3.1.2 The bipolar differential pair

Consider the bipolar differential pair of figure 3.2. It consists of the two emitter-coupled NPN-transistors T_1 and T_2, and a current source that provides the tail current I_{tail}. The input is the differential voltage $V_{in} = V_{b1} - V_{b2}$ and the output is the differential current

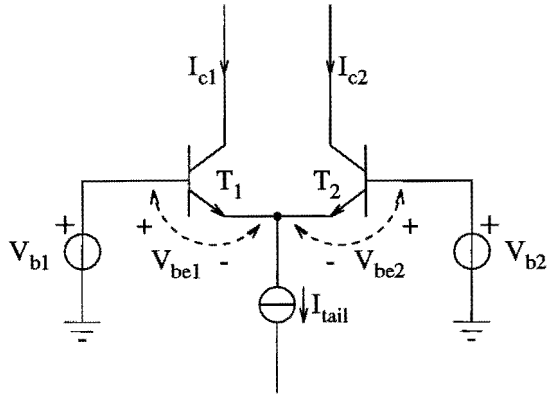

Figure 3.2: *The basic bipolar differential pair*

$I_{out} = I_{c1} - I_{c2}$. Summing the voltages around the loop consisting of the input voltage sources and the base-emitter junctions gives

$$V_{b1} - V_{be1} + V_{be2} - V_{b2} = 0. \tag{3.13}$$

From equations (3.11) and (3.12), assuming $V_{be1}, V_{be2} \gg V_T$, follows

$$V_{be1} = V_T \ln \frac{I_{c1}}{I_{S1}} \text{ and} \tag{3.14}$$

$$V_{be2} = V_T \ln \frac{I_{c2}}{I_{S2}}. \tag{3.15}$$

Assuming that transistors T_1 and T_2 are equal, the above yields

$$\frac{I_{c1}}{I_{c2}} = e^{\frac{V_{in}}{V_T}}. \tag{3.16}$$

Additionally, summing currents at the emitters gives

$$I_{e1} + I_{e2} = I_{tail} = \frac{1}{\alpha_F}(I_{c1} + I_{c2}). \tag{3.17}$$

By combining equations (3.16) and (3.17), expressions for the collector currents can be found:

$$I_{c1} = \frac{\alpha_F I_{tail}}{1 + e^{-\frac{V_{in}}{V_T}}}, \tag{3.18}$$

$$I_{c2} = \frac{\alpha_F I_{tail}}{1 + e^{\frac{V_{in}}{V_T}}}. \tag{3.19}$$

The output current is defined as the difference between the collector currents and can be written as

$$I_{out} = \alpha_F I_{tail} \tanh \frac{-V_{in}}{2V_T}. \tag{3.20}$$

This function has been plotted in figure 3.3. As can be seen, the amplifier is inverting when it is configured like in figure 3.2. To obtain non-inverted amplification, I_{c1} and I_{c2} should be exchanged.

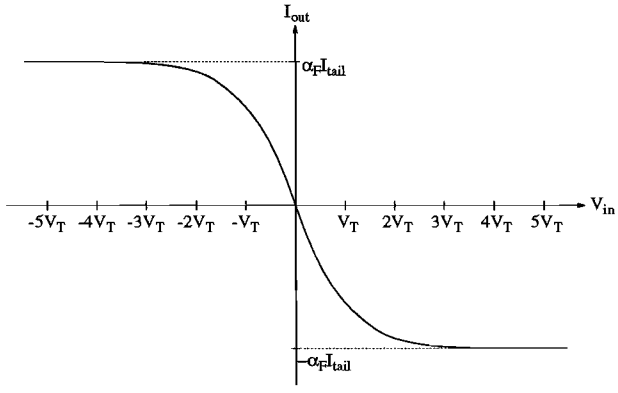

Figure 3.3: *Transfer function of the bipolar differential pair*

The transconductance G_m of the differential pair is defined and calculated as follows:

$$G_m(V_{in}) := \frac{\partial I_{out}}{\partial V_{in}} = -\frac{\alpha_F I_{tail}}{2V_T} \operatorname{sech}^2 \frac{V_{in}}{2V_T}. \tag{3.21}$$

For small signals, $V_{in} \approx 0$, the transconductance is approximately $-\frac{\alpha_F I_{tail}}{2V_T} =: g_m$. Transconductance as a function of input voltage is plotted in figure 3.4.

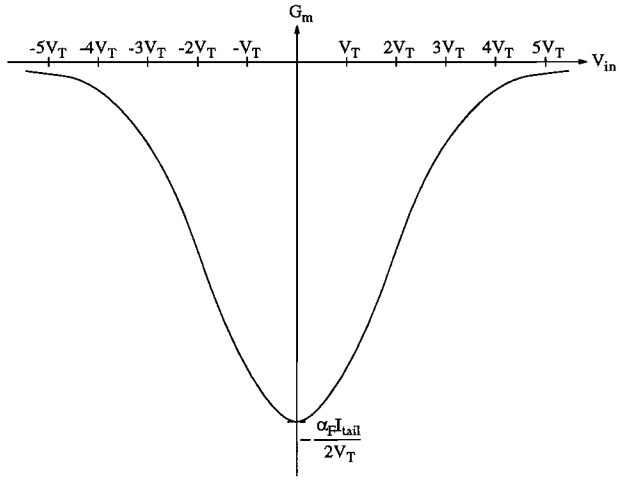

Figure 3.4: *Transconductance of the bipolar differential pair*

By applying an offset voltage ϕ to the input voltage of a differential pair, such that the effective input signal will become $V_{in} + \phi$, the transfer characteristic of figure 3.3 will shift

to the left by ϕ. The zero crossing point will move to $V_{in} = -\phi$. The characteristic can also be shifted to the right by applying a negative offset. The maximum value for the offset voltage is limited by the voltage space, determined by input voltage, supply voltage and voltage drop over the current source.

3.2 Multi-tanh structures

3.2.1 Coupling of differential pairs

The output currents of several differential pairs can be added together simply by connecting up their output terminals. The resulting circuit is called *multi-tanh structure* for obvious reasons and is depicted in figure 3.5. Note the non-inverting configuration of this amplifier.

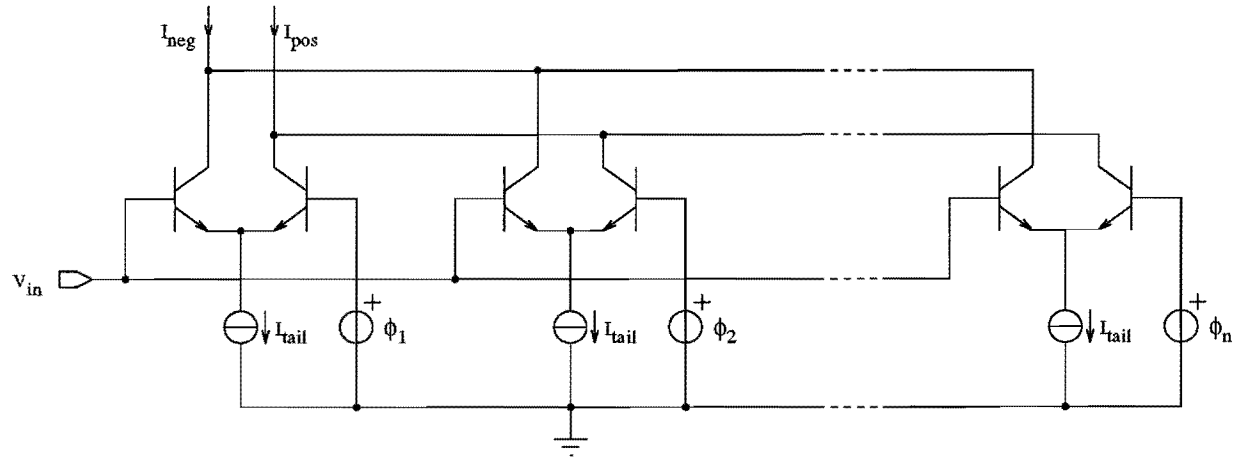

Figure 3.5: *The multitanh structure consisting of n coupled differential pairs*

The transfer function of each individual differential pair i can be shifted by varying the corresponding offset voltage ϕ_i. The overall output current $I^n_{out} = I_{pos} - I_{neg}$ is the sum of the individual output currents and thus can be written as

$$I^n_{out} = \alpha_F I_{tail} \sum_{i=1}^{n} \tanh \frac{V_{in} - \phi_i}{2V_T}. \tag{3.22}$$

Now suppose that all offsets ϕ_i are equal. The total output current then is simply n times bigger than the output current of a single differential pair. The transconductance follows by differentiating (3.22) to V_{in}:

$$G^n_m(V_{in}) = \frac{\partial I^n_{out}}{\partial V_{in}} = \frac{\alpha_F I_{tail}}{2V_T} \sum_{i=1}^{n} \operatorname{sech}^2 \frac{V_{in} - \phi_i}{2V_T}. \tag{3.23}$$

When all offsets ϕ_i are equal and have a value of, say, Φ, the transconductance will come to $\frac{n\alpha_F I_{tail}}{2V_T} =: g^n_m$ for $V_{in} \approx \Phi$. So, the gain of the multi-tanh structure with n differential pairs, all with the same offset, is n times bigger than the gain of a single differential pair.

When all offsets ϕ_i are taken equidistant according to a series

$$\phi_i = \frac{2i-1-n}{2} \cdot \Delta\Phi \quad \text{for} \quad 1 \leq i \leq n, \tag{3.24}$$

the transfer curves are spread evenly around $V_{in} = 0$. When $\Delta\Phi$ is taken 0, the case considered earlier arises. When $\Delta\Phi$ is increased, the transfer curves will move apart. The effect of this on the overall transconductance is that it gets wider and also lower. There exists a tradeoff between linear area and gain. This can be explained by the fact that the area of the overall transconductance function is independent of $\Delta\Phi$ or, in formula

$$\int_{-\infty}^{\infty} G_m^n(V_{in}) \mathrm{d}V_{in} \neq f(\Delta\Phi). \tag{3.25}$$

So changing $\Delta\Phi$ just changes the shape of the transconductance function; the area under it remains unchanged. When the transconductance curve would be modeled by a rectangle, the aspect ratio is dependent on $\Delta\Phi$ but the area is not. In this model, the height of the rectangle would stand for the gain and the width would be a measure for the size of the linear area.

When the transfer functions are shifted too much apart, i.e. $\Delta\Phi$ is made too large, the tails of the individual transconductance curves will not be large enough to compensate the tails of neighbouring curves. The overall transconductance will start showing a variation as a function of V_{in}. There is a value of $\Delta\Phi$, referred to as $\Delta\Phi_{max}$, for which the transconductance characteristic is maximally flat. Raising $\Delta\Phi$ beyond this value introduces a ripply nature in the transconductance characteristic. To find $\Delta\Phi_{max}$, a lot of algebra has to be performed. The assumption is made that for maximum flatness of $G_m^n(V_{in})$, its first derivative has to go through the origin exactly horizontal. This is the case when its first derivative, the second derivative of $G_m^n(V_{in})$ is 0 for $V_{in} = 0$. In formula, this means

$$\left.\frac{\partial^2 G_m^n}{\partial V_{in}^2}\right|_{V_{in}=0} = \left.\frac{\partial^3 I_{out}^n}{\partial V_{in}^3}\right|_{V_{in}=0} = 0, \tag{3.26}$$

which is very hard to calculate. From simulations, $\Delta\Phi_{max}$ was found to be $40mV$ to $60mV$, depending on the used type of transistor[1]. Figure 3.6 shows the transconductance as a function of input voltage for $\Delta\Phi = 0$, some values of $\Delta\Phi$ between 0 and $\Delta\Phi_{max}$, for $\Delta\Phi = \Delta\Phi_{max}$ and finally for a values of $\Delta\Phi$ greater than $\Delta\Phi_{max}$. The considered multi-tanh circuit consists of 8 differential pairs in parallel.

The mechanism of varying the transconductance at the expense of linear area size can be used fruitfully in automatic gain amplifiers. For small signals, the gain has to be large but the linear area can be small. For large input signals, the gain can be small. Now a large linear input range is needed.

[1]Especially the value of R_E, the emitter series resistance, appeared to be of great influence on $\Delta\Phi_{max}$ because of local feedback phenomena.

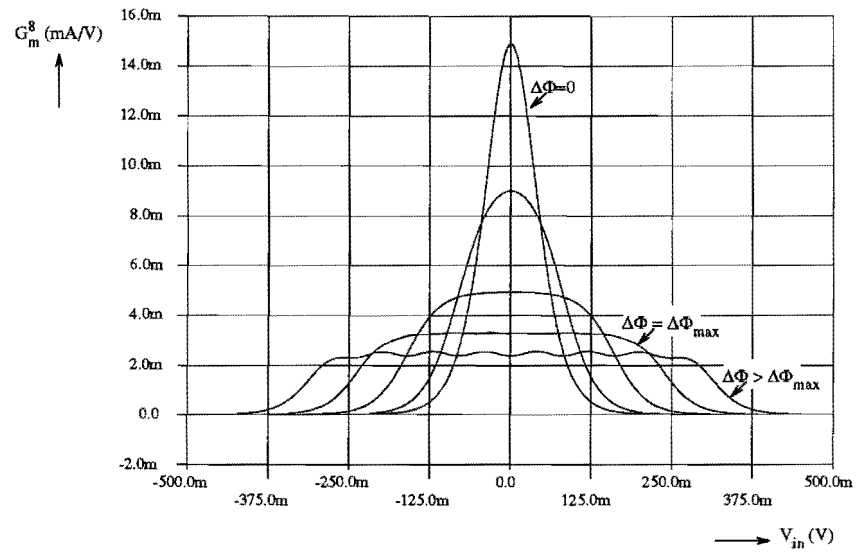

Figure 3.6: *Transconductance of the multi-tanh circuit as a function of input voltage*

3.2.2 Transconductance variation

To characterize the transconductance of the multi-tanh circuit, the value of G_m^n around $V_{in} = 0$ will be considered. This value is a function of the applied offset voltage $\Delta\Phi$, and of course of the number of pairs n and the transconductance g_m of these pairs. In the sequel, n is assumed to be even.

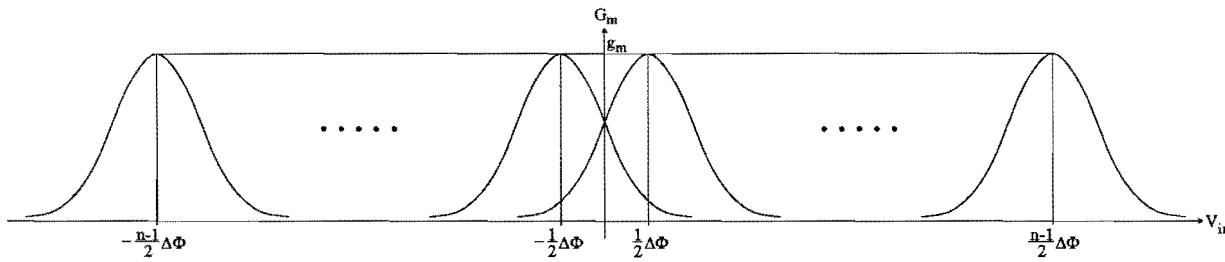

Figure 3.7: *Transconductance functions of individual differential pairs*

To calculate the gain around $V_{in} = 0$ for a given $\Delta\Phi$, figure 3.7 is considered. To $g_m^n := G_m^n(0)$, all differential pairs contribute. However, the contribution from the pairs operating around $V_{in} = 0$ is considerably larger than from pairs with large positive or negative offsets, whose only contributions are the asymptotic tails of their G_m-curve. After some manipulation, g_m^n can be written as a function of n and $\Delta\Phi$:

$$\begin{aligned} g_m^n &= G_m\left(-\frac{(n-1)\Delta\Phi}{2}\right) + \ldots + G_m\left(-\frac{3\Delta\Phi}{2}\right) + G_m\left(-\frac{\Delta\Phi}{2}\right) \\ &\quad + G_m\left(\frac{\Delta\Phi}{2}\right) + G_m\left(\frac{3\Delta\Phi}{2}\right) + \ldots + G_m\left(\frac{(n-1)\Delta\Phi}{2}\right), \end{aligned} \tag{3.27}$$

where $G_m(\cdot)$ is the transconductance function of a single differential pair, symmetrical around $V_{in} = 0$. Because of this symmetry, equation (3.27) can be rewritten as

$$g_m^n = 2\left[G_m\left(\frac{\Delta\Phi}{2}\right) + G_m\left(\frac{3\Delta\Phi}{2}\right) + \ldots + G_m\left(\frac{(n-1)\Delta\Phi}{2}\right)\right] \quad (3.28)$$

$$= 2\sum_{i=1}^{\frac{n}{2}} G_m\left(\frac{(2i-1)\Delta\Phi}{2}\right). \quad (3.29)$$

Figure 3.8 shows the normalized transconductance $\frac{g_m^n}{g_m}$ as a function of $\Delta\Phi$ for a multi-tanh circuit with 32 pairs in parallel.

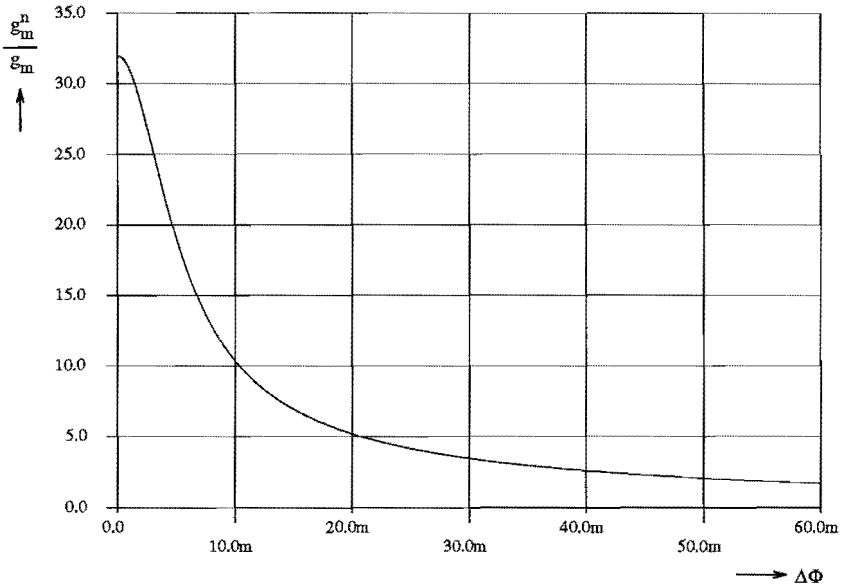

Figure 3.8: *Transconductance of the multi-tanh circuit as a function of offset voltage*

3.2.3 Gain range

An important characteristic of multi-tanh structures is the gain range, i.e. the difference between the gain at $\Delta\Phi = 0$ and $\Delta\Phi = \Delta\Phi_{max}$. This figure is dependent on the number of pairs n, as will be explained in the sequel.
In a previous section, the maximum gain (with $\Delta\Phi = 0$) for an n-fold differential pair was shown to be $g_m^n|_{\Delta\Phi=0} = \frac{n\alpha_F I_{tail}}{2V_T} = ng_m$, which from now on will be called $(g_m^n)_{max}$, the maximum small signal transconductance of an n-fold multi-tanh circuit.
To calculate $(g_m^n)_{min} := g_m^n|_{\Delta\Phi=\Delta\Phi_{max}}$, equation (3.29) can be used. To limit the number of terms in this sum, terms for which the argument of G_m is larger than $0.15V$ can be neglected, because the G_m function will have fallen to less than 1% of its maximum value by then. For $\Delta\Phi_{max} = 40mV$, terms with $i \geq 5$ can be neglected; for $\Delta\Phi_{max} = 60mV$,

terms with $i \geq 3$ can be neglected. Of course, this is only valid when n is large enough. Applying this to equation (3.29) yields

$$\begin{aligned}
\Delta\Phi_{max} = 40mV : (g_m^n)_{min} &= 2\sum_{i=1}^{4} G_m \left(\frac{(2i-1)\cdot 40\cdot 10^{-3}}{2} \right) = \frac{2.6\alpha_F I_{tail}}{2V_T} \\
&= 2.6 g_m \ @\ T = 300K, \\
\Delta\Phi_{max} = 60mV : (g_m^n)_{min} &= 2\sum_{i=1}^{2} G_m \left(\frac{(2i-1)\cdot 60\cdot 10^{-3}}{2} \right) = \frac{1.7\alpha_F I_{tail}}{2V_T} \\
&= 1.7 g_m \ @\ T = 300K.
\end{aligned}$$

The gain range follows by dividing the gain at $\Delta\Phi = 0$ by the values found in the previous equations. This leads to

$$\begin{aligned}
\Delta\Phi_{max} = 40mV &: \frac{(g_m^n)_{max}}{(g_m^n)_{min}} = 0.385n \text{ or } (20\log n - 8.3)dB, \\
\Delta\Phi_{max} = 60mV &: \frac{(g_m^n)_{max}}{(g_m^n)_{min}} = 0.588n \text{ or } (20\log n - 4.6)dB.
\end{aligned}$$

When for example 32 parallel pairs are used, the gain range will be between $21.8dB$ and $25.5dB$, depending on the type of transistor that is used.

3.2.4 Generating the offset voltages

To be able to vary the transconductance of the multi-tanh circuit, the offset voltages of the differential pairs must be made variable. However, the offset voltages must remain equidistant. So, in fact $\Delta\Phi$ must be made adjustable between 0 and about $40mV$ to $60mV$, depending on the transistor type in the differential pairs.
In the previous sections, a single ended input was considered. The other input terminal was used to apply the offset voltage to the differential pair. The voltage between the bases of pair i thus came to $V_{in} - \phi_i$, where $1 \leq i \leq n$. In figure 3.9 the location of these voltages on the V_{in}-axis is shown. To go from single ended to differential input operation, the input signal is assumed to consist of two components V_{pos} and V_{neg}, with $V_{in} = V_{pos} - V_{neg}$.

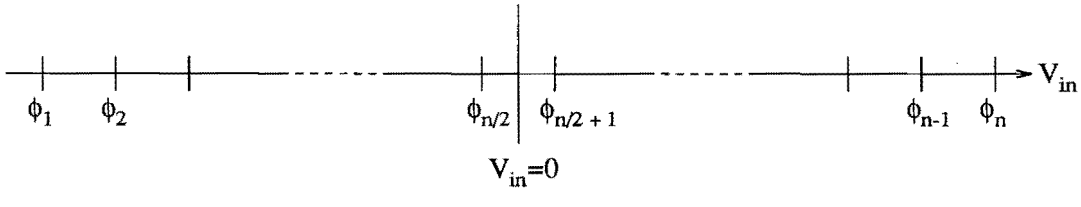

Figure 3.9: *Location of the differential pair base-to-base voltages*

Now, the offset voltages can also be divided in two parts $\phi_{i,pos}$ and $\phi_{i,neg}$, such that $\phi_{i,pos} - \phi_{i,neg} = \phi_i$. When input voltages $V_{pos} - \phi_{i,pos}$ and $V_{neg} - \phi_{i,neg}$ are applied to differential pair i, the voltage between its bases will become $V_{pos} - \phi_{i,pos} - (V_{neg} - \phi_{i,neg}) = V_{in} - \phi_i$.

When all offset voltages ϕ_i are taken equidistant according to equation (3.24), the values of both $\phi_{i,pos}$ and $\phi_{i,neg}$ will also be equidistant. The difference between two neighbouring values of $\phi_{i,pos}$ as well as $\phi_{i,neg}$ however will be $\frac{\Delta\Phi}{2}$. A possible choice for the values of $\phi_{i,pos}$ and $\phi_{i,neg}$ is shown in table 3.1. Here $\phi_{i,pos}$, resp. $\phi_{i,neg}$, is chosen according to a series which increases, resp. decreases, by $\frac{\Delta\Phi}{2}$ when i increases by 1. The result is that ϕ_i increases by $\Delta\Phi$ when i increases by 1. The values for ϕ_i are symmetric around 0, as was shown in figure 3.9.

Table 3.1: *Possible series $\phi_{i,pos}$ and $\phi_{i,neg}$*

i	$\phi_{i,pos}$	$\phi_{i,neg}$	$\phi_{i,pos} - \phi_{i,neg}$
1	0	$(n-1)\frac{\Delta\Phi}{2}$	$-(n-1)\frac{\Delta\Phi}{2}$
2	$\frac{\Delta\Phi}{2}$	$(n-2)\frac{\Delta\Phi}{2}$	$-(n-3)\frac{\Delta\Phi}{2}$
3	$2\frac{\Delta\Phi}{2}$	$(n-3)\frac{\Delta\Phi}{2}$	$-(n-5)\frac{\Delta\Phi}{2}$
⋮	⋮	⋮	⋮
$n-1$	$(n-2)\frac{\Delta\Phi}{2}$	$\frac{\Delta\Phi}{2}$	$(n-3)\frac{\Delta\Phi}{2}$
n	$(n-1)\frac{\Delta\Phi}{2}$	0	$(n-1)\frac{\Delta\Phi}{2}$

Figure 3.10 shows a possible construction to generate the base voltages for the differential pairs. All the voltage sources which provide for the offset voltages $\frac{\Delta\Phi}{2}$, $2(n-1)$ in total, have to be adjusted to the same value to get ϕ_i according to the series of equation (3.24). The voltage of these sources will have to be adjustable between 0 and about $20mV$ to $30mV$.

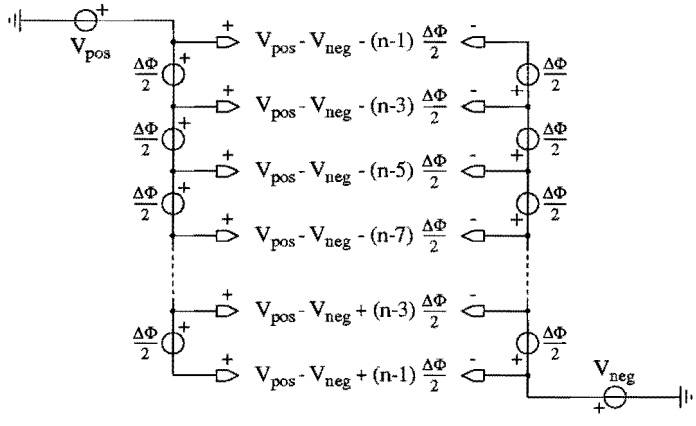

Figure 3.10: *Generation of the offset voltages*

3.2.5 Distortion

There are several causes for harmonic distortion, which will be treated separately. The most important ones are:

- Non-linearities in the transfer, caused by the finite number of differential pairs, all with a non-linear tanh-like transfer function. Because the circuit is completely differential and thus symmetrical, this will result in third- and higher odd-order distortion.
- Undesirable offsets in the differential pair transistors. These offset voltages will effectively change the value of the corresponding ϕ_i. This will have the same effect as mismatch in the voltage sources which take care of generating voltages $\phi_1 \ldots \phi_n$. Depending on the location of the error, usually higher order harmonic distortion will be the result.
- Mismatch in the tail current sources of the multi-tanh circuit. Much like the previous error, this will result in a local disturbance in the transfer and thus will usually cause higher order distortion.

The last two are specific for the used multi-tanh architecture. The first one is general for non-ideal systems and is also considered in appendix A.

Non-linearities in the transfer

Because of the complexity of the transfer function of the general multi-tanh circuit, calculating the level of harmonic distortion components is hard. However, when the number of parallel pairs is small, e.g. $n = 2$, distortion calculations are relatively simple. Comparing the distortion levels of a so called doublet (multi-tanh circuit with $n = 2$) and a simple differential pair will give some insight in the improvement that can be obtained by putting several differential pairs in parallel [4].
The general transfer function of a single differential pair is given by

$$I_{out} = \alpha_F I_{tail} \tanh \frac{V_{in}}{2V_T}, \tag{3.30}$$

which can be represented by a Taylor series in which only odd terms are present:

$$\begin{aligned} I_{out} &= \alpha_F I_{tail} \left(\frac{1}{2V_T} V_{in} - \frac{1}{24V_T^3} V_{in}^3 + \frac{1}{240V_T^5} V_{in}^5 - \ldots \right) && (3.31) \\ &= a_1 V_{in} + a_3 V_{in}^3 + a_5 V_{in}^5 + \ldots, && (3.32) \end{aligned}$$

for $|V_{in}| \ll 2V_T$. By substituting $V_{in} = \hat{v} \cos \omega t$, a Fourier series can be obtained from this Taylor series. From this, the harmonic distortion components can be calculated. This yields

$$\begin{aligned} HD_2 &= 0 \text{ and} && (3.33) \\ HD_3 &= \frac{1}{48} \left| \frac{\hat{v}}{V_T} \right|^2. && (3.34) \end{aligned}$$

For the doublet, the general transfer function is given by

$$I_{out} = \alpha_F I_{tail} \left(\tanh \frac{V_{in} - \frac{\Delta\Phi}{2}}{2V_T} + \tanh \frac{V_{in} + \frac{\Delta\Phi}{2}}{2V_T} \right). \tag{3.35}$$

The corresponding Taylor series can be written as

$$I_{out} = \alpha_F I_{tail} \left(\frac{\gamma_{\Delta\Phi}}{V_T} V_{in} + \frac{\beta_{\Delta\Phi}}{12 V_T^3} V_{in}^3 + \ldots \right) \tag{3.36}$$

$$= a_1 V_{in} + a_3 V_{in}^3 + \ldots, \tag{3.37}$$

where the following short hand notations are used:

$$\gamma_{\Delta\Phi} := \operatorname{sech}^2 \frac{\frac{\Delta\Phi}{2}}{2V_T} \quad \text{and} \tag{3.38}$$

$$\beta_{\Delta\Phi} := \gamma_{\Delta\Phi} \left(2\delta_{\Delta\Phi}^2 - \gamma_{\Delta\Phi} \right), \quad \text{with} \tag{3.39}$$

$$\delta_{\Delta\Phi} := \tanh \frac{\frac{\Delta\Phi}{2}}{2V_T}. \tag{3.40}$$

From this, the harmonic distortion components can be calculated again:

$$HD_2 = 0 \text{ and} \tag{3.41}$$

$$HD_3 = \frac{1}{48} \left| \frac{\hat{v}}{V_T} \right|^2 \frac{\beta_{\Delta\Phi}}{\gamma_{\Delta\Phi}}. \tag{3.42}$$

From equations (3.34) and (3.42) it is clear that the only difference between the distortion of the single differential pair and the doublet is the factor $\frac{\beta_{\Delta\Phi}}{\gamma_{\Delta\Phi}}$, which is dependent on the offset voltage $\Delta\Phi$. The distortion can be nulled by making this factor equal to zero. From equations (3.38) to (3.40) the following is found:

$$\begin{aligned}
& \frac{\beta_{\Delta\Phi}}{\gamma_{\Delta\Phi}} = 0 \\
\Rightarrow\ & 2\delta_{\Delta\Phi}^2 - \gamma_{\Delta\Phi} = 0 \\
\Rightarrow\ & 2\tanh^2 \frac{\frac{\Delta\Phi}{2}}{2V_T} = \operatorname{sech}^2 \frac{\frac{\Delta\Phi}{2}}{2V_T} = 1 - \tanh^2 \frac{\frac{\Delta\Phi}{2}}{2V_T} \\
\Rightarrow\ & \tanh \frac{\Delta\Phi}{4V_T} = \frac{1}{\sqrt{3}} \\
\Rightarrow\ & \Delta\Phi \approx 68.4mV \ @\ T = 300K.
\end{aligned}$$

So, by choosing $\Delta\Phi = 68.4mV \ @\ T = 300K$, the distortion of the doublet is nulled. In reality however, current source mismatch and transistor mismatch add distortion that will put a lower bound on the linearity of the multi-tanh structure. These effects will be considered next.

Differential pair and offset voltage mismatch

When the input terminals of an ideal differential pair are connected together, the base-to-base voltage is $0V$ and thus the current through both transistors is equal. In a real differential pair however, there will be an offset voltage in series with the differential input voltage. This is caused by mismatches in base width, base and collector doping level and effective emitter area of the two transistors. In figure 3.11 an ideal differential pair is shown, together with the offset voltage source V_{OS}. The differential input voltage of the ideal differential pair now is $V_{in} + V_{OS}$.

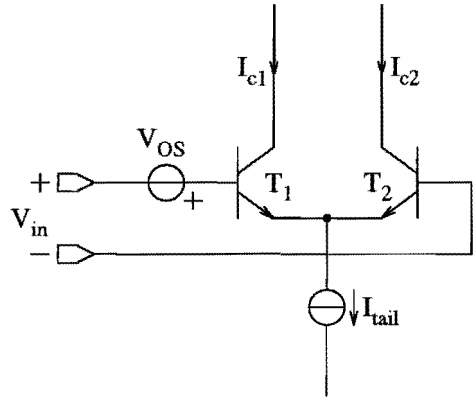

Figure 3.11: *Offset voltage in the differential pair*

In an ideal multi-tanh circuit, the differential input voltage of each pair i is $V_{in} - \phi_i$. In a non-ideal circuit, the effective input voltage will come to $V_{in} - \phi_i + V_{OS_i}$ because of device mismatch. The same effect occurs when there is a deviation V_{δ_i} in ϕ_i, caused by mismatch in the structure which generates the offset voltages $\phi_1 \ldots \phi_n$. The effective input voltage to differential pair i will become $V_{in} - \phi_i + V_{\delta_i} + V_{OS_i}$. The total error voltage will be defined as $V_{error_i} := V_{\delta_i} + V_{OS_i}$. Instead of ϕ_i, the effective offset voltage of pair i will thus be $\phi_i - V_{error_i}$.
The error voltages will cause a deviation in the equidistance of the offset voltages. Consider the case that all error voltages are zero except for one, say V_{error_j}. For the transconductance curves, this results in the situation of figure 3.12.

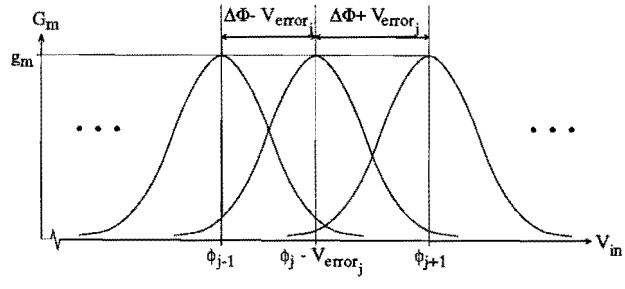

Figure 3.12: *Shifting of a transconductance curve caused by mismatch*

An error like this will disturb the total transconductance curve G_m^n around $V_{in} = \phi_j - V_{error_i}$, which will result in harmonic distortion. The effect of the error will only be noticeable in the proximity of ϕ_j, because the individual G_m-curves are active in a limited area of V_{in}. When the number of pairs n is assumed to be large, the total transconductance will ideally be constant for a large range of V_{in}. The shifting of one of the transconductance curves will cause a ripple in G_m^n. The total transconductance will increase in the interval where the distance between two neighbouring curves has decreased and vice versa. The error in the total transconductance can be defined as the normalized difference between the shifted version of transconductance curve j and the ideal one which has not shifted:

$$\Delta G_m^n = \frac{1}{g_m^n}\left[G_m\left(V_{in} - (\phi_j - V_{error_j})\right) - G_m\left(V_{in} - \phi_j\right)\right] \tag{3.43}$$

$$= \frac{g_m}{g_m^n}\left[\operatorname{sech}^2\frac{V_{in} - \phi_j + V_{error_j}}{2V_T} - \operatorname{sech}^2\frac{V_{in} - \phi_j}{2V_T}\right]. \tag{3.44}$$

When $V_{error} = 0$, this expression is 0 for all values of V_{in}. When $|V_{error}|$ increases, a ripple appears. In figure 3.13 the variation in G_m^n, normalized to $\frac{g_m}{g_m^n}$, is shown as a function of V_{in} and V_{error}. It can be seen from this picture that for $V_{error} = 0$ there is no ripple.

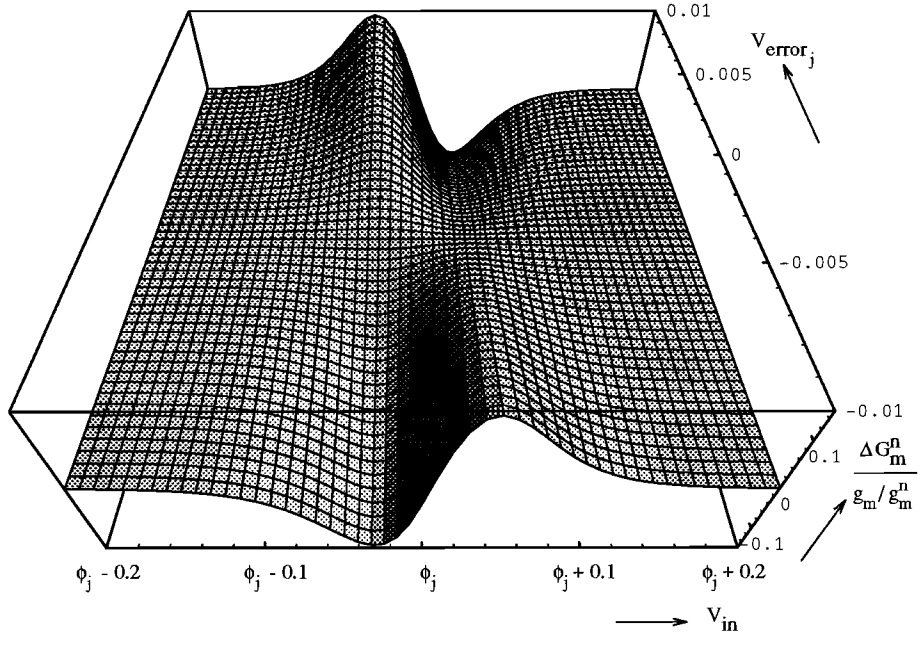

Figure 3.13: *The error in G_m^n as a function of V_{in} and V_{error}*

For an error voltage of $\pm 10mV$, the deviations in G_m^n are approximately $\pm 0.15\frac{g_m}{g_m^n}$, which is about $\pm 7.5\%$ at minimum gain. The situation with minimum gain is worst case, because $\frac{g_m}{g_m^n}$ reaches a maximum then. The effect this has on the harmonic distortion is highly dependent on the amplitude of the input signal and the location of the error. When the

input amplitude is much smaller than ϕ_j, the error will not have any effect on the distortion. When the input amplitude is about as large as ϕ_j, the error will cause low-order distortion, because only the peak of the input signal is affected. Finally, when the amplitude of the input signal is larger than ϕ_j, higher-order distortion will be the result. In figure 3.14 Fourier transforms of the output signal in these three cases are given.

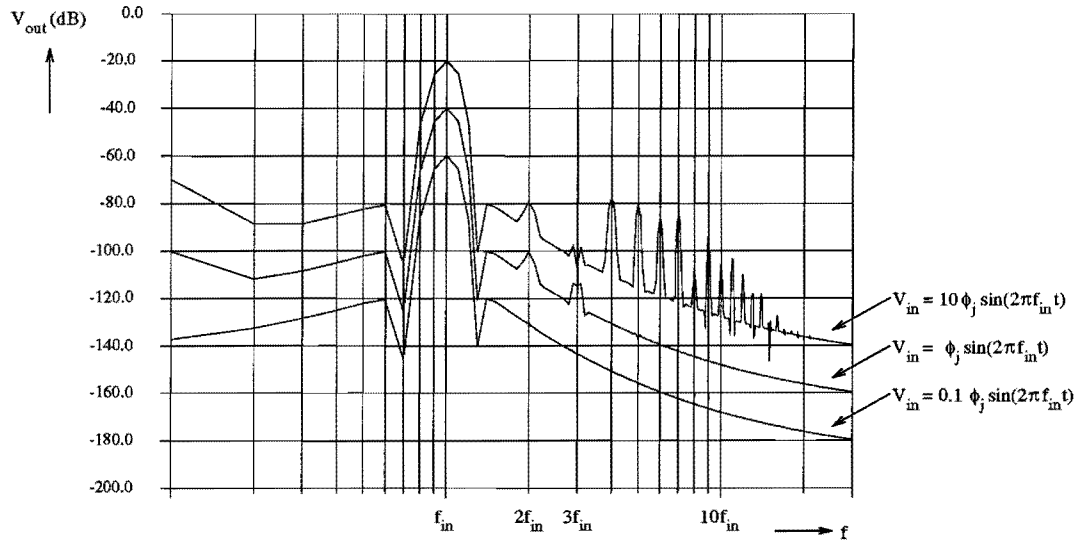

Figure 3.14: *Fourier transforms of the distorted output signal*

The above considered case, where only one of the differential pairs is erroneous, can be extended to the general case where all differential pairs are erroneous. However, this general case is very complicated and will not be treated here.

Current source mismatch

For mismatch in the tail current sources of the multi-tanh circuit, a similar effect as described in the previous section occurs. Consider the case that the tail current source of differential pair j has a value of $I_{tail} + \Delta I_{tail}$ instead of I_{tail}. Again, the deviation of G_m^n can be written as the difference between the disturbed transconductance curve and the ideal one:

$$\Delta G_m^n = \frac{\alpha_F(I_{tail} + \Delta I_{tail})}{2V_T} \operatorname{sech}^2 \frac{V_{in} - \phi_j}{2V_T} - \frac{\alpha_F I_{tail}}{2V_T} \operatorname{sech}^2 \frac{V_{in} - \phi_j}{2V_T} \tag{3.45}$$

$$= \frac{\Delta I_{tail}}{I_{tail}} \operatorname{sech}^2 \frac{V_{in} - \phi_j}{2V_T}. \tag{3.46}$$

In figure 3.15 the deviation in G_m^n is plotted as a function of V_{in} and $\frac{\Delta I_{tail}}{I_{tail}}$ for the pair with

offset voltage ϕ_j. For $\Delta I_{tail} = 0$ and thus $\frac{\Delta I_{tail}}{I_{tail}} = 0$, the deviation in G_m^n is also 0 and the resulting G_m^n-curve is flat.

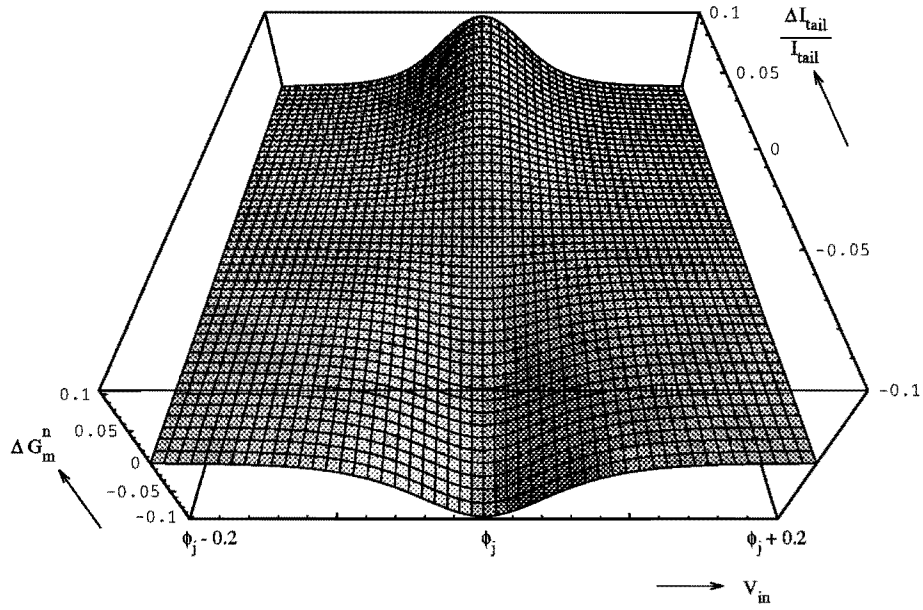

Figure 3.15: *The error in G_m^n as a function of V_{in} and $\frac{\Delta I_{tail}}{I_{tail}}$ of pair j*

From this picture it can be seen that the error in G_m^n varies linearly with the error in the tail current. For the resulting distortion, the same effects occur as in the previous section with transistor and offset mismatch.

3.2.6 Noise

The multi-tanh circuit considered so far, consisted of coupled differential pairs, driven by ideal tail current sources and ideal input voltage sources. The output was a differential current. The only noise sources in this circuit are the transistors in the differential pairs. In reality however, there will be additional noise sources because of the non-ideal implementation of the circuit. The most important ones are:

- The tail current sources, consisting of one transistor and a degeneration resistor. The circuit which provides the bias signal will also contribute noise.
- The structures which take care of generating the offset voltages, consisting of an emitter follower, loaded with a resistor ladder and a variable current source.
- The load resistors of the circuit, which take care of converting the output currents of the multi-tanh circuit into voltages.

Before taking all these noise sources in consideration, some general noise aspects of bipolar transistors will be described.
For a bipolar transistor, the hybrid-π model is often used in small signal analyses. This hybrid-π model can be extended to the model of figure 3.16, the hybrid-π model with noise sources [3].

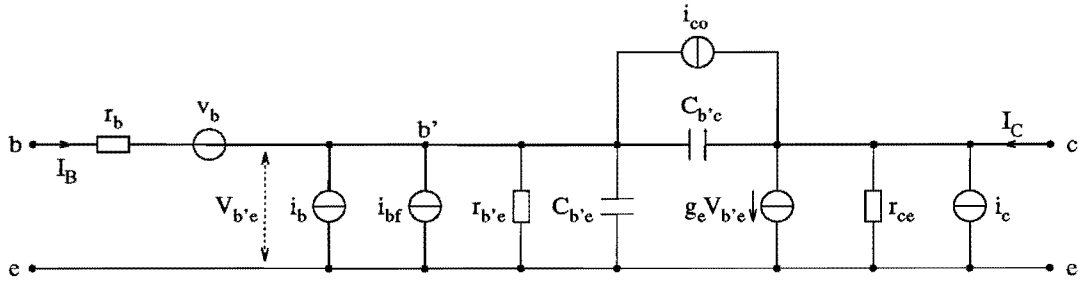

Figure 3.16: *Bipolar hybrid-π model with noise sources*

In this model, shot noise, thermal noise and $1/f$-noise are taken into account. The noise sources have the following mean-square values:

$$\overline{v_b^2} = 4kTr_b\Delta f, \tag{3.47}$$
$$\overline{i_b^2} = 2qI_B\Delta f, \tag{3.48}$$
$$\overline{i_{bf}^2} = 2qI_B\Delta f(f_l/f), \tag{3.49}$$
$$\overline{i_c^2} = 2qI_C\Delta f = 2kTg_e\Delta f, \tag{3.50}$$
$$\overline{i_{co}^2} = 2qI_{cob}\Delta f, \tag{3.51}$$

where f_l is the frequency where the white noise and $1/f$-noise have the same power density and I_{cob} is the collector reverse current. Because the circuit will operate on a frequency of about $60MHz$ and f_l is less than $100Hz$, the contribution of $\overline{i_{bf}^2}$ can be neglected. For silicon transistors, I_{cob} is very low, so $\overline{i_{co}^2}$ can also be neglected. When also i_c is transformed to the input, this results in the model of figure 3.17.

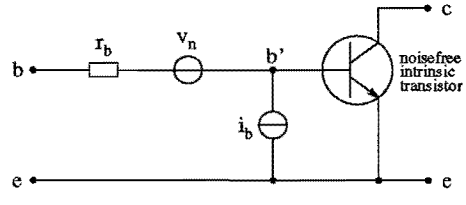

Figure 3.17: *Bipolar transistor with noise sources*

The noisefree intrinsic transistor models the complete noisefree transistor without base resistance. When i_c is transformed to the input, this results in a noise voltage source i_c/g_e, which can be added to v_b to become v_n:

$$\overline{v_n^2} = \overline{v_b^2} + \overline{(i_c/g_e)^2} = 4kT\left(r_b + \frac{1}{2}r_e\right)\Delta f, \tag{3.52}$$

where $r_e = \frac{1}{g_e}$. When the base voltage is supplied by a source with low impedance, i_b can be transformed to a voltage source in series with v_n. Under the assumption that $I_B \approx \frac{I_C}{r_{b'e}g_e}$, the following holds:

$$\overline{(r_b i_b)^2} = r_b^2 2qI_B\Delta f = 2kT\frac{r_b^2}{r_{b'e}}\Delta f. \tag{3.53}$$

Joining v_n and $r_b i_b$ in one voltage source, gives

$$\overline{v_r^2} = \overline{v_n^2} + \overline{(r_b i_b)^2} = 4kT\left(r_b + \frac{1}{2}r_e + \frac{1}{2}\frac{r_b^2}{r_{b'e}}\right)\Delta f. \tag{3.54}$$

So in a situation where the base voltage is supplied by a low-impedance source, noise can be modeled by a noisy base series resistance with value $R_r := r_b + \frac{1}{2}r_e + \frac{1}{2}\frac{r_b^2}{r_{b'e}}$.

Differential pairs

The input noise for the differential pair can be modeled by two independent noise voltage sources in series with the bases. The influence of these noise sources on the output signal depends on the state of the differential pair. If the differential pair is operating in its active area (base-to-base voltage smaller than approximately $2V_T$), the noise voltages will influence the current distribution in the differential pair. This will result in output noise. However, when the base-to-base voltage is larger than about $2V_T$, the current distribution is independent of the base-to-base voltage. The complete tail current will flow through only one of the transistors. In this case the noise will not influence the output current.
In the multi-tanh structure, only the active differential pairs will contribute noise to the output signal. When $\Delta\Phi$ is large, only a limited number of differential pairs will be active at the same time and this will be worst case. The noise of the circuit will be about the same as for a single differential pair. However, when $\Delta\Phi = 0$, all pairs will be active at the same time. This situation, including noise sources, is depicted in figure 3.18(a). Noise sources $v_{r_{ia}}$ and $v_{r_{ib}}$ of differential pair i can be added together into one voltage source v_{r_i}, with

$$\begin{aligned} \overline{v_{r_i}^2} &= \overline{v_{r_{ia}}^2} + \overline{v_{r_{ib}}^2} && (3.55)\\ &= 2\overline{v_{r_{ia}}^2} && (3.56)\\ \Rightarrow v_{r_i} &= \sqrt{2}v_{r_{ia}}, && (3.57) \end{aligned}$$

when $v_{r_{ia}}$ and $v_{r_{ib}}$ are assumed to be uncorrelated and equal in rms-value. In figure 3.18(b) the multi-tanh circuit with noise sources is depicted. The drawn transistors are noiseless.

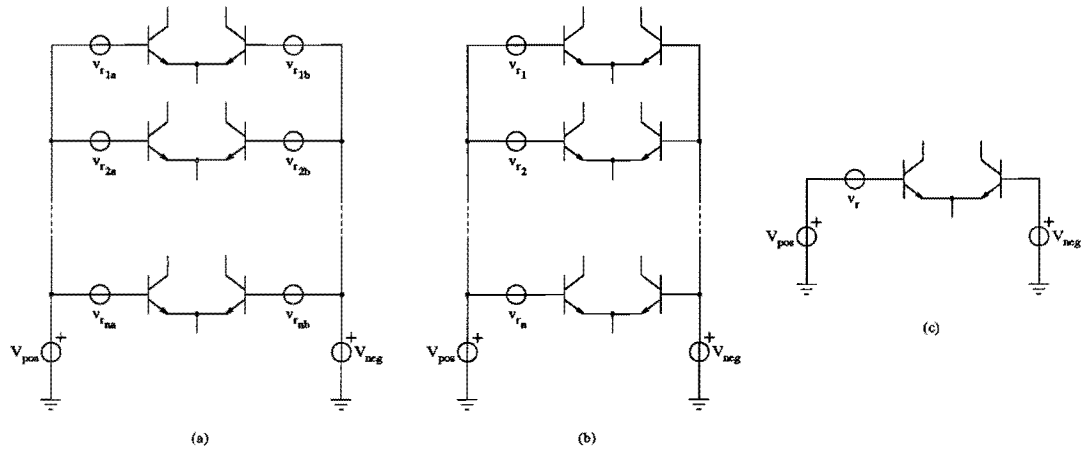

Figure 3.18: (a) *Multi-tanh structure with noise sources,* (b) *Noise sources moved to one side,* (c) *Equivalent simplified circuit*

If all differential pairs are assumed to have the same transconductance g_m and the noise sources are uncorrelated and have the same rms-value, the value of the total noise at the output will be:

$$v_{r,out} = \sqrt{\overline{(g_m v_{r_1})^2} + \overline{(g_m v_{r_2})^2} + \ldots + \overline{(g_m v_{r_n})^2}} \tag{3.58}$$

$$= \sqrt{n g_m^2 \overline{v_{r_1})^2}} \tag{3.59}$$

$$= \sqrt{n} g_m v_{r_1}. \tag{3.60}$$

When this noise voltage is transformed back to the input, as shown in figure 3.18(c), it has to be divided by the gain of the circuit, which is ng_m for $\Delta\Phi = 0$. The noise voltage now becomes

$$v_r = \frac{1}{\sqrt{n}} v_{r_1} \tag{3.61}$$

$$= \frac{1}{\sqrt{\frac{1}{2}n}} v_{r_{1a}}, \tag{3.62}$$

where $v_{r_{1a}}$ is the noise voltage of a single bipolar transistor, given in equation (3.54). So for a multi-tanh circuit with 32 parallel pairs, the noise voltage at the input (as shown in figure 3.18(c) above) is 0.25× the noise voltage of a single bipolar transistor when the circuit is adjusted to maximum gain. The noise of the complete circuit will be between 0.25× and 1× the noise of a single differential pair. Tail current sources and load resistors are assumed to be ideal. Their noise contribution will be considered next.

Tail current sources

Previously, the tail current sources were considered to deliver a perfectly constant current. In practice, this current will show fluctuations because of transistor and resistor noise.

The tail current source circuit, including biasing, is shown in figure 3.19(a). Noise voltage source v_r comprises both transistor noise and noise from the biasing circuit. Degeneration resistor R_e is also assumed to be noisy.

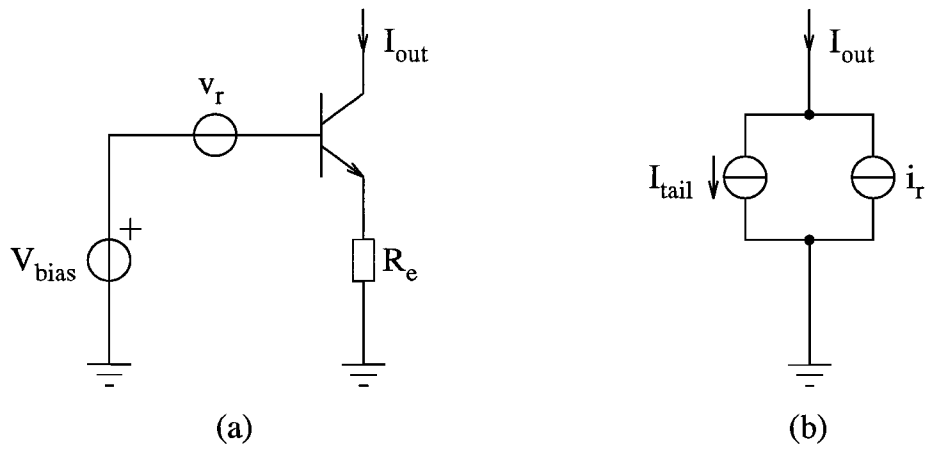

Figure 3.19: (a) *Noisy tail current source with biasing,* (b) *Equivalent simplified circuit*

The noise of degeneration resistor R_e has a mean-square value of $\overline{v_{R_e}^2} = 4kTR_e\Delta f$. This noise can be modeled by a voltage source in series with a noiseless version of R_e. Noise voltage source v_r can be moved in series with R_e for noise considerations also. Because v_{R_e} and v_r are not correlated, they can be added together to one voltage source with mean-square value $\overline{v_n^2} = \overline{v_{R_e}^2} + \overline{v_r^2}$.
The noise voltage v_r consists of the noise voltage generated by the transistor and the noise voltage generated by the bias circuit. This last component is not important, because all tail current sources are biased by the same circuit. A noisy bias voltage will result in a common mode noise at the output of the multi-tanh circuit. Because the circuit is completely differential, this noise will not influence the performance.
The noise from the current source transistor is given by equation (3.54). The mean-square value of the complete noise voltage comes to $\overline{v_n^2} = 4kT\left(R_e + R_r\right)\Delta f$. Dividing this voltage by R_e gives the noise current i_r of figure 3.19(b):

$$\overline{i_r^2} = \overline{\left(\frac{v_{R_e}^2}{R_e}\right)^2} + \overline{\left(\frac{v_r^2}{R_e}\right)^2} \tag{3.63}$$

$$= 4kT\left(\frac{1}{R_e} + \frac{R_r}{R_e^2}\right)\Delta f. \tag{3.64}$$

Because $R_r \ll R_e^2$, the term $\frac{R_r}{R_e^2}$ can be neglected with respect to the term $\frac{1}{R_e}$. The noise current of the tail current source thus comes to $\overline{i_r^2} = \frac{4kT}{R_e}\Delta f$.
The influence of the noisy tail current sources on the overall noise behaviour depends on the configuration of the multi-tanh circuit. When all pairs are put in parallel ($\Delta\Phi = 0$), tail current noise results in a common mode noise, which does not deteriorate the completely differential circuit. When a large $\Delta\Phi$ is applied, noise currents through both load resistors

will not be correlated, which will result in differential mode noise. Each of the two load resistors will receive half the number of available tail currents, including noise. The total noise current which flows through a load resistor will be the sum of $\frac{n}{2}$ uncorrelated noise currents from the tail current sources:

$$\overline{i_{r_l}^2} = \frac{n}{2}\overline{i_r^2} \tag{3.65}$$

$$= \frac{2nkT}{R_e}\Delta f. \tag{3.66}$$

Because the circuit is differential and the noise in the positive load resistor and the negative load resistor is uncorrelated, the differential noise current originating from tail current source noise is

$$\overline{i_{diff}^2} = 2\,\overline{i_{r_l}^2} \tag{3.67}$$

$$= \frac{4nkT}{R_e}\Delta f. \tag{3.68}$$

With (noiseless) load resistors R_l, this results in a differential output noise voltage of

$$\overline{v_{diff}^2} = \overline{(i_{diff}R_l)^2} = 4kTn\frac{R_l^2}{R_e}\Delta f \tag{3.69}$$

$$\Rightarrow v_{diff} = \sqrt{4kTn\frac{R_l^2}{R_e}\Delta f}. \tag{3.70}$$

This noise will increase because the load resistors themselves also generate noise. This will be considered next.

Load resistors

The thermal noise generated by a conductor with resistance R_l can be expressed as follows:

$$\overline{v_{R_l}^2} = 4kTR_l\Delta f. \tag{3.71}$$

In the multi-tanh circuit, both load resistors will generate a noise voltage which will add directly to the output voltage. Because the noise from the two load resistors is uncorrelated, the differential noise voltage can be found by

$$\overline{v_{diff}^2} = 2\overline{v_{R_l}^2} = 8kTR_l\Delta f \tag{3.72}$$

$$\Rightarrow v_{diff} = \sqrt{8kTR_l\Delta f}. \tag{3.73}$$

This is a constant noise source, which does not depend on the configuration of the multi-tanh circuit.

Offset generation ladders

The offset generation ladders take care of generating a series of equidistant voltages related to the input signal. The distance of the voltages can be adjusted by means of varying the current through the ladder. In figure 3.20, the noise model of this ladder is shown.

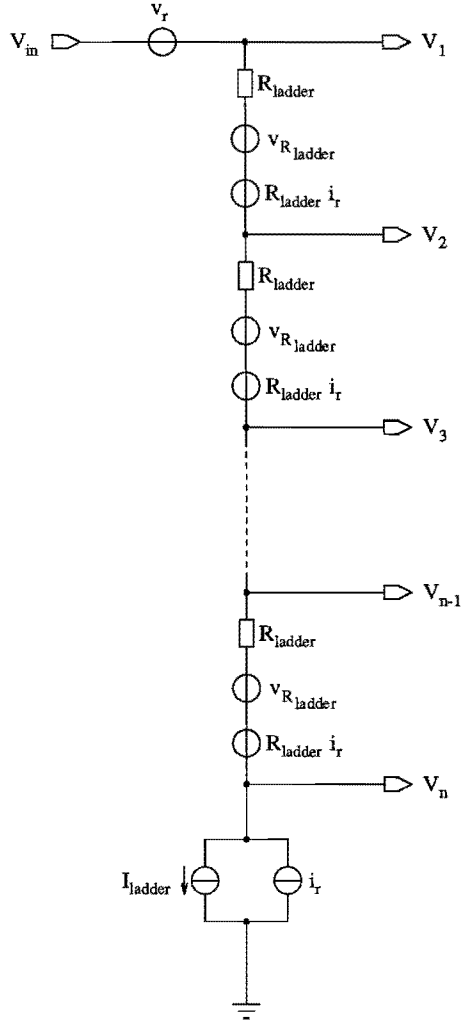

Figure 3.20: *Simplified offset generation ladder with noise sources*

Not shown is the input transistor, used as emitter follower. Noise contributing elements in this structure are the input transistor, the ladder resistors and the ladder current source. The latter will generate a noise voltage in the ladder resistors. In figure 3.20, both the ladder current noise source and the resulting noise voltage sources are drawn. These noise voltage sources are fully correlated. The noise voltage source in series with the input (v_r) originates from the input transistor.
Its clear that, because node V_1 is used as a reference for the complete ladder, the noise

voltage present on node V_i will increase with increasing i. For the mean-square value of the noise voltage present on node V_i,

$$\overline{v_i^2} = \overline{v_r^2} + (i-1)\overline{v_{R_{ladder}}^2} + \overline{((i-1)R_{ladder}i_r)^2} \tag{3.74}$$

can be written. Because of the differential operation of the circuit, there are two ladders. The differential pairs are cross coupled between these two ladders (cf. figure 3.10). The resulting differential noise for pair i can be calculated as follows[2]:

$$\begin{aligned} \overline{v_{diff_i}^2} &= \overline{v_i^2} + \overline{v_{n-i}^2} && (3.75) \\ &= 2\overline{v_r^2} + (n-2)\overline{v_{R_{ladder}}^2} + (n^2 - 2ni - 2n + 2i^2 + 2)\overline{(R_{ladder}i_r)^2}. && (3.76) \end{aligned}$$

Like with differential pair noise, this noise has the most influence on the performance when $\Delta\Phi = 0$. In this case, the total differential noise voltage at the input of the n parallel differential pairs can be shown to be

$$v_{diff} = \frac{1}{n}\sqrt{\sum_{i=1}^{n}\overline{v_{diff_i}^2}}. \tag{3.77}$$

Total noise

The total noise of the circuit will consist of all the uncorrelated noise sources described in the previous sections. The noise contribution of the tail current sources can be neglected in comparison with the differential pair and load resistor noise contributions. The noise contribution of the input ladders will also be small for a large number of pairs in parallel. From the above follows that worst case noise performance will occur when the circuit is adjusted to minimum gain ($0dB$). The mean-square value of the equivalent input noise voltage then comes to

$$\overline{v_{total}^2} \approx 8kT\left(R_l + R_r\right)\Delta f. \tag{3.78}$$

In reality, $R_l \approx 760\Omega$ and $R_r \approx 1.6k\Omega$, which yields a total worst case noise voltage of about $8.8nV/\sqrt{Hz}$. Best case is a quarter of this value, which is about $2.2nV/\sqrt{Hz}$. In reality, noise levels will be somewhat higher, because in the above only the two most important sources have been considered.

3.2.7 Conclusions

By putting several differential pairs in parallel and applying a variable offset voltage to each of these pairs, an amplifier with a variable gain can be constructed. Calculations yield that to get a gain range of about $25dB$, 32 differential pairs should be put in parallel.

[2]This is not completely correct, because the ladder current noise sources show a little correlation since they are biased from the same circuit. However, their correlation can be neglected because other, uncorrelated noise sources dominate.

By varying the offset voltage between each two neighbouring pairs from 0 to about $40mV$ to $60mV$, the gain can be varied between its maximum value and minimum value over a range of about $25dB$.
In the multi-tanh structure several sources of harmonic distortion are present. Mismatch between the differential pair transistors, the offset voltages and the tail current sources are the most important ones. To minimize distortion, the differential pair transistors should not be too small and they should be as close as possible to each other on the layout. The same goes for the tail current sources, which also should be biased by the same bias circuit. The ladders that take care of generating the offset voltages should consist of resistors that are considerable in size. The relative value of the resistors is more important than the absolute value.
The most important noise sources are the offset generation ladders, the tail current sources, the differential pair transistors and the load resistors. To minimize the effects of these noise sources, several measures should be taken. The resistors in the offset generation ladders should be small in value to reduce thermal noise. Transistors should be as large as possible. The tail current sources should be degenerated with a large resistor to minimize noise current. The voltage drop over the tail current source limits the value of the degeneration resistor. Thermal noise of the load resistors can be limited by choosing their value not too large.

Chapter 4

Implementation in QUBiC1

In this chapter, the implementation in QUBiC1 of the previously treated circuits will be described. This involves choosing transistor and resistor types and optimizing the circuit using simulation results. Also the bias circuitry, left unconsidered until now, will be filled in. Each of the blocks in the complete circuit will be described separately. First, an overview of the complete circuit will be given.

4.1 Block diagram

Figure 4.1 on the next page shows the complete block diagram of a 32-fold multi-tanh circuit, including bias circuits, input buffers and load circuit. Each of the blocks will be dealt with separately in the next sections.
The basic circuit, shown in figure 4.1, was designed to have a gain that is adjustable between $0dB$ and $25dB$. With this basic circuit, four different chips were constructed. They are named 'onestage', 'twostage', 'threestage' and 'threesep'. In table 4.1, their characteristics have been put together.

Table 4.1: *Chip version characterization*

Property	'onestage'	'twostage'	'threestage'	'threesep'
Number of cascades	1	2	3	3
Minimum gain	$0dB$	$0dB$	$0dB$	$0dB$
Maximum gain	$25dB$	$50dB$	$75dB$	$75dB$
Gain range	$25dB$	$50dB$	$75dB$	$75dB$
Power supply	combined	combined	combined	separate

The next chapter will deal with some layout topics of these four chips. Hard-copies of the layouts can be found in appendix C. At the end of this chapter, some simulation results of the complete circuit are included.

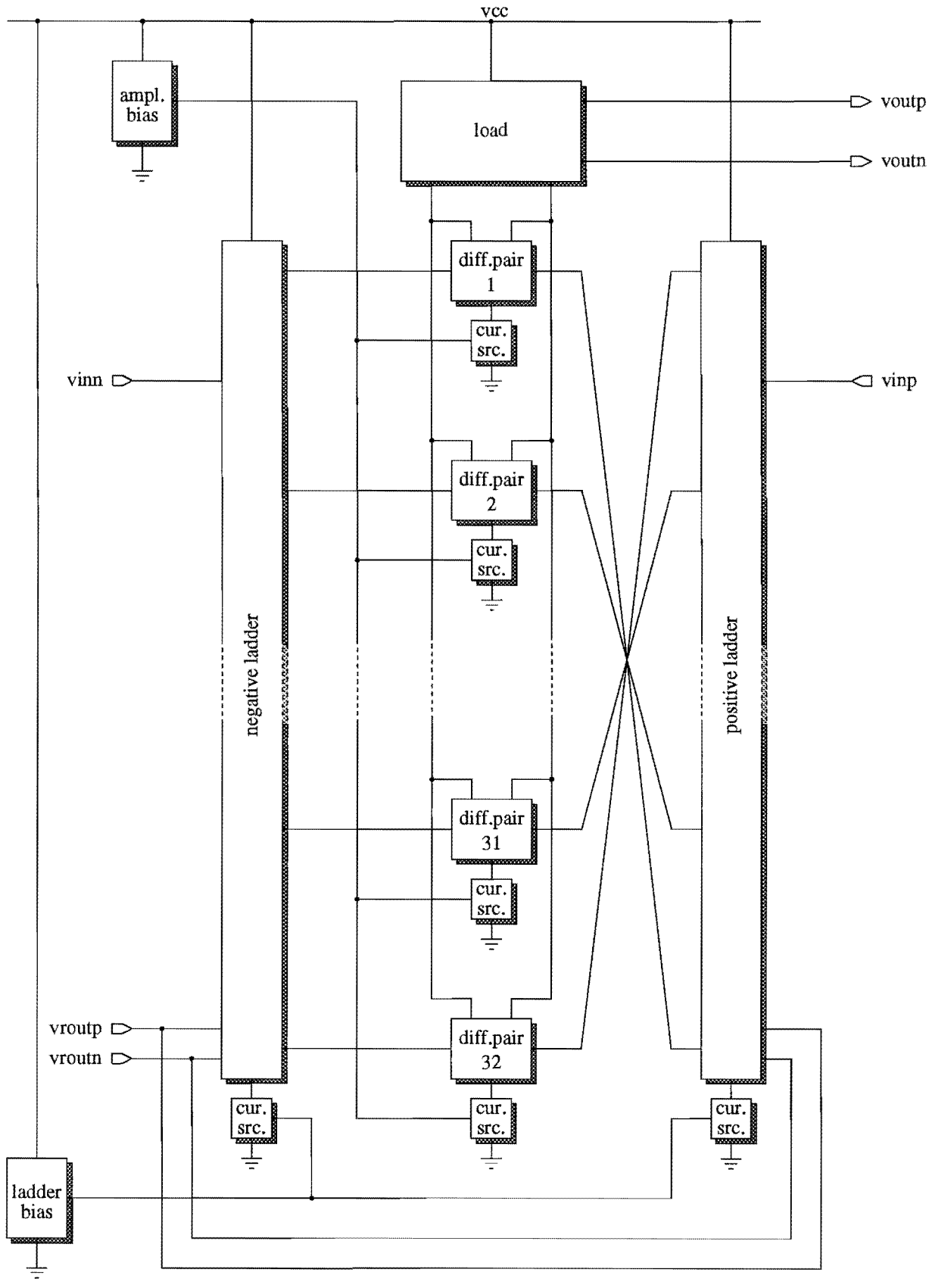

Figure 4.1: *Block diagram of the complete 32-fold multi-tanh circuit*

4.2 Differential pairs

The transistors in the differential pairs have to fulfill several demands. The most important ones are:

- Low base resistance r_b. Because the base current varies with collector current, the voltage drop across the base resistance will also vary. When the base resistance is large, this will result in a large, collector current dependent, voltage drop.
- High forward current gain β_F. This will result in a low base current, which will cause less voltage drop across the base resistor. The lower the base current is, the higher the impedance of the offset generation ladder is allowed to be. When the impedance of the ladder is too low, the base currents will influence the offset voltages. Also, the lower the ladder impedance is, the higher the ladder current has to be to obtain the same offset voltages. High ladder impedance thus results in low power consumption.
- Good matching capabilities. The two transistors in a differential pair have to be closely matched to prevent offsets from occurring. The smaller transistors are, the harder it is to match them. By giving two transistors the same orientation on the layout and by putting them as close to each other as possible, matching can be improved.
- Low collector capacitance C_{jc}. Because a lot of collectors will be connected together, the capacitance on the collector node (the sum of all the individual collector capacitances) will be high. Together with the load resistor, this capacitance will cause a time constant, which has to be low enough to allow the system to run at about $60MHz$ without too much attenuation.

The choice was made for a small transistor. Apart from matching capabilities, it satisfies most needs reasonably. It also makes low power operation possible without bandwidth problems. The transistor is named BNB020NTW in QUBiC1 and some of its properties are listed in table 4.2 below.

Table 4.2: *Properties of NPN-transistor BNB020NTW*

Property	Symbol	Value
Emitter area	A_E	$1\mu m \times 2\mu m$
Base series resistance	r_b	539.2Ω
Emitter series resistance	r_e	30.8Ω
Collector series resistance	r_c	115Ω
Forward current gain	β_F	127.5
Zero bias emitter depletion capacitance	C_{jc}	$7.13fF$
Zero bias collector-base depletion capacitance	C_{je}	$4.7fF$

The peak value of f_T is reached at a collector current of about $400\mu A$. For higher collector currents the value of f_T will decrease rapidly. Thus, operation at collector currents of more than $400\mu A$ should be avoided, unless the device is operated at very low frequencies. Figure 4.2 shows the final implementation of the differential pair with terminal naming.

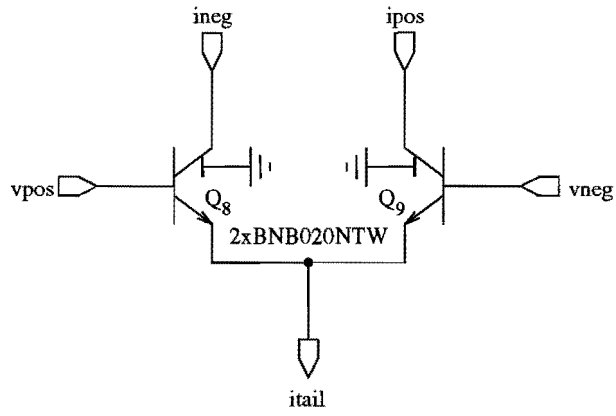

Figure 4.2: *The differential pair with terminals*

4.3 Tail current sources

The current sources have to supply the differential pairs with a constant tail current. Figure 4.3 shows the implementation of the current source. The applied type of transistor is the same as in the differential pair, the BNB020NTW.

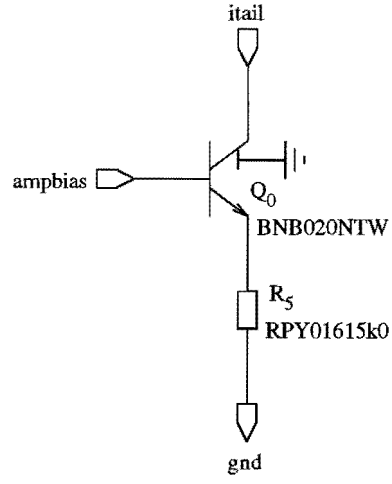

Figure 4.3: *The tail current source*

Ideally, when the terminal named 'ampbias' is kept at a constant voltage $V_{ampbias}$, the collector current of Q_0 will be constant. The value of this current depends mainly on the

value of $V_{ampbias}$ and R_5. The voltage $V_{ampbias}$ is generated by one common circuit for all 32 differential pairs. This means that ideally all 32 current sources should generate exactly the same current when their resistors have the same value.
In reality however, the generated currents will show deviations from the ideal value because of the finite output impedance of the current sources and also because of mismatch in the transistors and resistors. A limited output impedance will make the output current depend on the voltage across the current source. Mismatch in transistors and resistors will cause the currents, generated by the different current sources, to be unequal.
The output impedance R_0 of a current source without degeneration, that is $R_5 = 0$, is the same as the output impedance r_0 of the transistor. For a current source degenerated with resistor R_5 and generating a current I_{tail}, the output impedance is [4]

$$R_0 = r_0 \left(1 + \frac{I_{tail} R_5}{V_T}\right). \tag{4.1}$$

It can be observed from this equation that the output impedance R_0 can be increased by increasing either the output current or the value of the degeneration resistor. Increasing the output current is impractical, because its value is usually determined by the rest of the circuit. Increasing the value of the degeneration resistor can only be done to a certain extent because the voltage space of the current source is usually limited. The voltage drop across the current source increases as the degeneration resistor does.
The sensitivity of the output current to transistor and resistor mismatch also depends on the value of R_5. In [4], appendix A4.1, the following relation is derived:

$$\left|\frac{\Delta I_{tail}}{I_{tail}}\right| \simeq \left(\frac{1}{1 + \frac{g_m R_5}{\alpha_F}}\right) \frac{\Delta I_S}{I_S} + \frac{\frac{g_m R_5}{\alpha_F}}{1 + \frac{g_m R_5}{\alpha_F}} \left(-\frac{\Delta R_5}{R_5} + \frac{\Delta \alpha_F}{\alpha_F}\right), \tag{4.2}$$

where $g_m = \frac{I_{tail}}{V_T}$. From this formula it can be seen that when the current sources are well degenerated ($I_{tail} R_5 \gg V_T$), current mismatch is mainly determined by resistor and transistor α_F mismatch. When there is little or no degeneration ($I_{tail} R_5 \ll V_T$), current mismatch is mainly determined by transistor I_S mismatch. Resistor and α_F mismatch are much smaller than I_S mismatch in reality. This means that choosing a large value for R_5 is advantageous for current mismatch. Little or no data about resistor and transistor matching in QUBiC1 is available, but it can be assumed that resistor mismatch ranges from $\pm 0.1\%$ to $\pm 2\%$ and α_F mismatch is in the $\pm 0.1\%$ range for NPN-transistors.
The voltage space for the current sources in the multi-tanh circuit is about $1.5V$. The transistor needs a collector-emitter voltage V_{CE} of about $0.85V$. This leaves about $0.65V$ for the resistor, which results in a resistor value of $15k\Omega$ for a current of $40\mu A$. The precise bias voltage will be determined later. Figure 4.4 shows the delivered current I_{tail} as a function of the voltage V_C at the collector of the current source transistor. When the current source is given a small voltage space ($< 0.85V$), it does not function properly. When the voltage space is large enough, the delivered current I_{tail} is almost independent from V_C. The output impedance in this area is over $10M\Omega$. Table 4.3 summarizes the specifications of the current source, assuming it is well-biased.

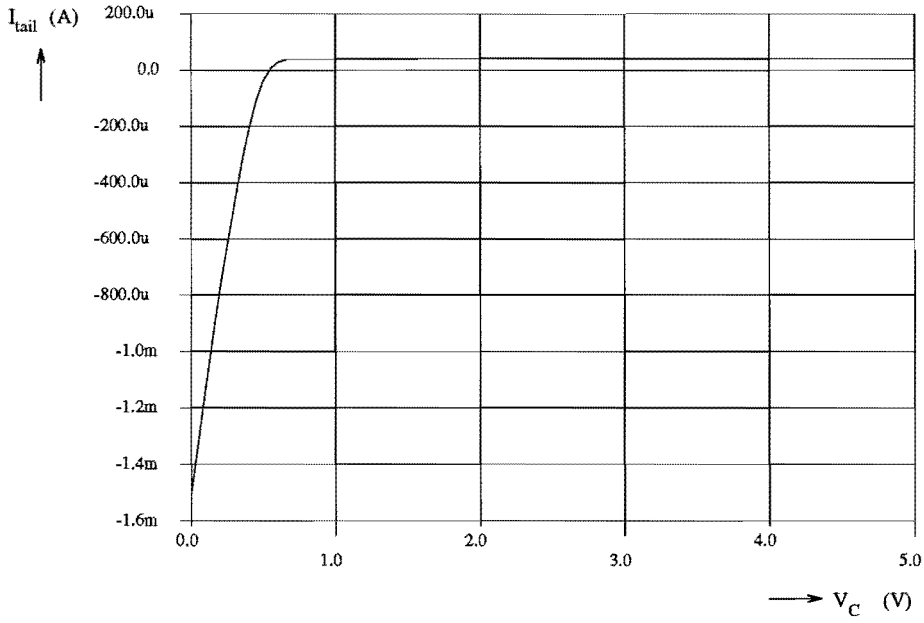

Figure 4.4: *Current source output current as a function of voltage drop*

Table 4.3: *Tail current source specifications*

Property	Symbol	Value
Output current	I_{tail}	$40\mu A$
Output impedance	R_0	$> 10M\Omega$
Required voltage space	V_C	$\geq 0.85V$

4.4 Tail current bias circuit

In the previous section the implementation of the tail current source was described. To generate a constant current, this current source has to be biased with a constant bias voltage. This section will describe the implementation of the circuit which provides this bias voltage. The most important demands on this circuit are:

- Low supply voltage dependence. The sensitivity of the generated bias voltage to (moderate) variations in supply voltage has to be small. This means that the current, generated by the current sources, will remain constant, even when the supply voltage varies $\pm 10\%$.
- Low temperature dependence. The same goes for temperature variations. Usually, the bias voltage depends on one or more base-emitter voltages. Because this voltage

is dependent on temperature, the bias voltage will also be.

- Usage of NPN-transistors only. PNP-transistors in QUBiC1 are very limited and thus only NPN-transistors should be used in this circuit.

The simplest circuit to generate a bias voltage uses a diode and a resistor [3, 4]. The drawback of this method is that the generated bias voltage is very sensitive to variations in temperature and supply voltage. To decrease this sensitivity, the bias circuit of figure 4.5 can be used [2].

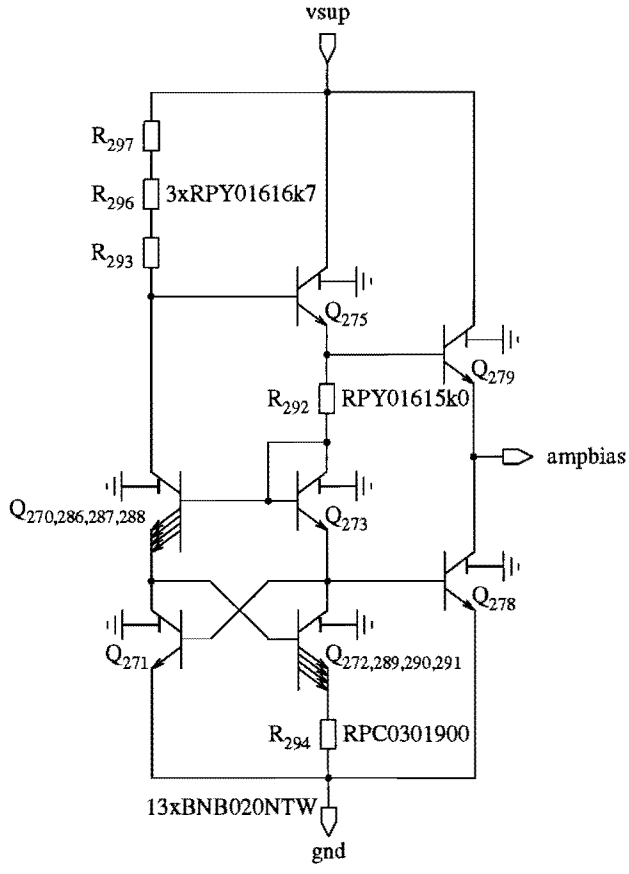

Figure 4.5: *Bias circuit for the differential pair current sources*

As can be seen, transistors $Q_{270,286,287,288}$, $Q_{272,289,290,291}$, Q_{271} and Q_{273} form a cross-coupled quad with a 1 : 4 emitter ratio. The current flowing through the right half of this quad, and thus through R_{294}, can be expressed as follows:

$$I_{R_{294}} = \frac{kT}{qR_{294}} \ln p, \tag{4.3}$$

where $p = 4$ is the emitter ratio of the quad. This current is independent of supply-voltage. The voltage at the collector of Q_{273} equals $V_{BE273} + V_{BE271}$, where V_{BE273} is

supply-voltage-independent because the current flowing through Q_{273} is supply-voltage-independent. The current flowing through Q_{271} is supply-voltage-dependent and this makes V_{BE271} also supply-voltage-dependent. To the collector voltage of Q_{273} a voltage equal to

$$V_{R_{292}} = \frac{R_{292}}{R_{294}} \frac{kT}{q} \ln p \tag{4.4}$$

is added by R_{292}. Now transistors Q_{278} and Q_{279} are added. Transistor Q_{278} is connected in parallel with transistor Q_{271} and thus forms a current mirror. This causes the currents through Q_{278} and Q_{279} to vary in exactly the same way as the current through Q_{271}. Because of this, the base-emitter voltage variation of Q_{279} will be the same as the base-emitter voltage variation of Q_{271}. This voltage variation across Q_{279} is subtracted from the voltage developed across Q_{271} and Q_{273} and therefore the voltage variation at the emitter of Q_{279} will be zero.
The voltage at the terminal named 'ampbias' will be equal to the base-emitter voltage of Q_{273} plus the voltage drop across resistor R_{292}. When $R_{294} = 1900\Omega$, $R_{292} = 15k\Omega$ and $R_{293} + R_{293} + R_{293} = 50k\Omega$, the bias voltage is such that the output current of the current sources equals $40\mu A$. Figure 4.6 shows the output current of a current source biased by the above circuit as a function of supply voltage V_{cc}. This current is not completely independent of the supply voltage, but the sensitivity to supply voltage variations is small.

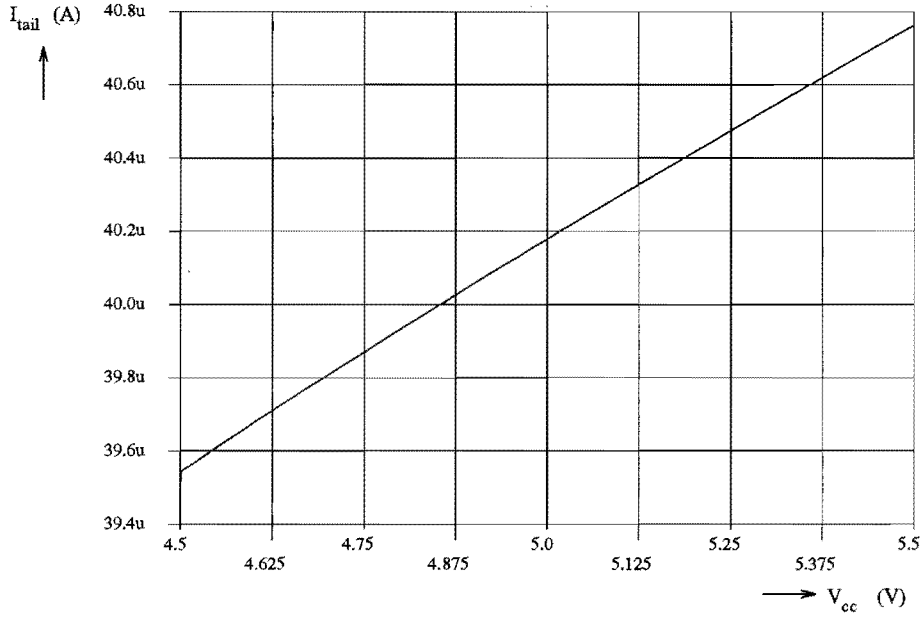

Figure 4.6: *Sensitivity of the bias circuit to supply voltage variation*

The slope of the graph in figure 4.6 around $V_{cc} = 5V$ is about $1.2\mu A/V$ $(3\%/V)$. When the output voltage $V_{ampbias}$ is adjusted to

$$V_{ampbias} = V_g + (n-1)\frac{kT}{q}, \tag{4.5}$$

where $V_g \approx 1.2V$ is the bandgap voltage of silicon and $n \approx 1.4$ is a constant, the output will show the parabolic temperature dependence equal to a bandgap reference source. For $T = 300K$, this would mean $V_{ampbias} \approx 1.21V$. Figure 4.7 shows the output current of the current source as a function of temperature.

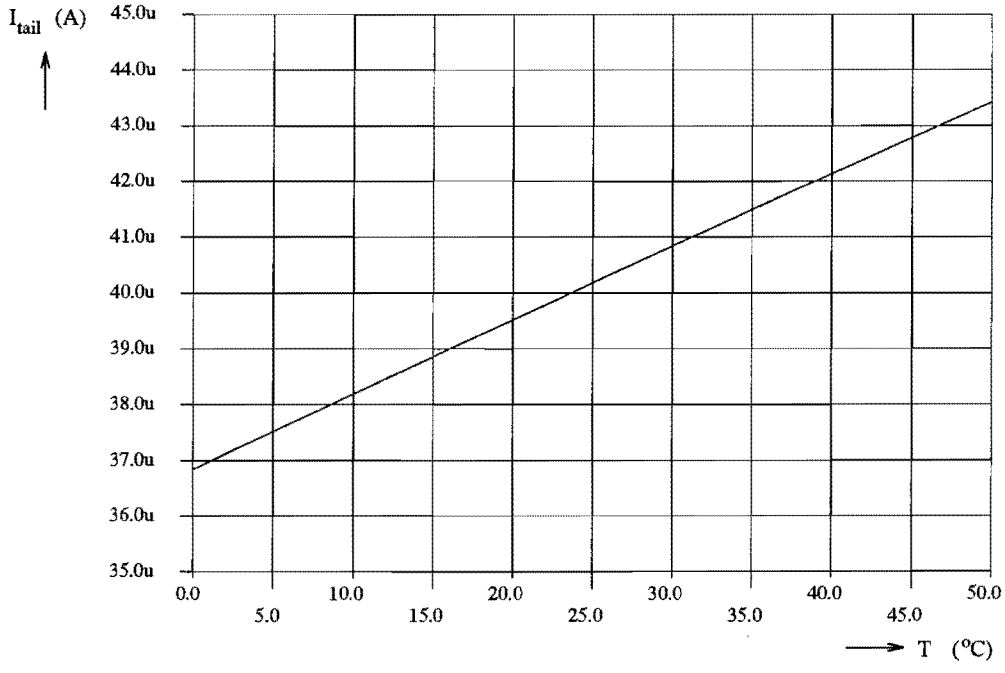

Figure 4.7: *Sensitivity of the bias circuit to temperature variation*

There is a small positive temperature dependence, because the bias circuit is not adjusted according to equation (4.5). However, this dependence is very small and will be tolerated. The slope of the graph around $T = 25°C$ is about $132nA/°C$ $(0.3\%/°C)$.
The power consumption of the circuit, operating at $V_{cc} = 5V$, was found to be $650\mu W$. Table 4.4 summarizes the properties of the bias circuit driving 32 current sources. The power consumption figure does not include the power consumption of these 32 current sources.

Table 4.4: *Tail current bias circuit specifications*

Property	Symbol	Value
Power supply sensitivity	$S_{V_{cc}}^{I_{tail}}$	$3\%/V$
Temperature sensitivity	$S_T^{I_{tail}}$	$0.3\%/°C$
Power consumption	P	$650\mu W$ @ $5V$

4.5 Input ladder

The input ladders have to take care of generating 32 equidistant voltages, related to the input voltage, with a distance which is variable between $0V$ and about $30mV$. Because the multi-tanh circuit is completely differential, there will be two input ladders. Figure 4.8 shows the implementation of these input ladders.

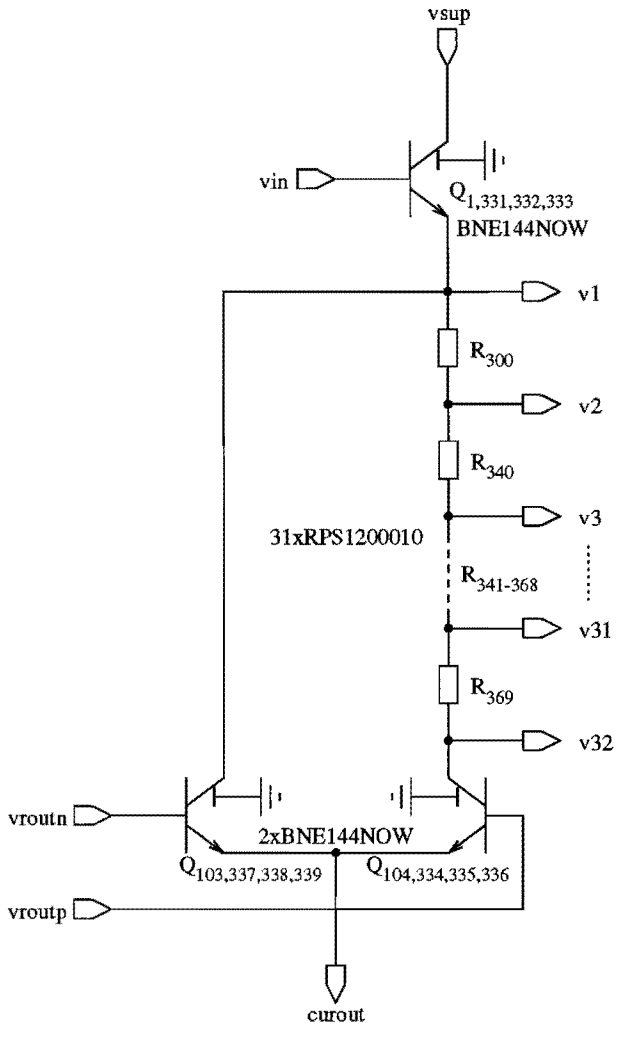

Figure 4.8: *Implementation of the input ladder circuit*

The input signal is buffered by an emitter follower. The voltage at the emitter of the four parallel transistors $Q_{1,331,332,333}$ will follow the input voltage at terminal 'vin'. The voltage difference will be one $V_{BE}(\approx 0.8V)$. The emitter is loaded with a resistor ladder consisting of 31 equal resistors with value R_{ladder}. When there is no current flowing through the ladder, the tap voltages at the terminals marked 'v1' through 'v32' will be equal. When a current I is flowing through the ladder, each resistor will have a voltage IR_{ladder} across it. Because the current through all resistors is equal and also all resistors have the same value,

the voltage drops across all resistors will be the same. In this way, a series of equidistant voltages

$$V_{vi} = V_{vin} - V_{BE} - (i-1)IR_{ladder} \tag{4.6}$$

is obtained. The differential pair consisting of fourfold transistors $Q_{103,337,338,339}$ and $Q_{104,334,335,336}$ takes care of routing the constant current supplied at the terminal marked 'curout' either through the ladder or passed the ladder, depending on the differential voltage between the terminals marked 'vroutp' and 'vroutn'. The offset voltages are now controllable by the voltage $V_{vroutp} - V_{vroutn}$. Note that the current through the emitter follower transistor is constant. This guarantees optimal operation of the input buffer. Figure 4.9 shows the 32 output voltages as a function of $V_{vroutp} - V_{vroutn}$ for a constant value of V_{vin}.

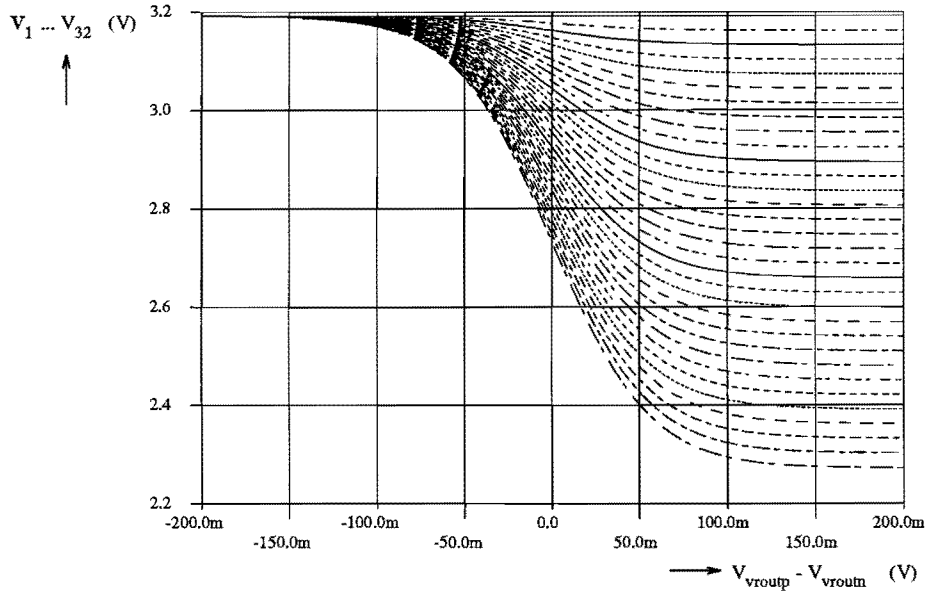

Figure 4.9: *Ladder output voltages as a function of routing voltage*

From each terminal 'v1' ... 'v32', the base current for the belonging differential pair transistor is drawn. This current is not constant. It is in the range $0 \ldots \frac{I_{tail}}{\beta_F}$ and depends on the actual collector current distribution in the differential pair. The base currents will flow through the resistor ladder. Through the top resistor, R_{300}, all 32 base currents will flow. When the value R_{ladder} of the ladder resistors is too large, the base currents will cause too large a disturbance in the voltages according to the series of equation (4.6). However, when R_{ladder} is small, the ladder current I has to be large to obtain the wanted maximum offset of about $30mV$, which will result in large power consumption.
From simulations, a value of 10Ω, together with a maximum tail current of $3mA$ was found to be a good compromise. This relatively large current implies the use of large transistors. Each transistor was implemented by four parallel BNE144NOW transistors. Because of the low value of the resistors, only metal and polysilicon resistors are applicable. The metal

resistors would be very large, because the sheet resistance is only $125m\Omega$/square. The width of such a resistor would have to be considerable to prevent electro migration. A 10Ω resistor would need a space of approx. $400\mu m \times 20\mu m$. Polysilicon has a sheet resistance of 8Ω/square, which yields a resistor of 1.25 squares. The chosen resistor has a width of $12\mu m$ and is called RPS1200010.
Finally, table 4.5 lists the most important properties of the input ladder circuit. The power consumption is independent of the adjusted offset voltage, because the ladder current is simply rerouted. The input impedance was determined by looking at the change in input current caused by a change in input voltage. As expected from this emitter follower configuration, the input impedance is high, which is an advantage when several stages are cascaded.

Table 4.5: *Input ladder circuit specifications*

Property	Symbol	Value
Input impedance	R_i	$1.2M\Omega$
Ladder current	I_{ladder}	$3mA$
Total ladder impedance	R_{total}	310Ω
Power consumption	P	$15mW$ @ $5V$

4.6 Ladder current sources

To supply the ladders with a $3mA$ current, the same type of degenerated current source is used as for the differential pairs. However, in this implementation, the transistor is larger because of the large collector current. The degeneration resistor can have a smaller value because the current flowing through it is larger. In figure 4.10 the ladder current source is depicted.
The voltage drop across resistor R_8 will be $3mA \times 83\Omega \approx 250mV$, which means that the output impedance of the degenerated current source will be about 11 times larger than without degeneration. The resistor is a polysilicon one, which means that it has to be about 10 squares in area. The applied type of transistor is the same as in the input ladder. Because the current sources of both transistors will be biased by the same circuit, mismatch in the transistors and resistors will be the main cause of mismatch in the output currents. Transistor mismatch will be small because of the considerable emitter area. The same goes for the resistors. They are chosen to have a width of $9\mu m$ and a length of almost $94\mu m$. However, because of the cross coupling between the differential pairs and both input ladders (cf. figure 4.1), one of the input ladders has to be flipped on the layout, which causes the distance between the current sources to be quite large.

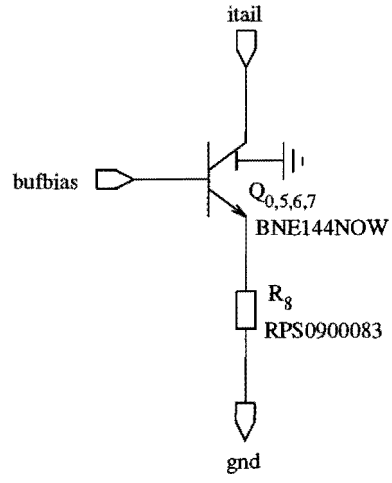

Figure 4.10: *Implementation of the tail current source*

Figure 4.11 shows the output current I_{tail} of the well-biased current source as a function of the voltage V_C at the collector of the transistor. It can be seen from this graph that the impedance of the current source is high again. The required voltage space is about $0.5V$. Table 4.6 lists the most important properties of the well-biased ladder current source.

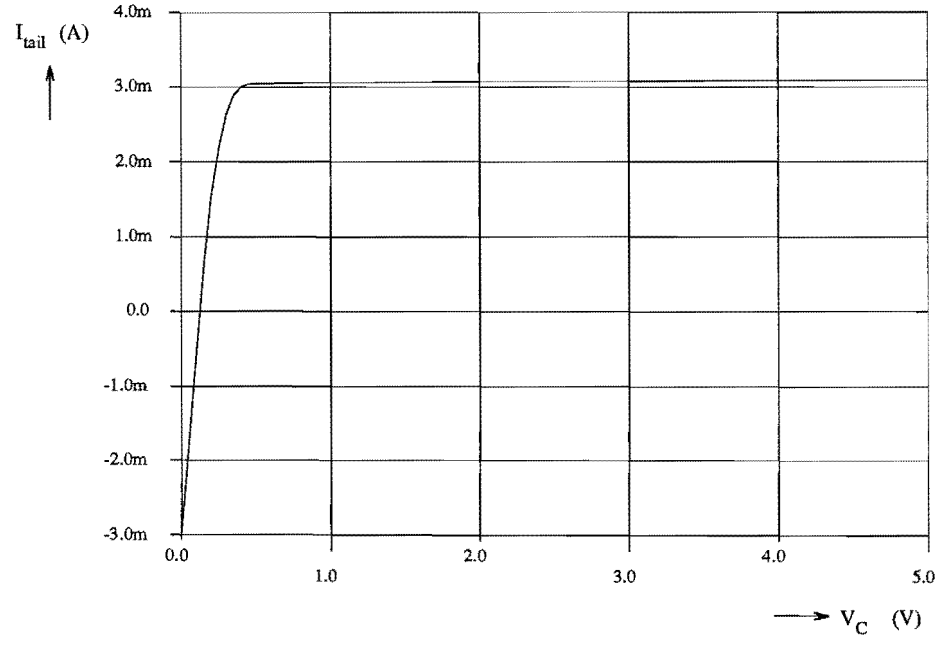

Figure 4.11: *Ladder current source output as a function of voltage drop*

Table 4.6: *Ladder current source specifications*

Property	Symbol	Value
Output current	I_{tail}	$3mA$
Output impedance	R_0	$80k\Omega$
Required voltage space	V_C	$\geq 0.5V$

4.7 Ladder current bias circuit

After some adjustments, the same biasing circuit as for the differential pair current sources can be used. Adjustments are necessary because the currents in the biasing circuit are larger and because the bias voltage is different. The used type of transistor is the BNF024NOW. Instead of putting four of these in parallel to obtain a 1 : 4 emitter ratio, one transistor of type BNF096NOW was used. The resulting circuit is depicted in figure 4.12.

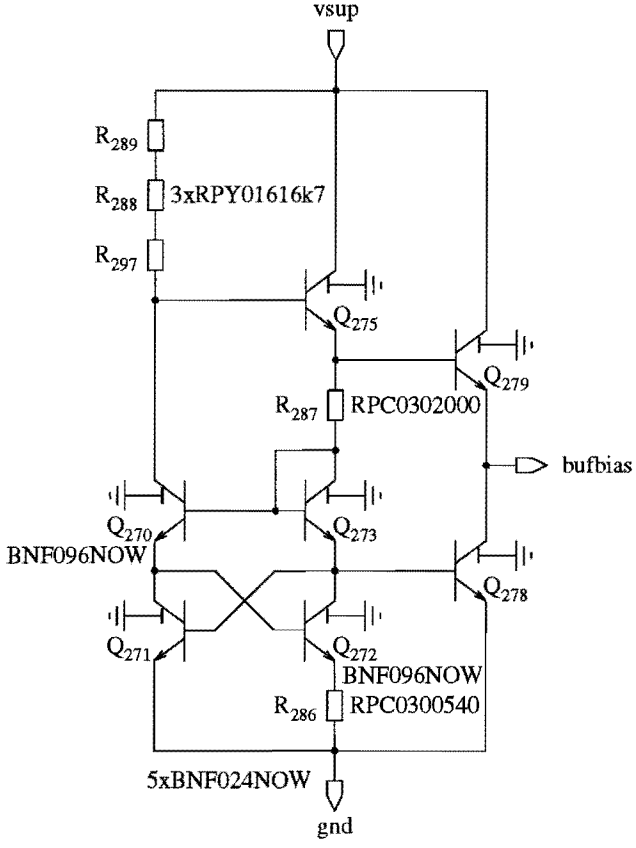

Figure 4.12: *Bias circuit for the ladder current sources*

The supply voltage dependency of the output current is shown in the graph of figure 4.13. The slope of the graph around $5V$ is $120.6\mu A/V$ $(4\%/V)$.

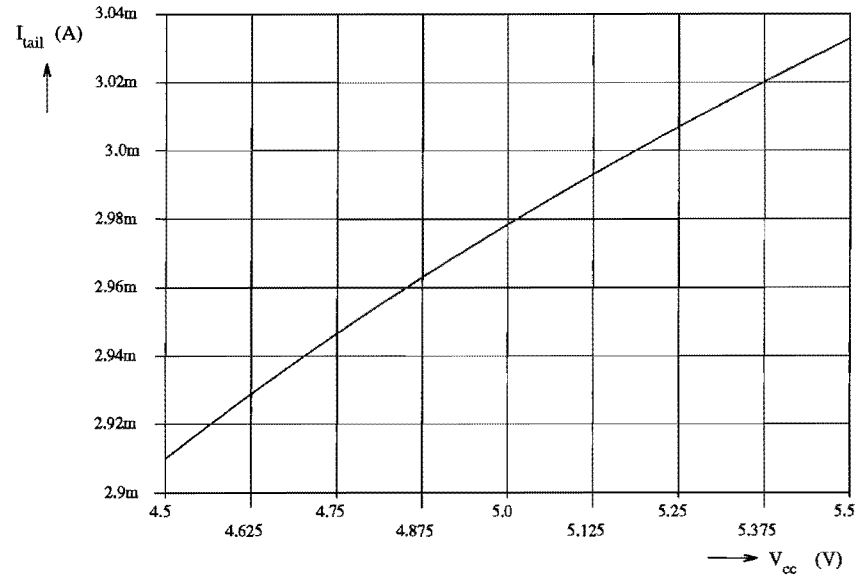

Figure 4.13: *Sensitivity of the bias circuit to supply voltage variation*

The sensitivity of the output current to temperature changes is also small. The slope of the graph in figure 4.14 around $T = 25°C$ is $5.2\mu A/°C$ $(0.2\%/°C)$.

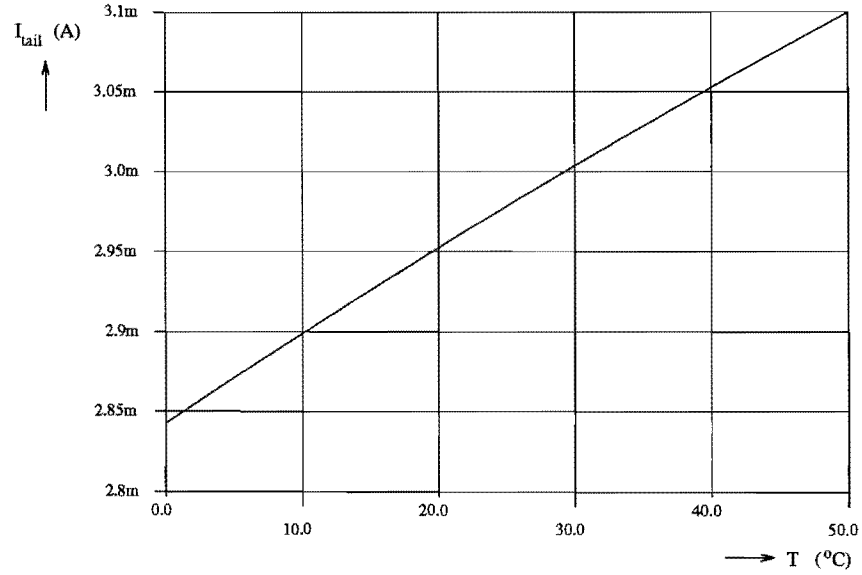

Figure 4.14: *Sensitivity of the bias circuit to temperature variation*

Table 4.7 lists the specifications of the ladder current source bias circuit. Power consumption does not include the input ladders.

Table 4.7: *Ladder current bias circuit specifications*

Property	Symbol	Value
Power supply sensitivity	$S_{V_{cc}}^{I_{tail}}$	$4\%/V$
Temperature sensitivity	$S_{T}^{I_{tail}}$	$0.2\%/^{\circ}C$
Power consumption	P	$1.5mW$ @ $5V$

4.8 Load circuit

The output of the coupled differential pairs is a differential current. Each of the 32 differential pairs is operated with a tail current of $40\mu A$. The total current thus is $32 \times 40\mu A = 1.28mA$. The common mode current will be half of this value, $640\mu A$ per output branch. The signal current will be superposed on this common mode current. To convert the differential output current into a differential output voltage, a pair of resistors is used. The advantage of resistors is that they can be made very linear, which will benefit the performance of the circuit. A disadvantage is that not only the signal current will be converted, but also the common mode current. This will cause a voltage drop across the resistors for which there has to be space. This limits the output voltage swing.

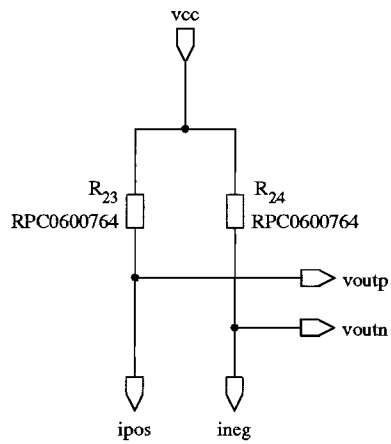

Figure 4.15: *Implementation of the load circuit*

Figure 4.15 shows the load circuit. The value of the resistors R_{23} and R_{24} is chosen such that the gain of the circuit (the transconductance multiplied by the resistance of the load) is variable between $0dB$ and $25dB$. For matching considerations, the resistors are $6\mu m$

wide. Mismatch between the two resistors will mainly cause a DC offset at the output. When several stages are cascaded, this DC offset will be amplified and might cause an overload in a later stage.

4.9 Complete multi-tanh circuit

Now that all separate blocks of which the multi-tanh circuit consists are filled in, simulations of the complete circuit can be performed. All simulations are performed using the 'onestage' circuit. The section is concluded with a summary of the specifications of the complete multi-tanh circuit.

4.9.1 DC performance

DC-analyses were performed for several values of the offset voltage between 0 and $60mV$. An ideal input voltage source was used. The common mode level at the input was $4.52V$. The routing voltage had a common mode level of $2.5V$. The common mode level at the output came to $4.52V$, which means that several stages can be cascaded without further adjustments. Figure 4.16 shows the differential output voltage as a function of the differential input voltage. The values of the differential routing voltage were respectively $-100mV$, $-50mV$, $-25mV$, $-10mV$, $0mV$, $10mV$, $25mV$, $50mV$ and $100mV$.

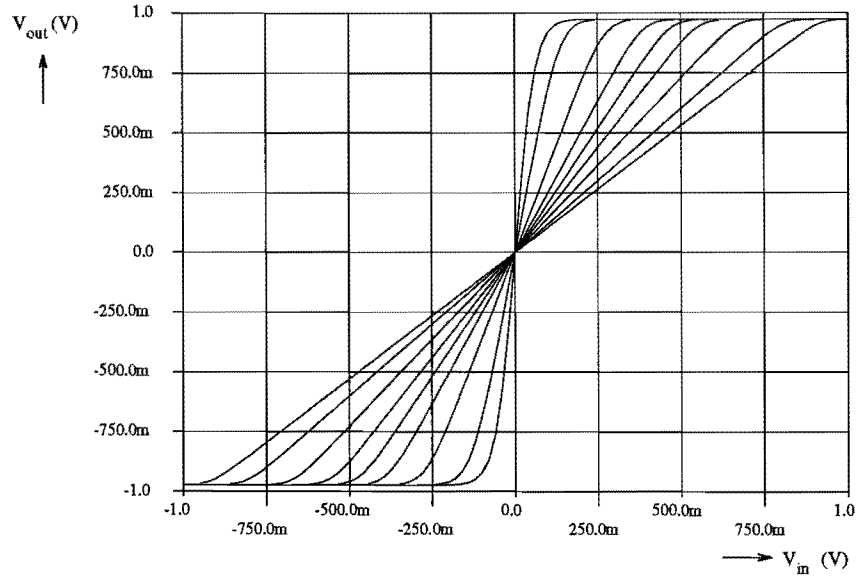

Figure 4.16: *Differential output voltage as a function of differential input voltage*

In figure 4.17 the differential gain is plotted as a function of differential input voltage. Here, the routing voltage was respectively $-100mV$, $-50mV$, $-25mV$, $-10mV$, $0mV$, $25mV$ and $100mV$, where $-100mV$ gives the highest gain ($16\times$) and $100mV$ results in unity gain.

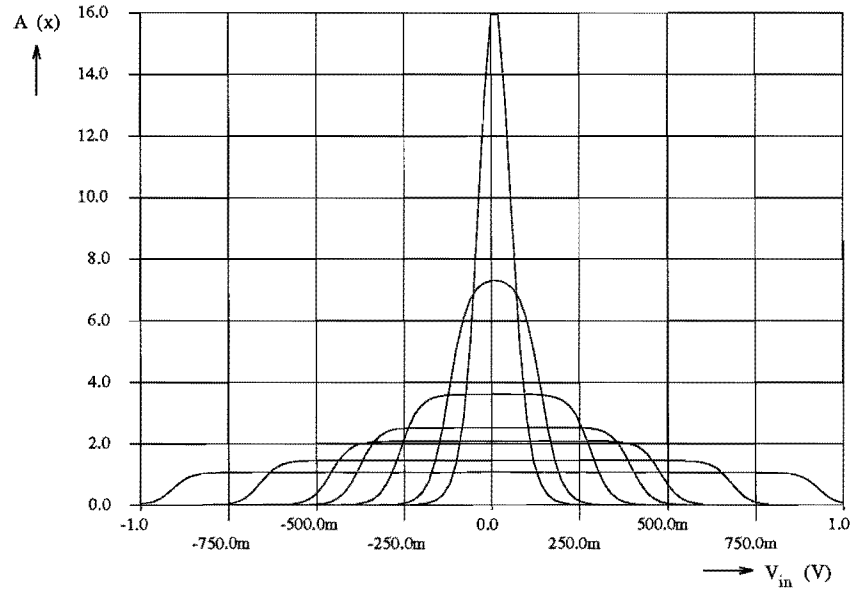

Figure 4.17: *Differential gain as a function of differential input voltage*

Here, the trade-off between gain and linear input range can be seen. In one of the next sections, the relation between gain and linear input range will be determined. The gain ranges from $1\times$ ($0dB$) to $16\times$ ($24dB$), so the gain range is $24dB$. Figure 4.18 shows the dependence between the routing voltage V_{rout} and the gain.

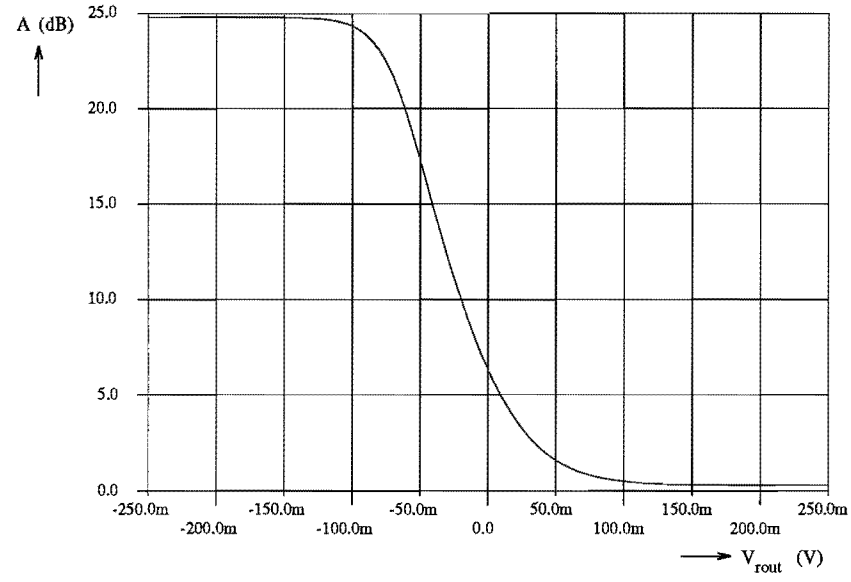

Figure 4.18: *Differential gain as a function of differential routing voltage*

4.9.2 AC performance

The gain of the circuit, determined in the previous section, will not be constant for all input frequencies. The combination of resistance and capacitance at the output will cause a time constant. The system will show low pass behaviour. When the time constant is low enough, the fall off frequency will be high. The frequency where the gain has fallen $3dB$ compared to the DC gain, has to be at least $60MHz$. Figure 4.19 contains a graph showing the gain as a function of frequency for several gain settings (routing voltage resp. $-100mV$, $-50mV$, $-25mV$, $0mV$, $25mV$ and $100mV$).

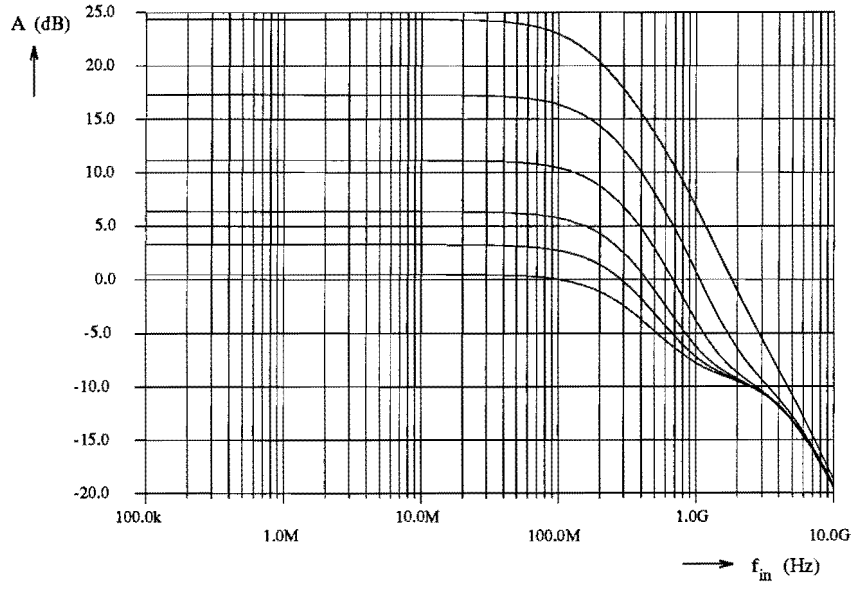

Figure 4.19: *Differential gain as a function of input signal frequency*

The $-3dB$-bandwidth increases with decreasing gain. For maximum gain, the bandwidth is still $160MHz$, which fulfills the demand of at least $70MHz$ bandwidth.

4.9.3 Harmonic distortion

An important figure of an amplifier is the harmonic distortion. Because the linear input range varies with varying gain, the intermodulation points (IP) will also be functions of gain. To determine the IP2 and IP3 point, a sine wave with an amplitude which does not overload the input will be used. The frequency of this sine wave is $50MHz$, the normal operating frequency of the amplifier. After performing a Fourier transform on the output signal, The amount of harmonic distortion can be determined and the IP2 and IP3 points can be calculated. Figure 4.20 shows the output IP3 as a function of differential gain. The IP2 point was higher than $175dBm$ for all gain settings and is not depicted.
To have less than $-70dB$ distortion at an output level of $190mV_{p-p}$, the IP3 point has to be at least $24.6dBm$ for all gain settings. As can be seen from figure 4.20, this target is not

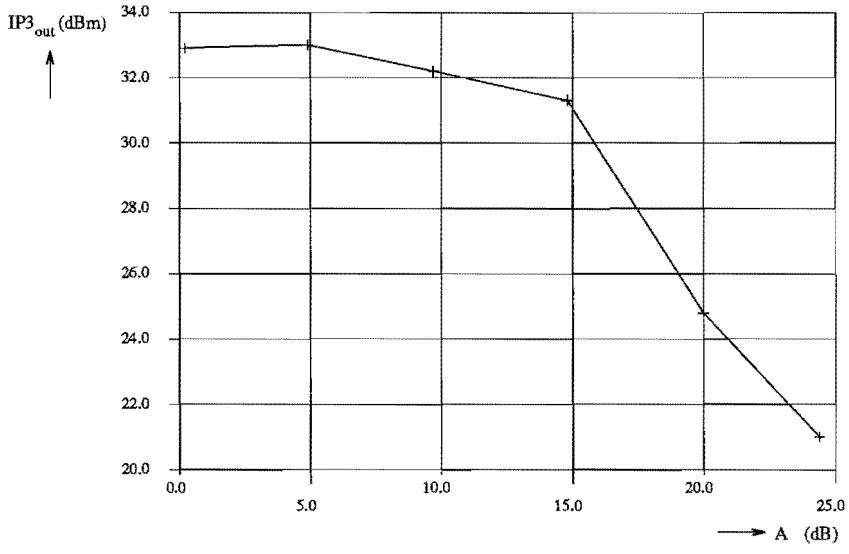

Figure 4.20: *Output IP3 as a function of differential gain*

reached for all gain settings. At high gain, the distortion level will be worse than $-70dB$, because the linearity of the amplifier is decreased to the level of a single differential pair. There are several ways to obtain a better linearity:

- Increasing the number of pairs. This will increase the maximum linear range and the gain range, but also the power consumption.
- Decreasing the gain range. In figure 4.20 can be seen that for low gain ($0dB$ to $20dB$), the performance is good. When the circuit is never set to high gain (offset voltages almost zero), the gain range is smaller but the performance is better.
- Using a smaller ladder impedance. Decreasing the value of the resistors in the ladders will lower the influence of the differential pair base currents. The power consumption will increase.

4.9.4 Noise performance

To perform a noise analysis in Pstar, a twoport has to be defined. The input port has to be terminated with a resistor. Pstar will now calculate the equivalent input noise current and output noise voltage spectral densities. Noise of the input resistor is included, unless this resistor is explicitly defined as a noisefree resistor. The input noise current source can be transformed to an input noise voltage source. The resulting configuration is depicted in figure 4.21.
Noise voltage sources $v_{n,in}$ and $v_{n,out}$ are related by the following equation:

$$v_{n,out} = Av_{n,in}, \tag{4.7}$$

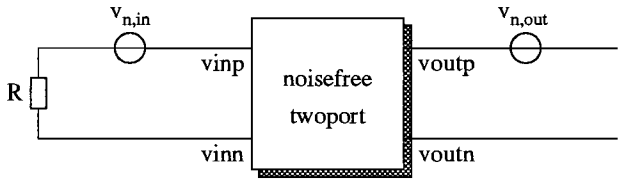

Figure 4.21: *Equivalent noisefree twoport with noise sources*

where A, the differential gain of the system, is a function of frequency. In figure 4.22 the rms-value of the equivalent input noise voltage as a function of frequency is plotted. As can be seen, when the system is adjusted to minimum gain, the noise voltage is maximal.

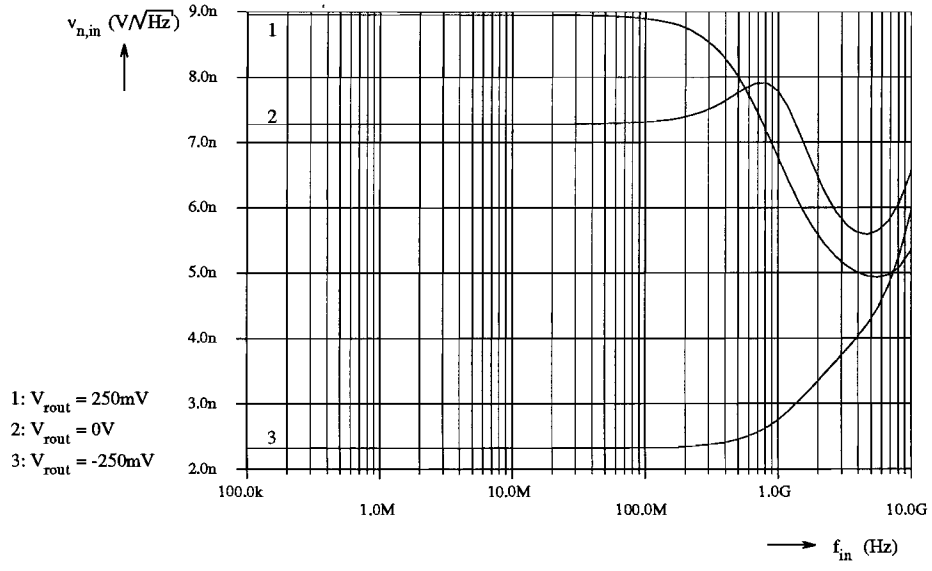

Figure 4.22: *Equivalent input noise voltage as a function of frequency*

When these graphs are multiplied by the gain function, the graphs of figure 4.23 appear. Now the noise voltage has the highest value at maximum gain. However, the wanted signal will be amplified by the same gain function as the input noise voltage.
The total noise voltages $V_{n,in}$ and $V_{N,out}$ over the frequency band from 0 to $60MHz$ are stated in table 4.8 below. They were calculated by integrating the graphs of figures 4.22 and 4.23 over $f = 0 \ldots 60MHz$.

Table 4.8: *Total input and output noise voltages over* $60MHz$ *band*

V_{rout}	$V_{n,in}$	$V_{N,out}$
$-250mV$	$18.6\mu V$	$308.8\mu V$
$0mV$	$56.5\mu V$	$118.7\mu V$
$250mV$	$69.7\mu V$	$69.7\mu V$

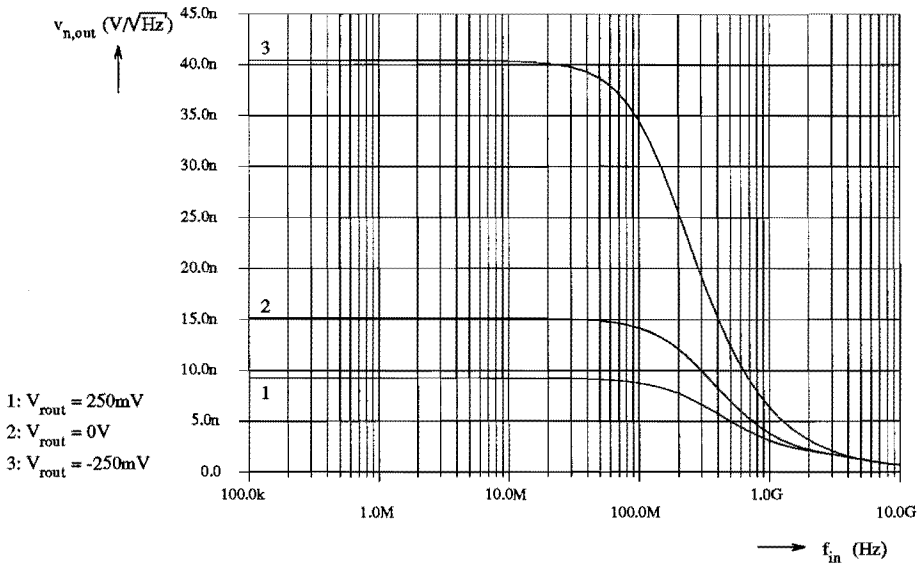

Figure 4.23: *Equivalent output noise voltage as a function of frequency*

The simulation results agree quite well with the results obtained in the previous section. The noise of the multi-tanh circuit is not good enough according to the demands imposed on the circuit in chapter 2. There are several solutions to this problem. The most promising one is increasing the size of the differential pair transistors. A drawback of this solution is that power consumption will increase.

4.9.5 Input and output impedance

Because the multi-tanh circuit will be part of a larger system, the differential input and output impedance are important figures. The input impedance will be quite large, because the input signal is directly buffered by emitter followers. Measuring the differential impedances was performed by analyzing the differential current as a function of the differential voltage at the input and output.

The input impedance is mainly determined by the 32 parallel differential pairs. From calculations, it can be shown that these 32 pairs can be replaced by one differential pair, degenerated with $4k\Omega$. The input impedance of the complete circuit will thus come to $\beta_F \times 4k\Omega \approx 400k\Omega$. The differential input impedance is two times this value, which is $800k\Omega$. Measurements showed a differential input impedance of $630k\Omega$ to $1.8M\Omega$, depending on the gain setting.

The differential output impedance is mainly determined by the two load resistors. Their value is 763Ω, which means the total differential output impedance will come to $2 \times 763\Omega \approx 1.5k\Omega$. Simulations showed the same value.

Table 4.9: *Differential input and output impedance*

Property	Symbol	Value
Differential input impedance	R_{in}	$\geq 630k\Omega$
Differential output impedance	R_{out}	$1.525k\Omega$

4.9.6 Power consumption

The power consumption of each of the individual blocks is known, so the total power consumption can easily be calculated. Table 4.10 states all power consumption figures.

Table 4.10: *Power consumption of the complete circuit*

Block	Number	Power	Total
Differential pairs with current sources	32	$200\mu W$	$6.4mW$
Bias circuit	1	$650\mu W$	$0.65mW$
Input ladders with current sources	2	$15mW$	$30mW$
Bias circuit	1	$1.5mW$	$1.5mW$
Total power consumption			$38.55mW$

From simulations of the complete circuit at $5V$ the power consumption was found to be $37.5mW$ almost independent of the gain setting and the input level. This means the amplifier can be classified as Class A.

4.9.7 Supply voltage dependence

Figure 4.24 shows the supply voltage dependence of the differential gain for three different gain settings (V_{rout} respectively $100mV$, $0mV$ and $-100mV$). The sensitivity to supply voltage variation is obviously very small.

4.9.8 Temperature dependence

Figure 4.25 shows that the sensitivity to temperature variation is the largest when the circuit is adjusted to high gain. When the temperature increases, the gain range decreases. When temperature changes from $-50^{\circ}C$ to $100^{\circ}C$, the gain range decreases about $2dB$.

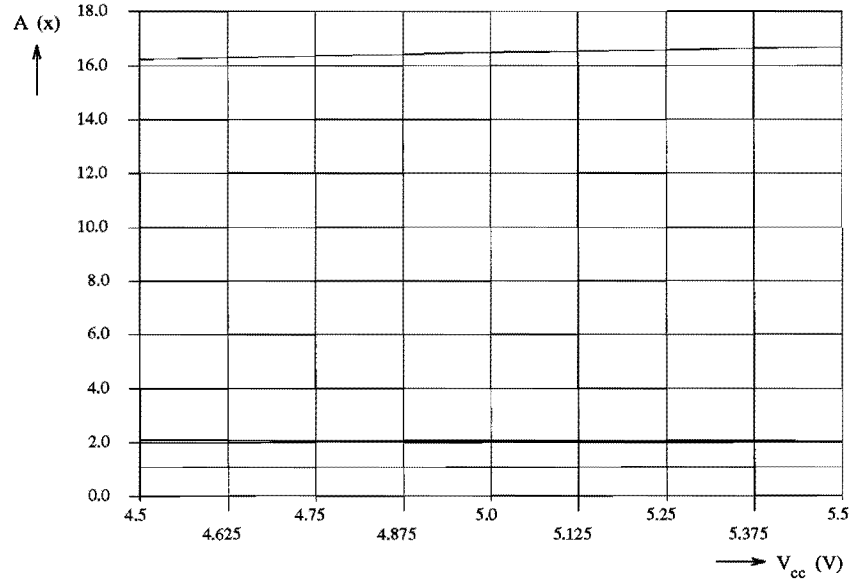

Figure 4.24: *Differential gain as a function of supply voltage*

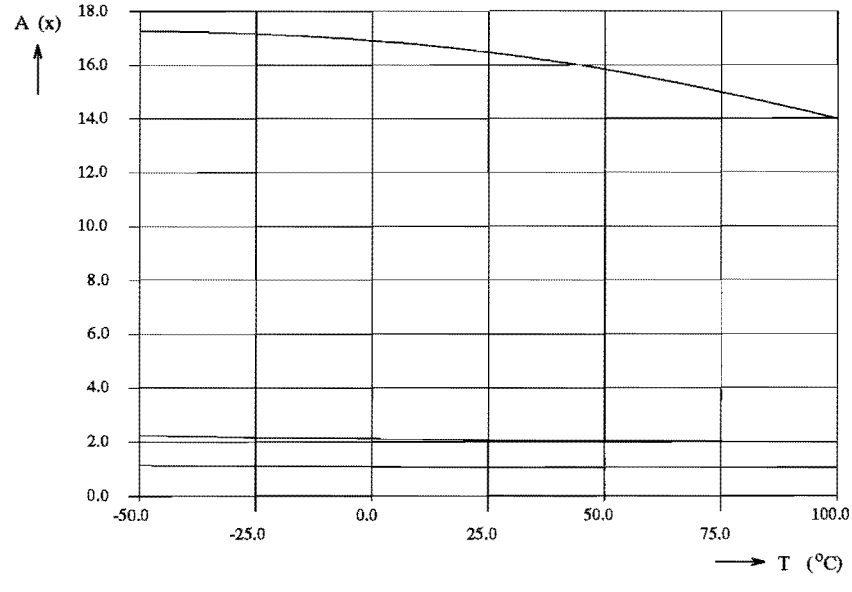

Figure 4.25: *Differential gain as a function of temperature*

4.9.9 Summary

Table 4.11 lists all the previously analyzed properties. When applicable, a minimum, typical and maximum value is specified for the property. Usually, a dependence on the gain setting exists. The previous sections make clear what is meant by minimal, maximal and typical for each property.

Table 4.11: *Summary of 'onestage' specifications*

Property	Symbol	Min.	Typ.	Max.	Unit
Differential voltage gain	A	0.2	6.3	24.4	$[dB]$
$-3dB$ Bandwidth	B_{-3dB}	160	250	300	$[MHz]$
Output IP3 $f_{in} = 50MHz$	$IP3_{out}$	21	33	33	$[dBm]$
Equivalent input noise voltage	$v_{n,in}$	2.4	7.3	9.0	$[nV/\sqrt{Hz}]$
Differential input impedance	R_{in}	$630k$	$1.6M$	$1.8M$	$[\Omega]$
Differential output impedance	R_{out}		$1.525k$		$[\Omega]$
Input common mode level	$V_{cm,in}$		4.52		$[V]$
Output common mode level	$V_{cm,out}$		4.52		$[V]$
Routing voltage common mode level	$V_{cm,rout}$		2.5		$[V]$
Gain sensitivity to supply voltage	$S^A_{V_{cc}}$			0.25	$[dB/V]$
Gain sensitivity to temperature	S^A_T			-0.011	$[dB/°C]$
Power dissipation @ $V_{cc} = 5V$	P		37.5		$[mW]$

4.10 Threestage circuit analysis

The multi-tanh circuit was designed for application in the TV-IF frontend. This application requires the use of three cascaded multi-tanh circuits. This section will describe some simulations on the 'threestage' circuit concerning AC gain, distortion and noise performance.

4.10.1 AC performance

Figure 4.26 shows the gain as a function of frequency for three different gain settings (varying from maximum gain to minimum gain). The three stages were adjusted to the same gain by connecting the routing voltage inputs of all stages together.
The bandwidth increases with decreasing gain and is at least $70MHz$, which is sufficient for TV-IF applications. Increasing the bandwidth can be achieved by increasing the tail current of the differential pairs. This will result in a higher power consumption.

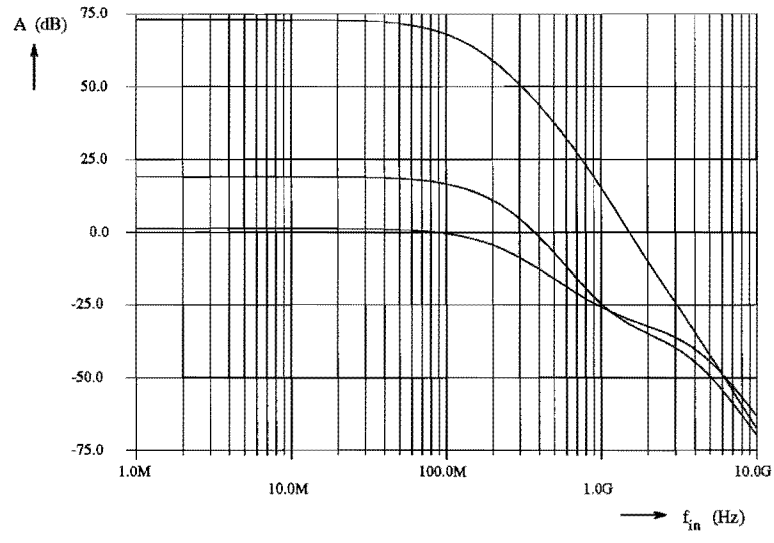

Figure 4.26: *Differential gain as a function of frequency for three gain settings*

4.10.2 Harmonic distortion

The amount of harmonic distortion will depend on the gain distribution amongst the three stages. When the first stage has a high gain, the second and third stages will have to cope with a considerable input level. To optimize harmonic distortion for all input levels, the last stages in the system should have the highest gain.

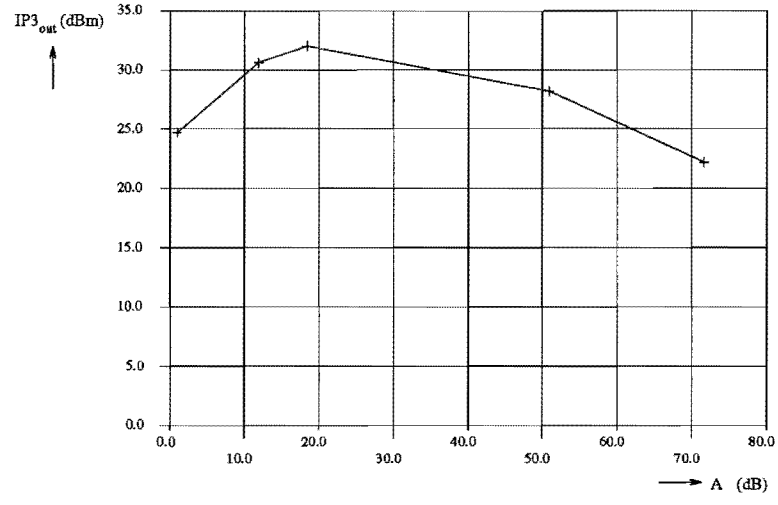

Figure 4.27: *Output IP3 as a function of differential gain for 'threestage'*

Figure 4.27 shows the output IP3 in dBm as a function of differential gain. All three stages were adjusted to the same gain by connecting their routing voltage inputs together. To meet the demand of a maximum 3^{rd} order distortion of $-70dBc$ for all gain settings, the output IP3 should be at least $24.6dBm$. Again, for high gains the circuit does not meet

this demand.

4.10.3 Noise performance

The noise performance of the circuit will also depend on the gain distribution amongst the three stages. Is is advantageous for the total noise to have high gain in the first stage. This is in contradiction with the requirements to achieve optimal distortion behaviour.
When all three stages are adjusted to minimum gain ($1\times$), the total equivalent input noise voltage source will be $\sqrt{3}\times$ the noise of each individual stage, which comes to a value of about $15.6nV/\sqrt{Hz}$. Noise simulations show about the same value.
When all three stages are adjusted to maximum gain ($24.4dB$), the noise of the first stage will be dominant. The total equivalent input noise voltage source will be about $2.4nV/\sqrt{Hz}$ in this case. Again, a noise analysis shows this is correct.
The total noise at the output benefits from the low pass filtering of the circuit. The $-3dB$-bandwidth of the system is about $70MHz$, so the high frequency components of the noise will be filtered out.

4.11 Conclusions

According to the results of the previously described analyses, the circuit performs quite well. However, some improvements will have to be made before it meets all demands.

- The distortion at high gains does not meet 10 bits accuracy. Possible solutions to this problem are described in section 4.9.3.
- The noise, generated by the circuit, is too high. The noise performance can be improved by using larger transistors in the differential pairs. However, as a consequence the power consumption will have to increase to maintain the same bandwidth. When several stages are cascaded, making the gain of the first stages higher than the gain of later stages will improve the overall noise performance.

Chapter 5

Layout design

This chapter will deal with the layout design of the previously described circuits. As mentioned before, four chips have been completed. There is a onestage chip, a twostage chip and two threestage chips. Of these last two, one has a separate power supply for each stage and the other has a combined power supply for the three stages. Plots of the core and of each of the four complete chips are included in appendix C.

5.1 The basic cell

5.1.1 Placement considerations

In the placing of the different parts of the multi-tanh circuit on the layout, the following considerations were made:

- The orientation of the differential pair transistors should be equal and they should be put as close to each other as possible to obtain the best possible matching.
- Neighbouring differential pairs and current sources should be put close to each other, again for matching considerations.
- The connection from the input ladder taps to the differential pair base terminals should be short to obtain a low series resistance. The connections should be equal in length and width for all differential pairs.
- Connecting the differential pair collector terminals should be easy. Crossing the input leads with the output leads should be prevented.
- Substrate contacts should be distributed symmetrically around the most sensitive part of the circuit, in this case the differential pairs.
- The ladder current sources should be put close to each other. Because of the considerable base current, the biasing leads to both ladder current sources should be equal in length and width to prevent an asymmetrical voltage drops across these leads.

- Low-impedant supply voltage leads should be easily reachable for all parts of the circuit.

Keeping these considerations in mind, the floorplan of figure 5.1 was designed. The major problem was layouting the input ladders. Because of the cross coupling between the input ladders and the differential pairs, one of the ladders had to be flipped. A consequence is that the distance between the input transistors of both ladders becomes very large. This is a disadvantage for the matching. The ladder current sources were separated from the ladders and placed close to the biasing circuit.

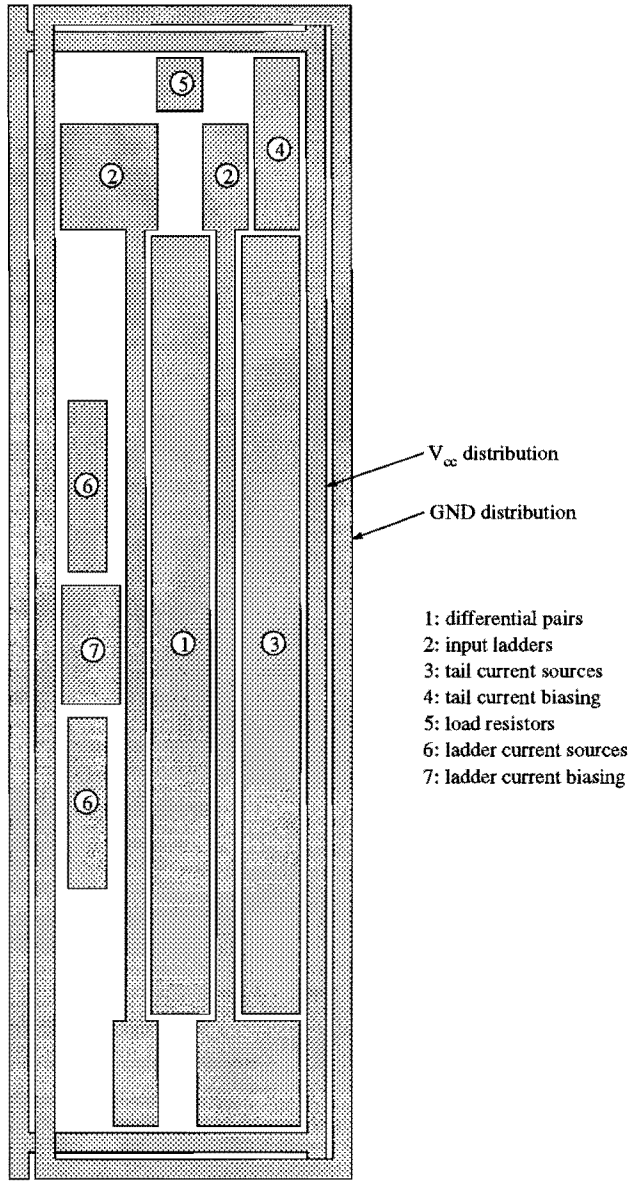

Figure 5.1: *Floorplan of the multi-tanh cell*

5.1.2 Power supply distribution

The complete core is surrounded by two rings to distribute V_{cc} and GND, the power supply nets. When two cells are placed such that the nets on the left side of one cell overlap the ones on the right side of the other cell, V_{cc} and GND of both cells are connected together automatically. This property is used in the chips 'twostage' and 'threestage'.

Where possible, power supply leads have been laid out in M2, the metal layer with the lowest resistance, to prevent voltage drop across these leads. Empty space inside the power distribution rings was filled with earth plane, connected to GND. Where possible, substrate contacts were put.

5.1.3 Input ladders

The input ladders consist of three main parts, viz. an input transistor, a resistor ladder and a routing differential pair. The resistor ladder consists of a strip of polysilicon (PS) with contacts to M0 at each tap. Current is injected into the ladder through contacts from M1 to M0 and from M0 to PS. In the beginning of the ladder, the current has a direction which is orthogonal to the chip surface. After some distance, this current will flow parallel to the chip surface. The piece of the ladder where the current is not flowing completely parallel to the chip surface will not show the same properties as the rest of the ladder. The same goes for the other end of the ladder.

To prevent these ends from causing deviations in the tap voltages, dummy resistors are put at both ends of the ladder. Figure 5.2 shows a perspective view of one end of the ladder.

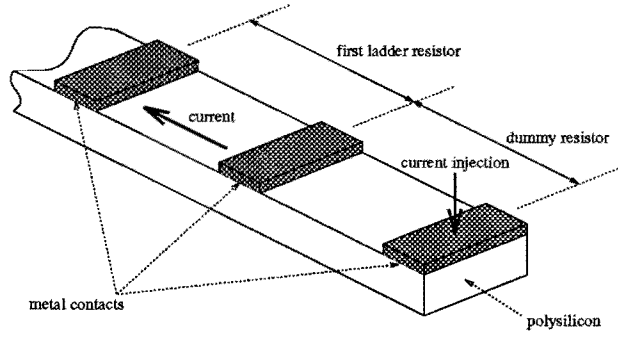

Figure 5.2: *Perspective view of the polysilicon ladder*

The current is injected at the end of the ladder. When it reaches the first real ladder resistor, its direction will have become parallel to the polysilicon strip. A small part of the current will flow out of each tap. Each "active" tap will be operating under the same conditions, which will improve matching of the generated tap voltages.

5.2 The four complete chips

With the previously described cell, four different chips were constructed. There is a chip which contains only one instance of the multi-tanh cell, one which contains two instances and two which contain three instances. The two chips which contain three cascades differ in the way the power supply is distributed. Chip 'threestage' has one pair of power supply clamps for all three stages. Chip 'threesep' has three separate pairs of power supply clamps. See appendix D for pinning information on these four chips.
Each chip has at least one pair of pins for the differential input, one pair of pins for the differential output and one pair of power supply pins. Further, per stage each chip has a pair of pins for the routing voltage and a set of bias leads. These bias leads can be decoupled or monitored externally. Also, an external bias voltage can be applied to these pins. Each chip has at least one extra set of supply voltage pins. Chip 'threesep' even has three extra supply voltage pins.
The layouts of the top levels of all four chips are included in appendix C. The numbers at the bonding pads correspond with the pin numbers of a DIL package. The active and total area of each of the four chips is listed in table 5.1. Also, the type of package is listed. The three chips in the DIP20 package are pin compatible.

Table 5.1: *Chip area and package of the four realized chips*

Chip name	Active area	Total area	Package
'onestage'	$0.15mm^2$	$1.5mm^2$	DIP20
'twostage'	$0.27mm^2$	$1.5mm^2$	DIP20
'threestage'	$0.40mm^2$	$1.5mm^2$	DIP20
'threesep'	$0.45mm^2$	$2.0mm^2$	DIP24

Chapter 6

Recommendations and conclusions

A study on the possibilities of implementing a voltage controlled amplifier with a high gain range and low distortion has been performed. Test versions of the designed circuit have been implemented in QUBiC1. At the time this report was finished, no measurements had been performed. About the designed and implemented circuit, the following conclusions can be stated:

- The circuit is very simple and very flexible in that it can be adapted to many operating conditions. By varying the number of differential pairs, the tail currents and the load resistors, the gain range and absolute gain can be adjusted.

- The harmonic distortion of the circuit is too high at high gain settings. For low gain settings, the circuit performs excellent with respect to harmonic distortion. Because of the fully differential design, even order distortion is almost absent, which makes odd order distortion dominant.

- The noise performance is not good enough, especially for low gain settings. There are however some possible solutions to this problem.

- Power dissipation is about $40mW$ @ $V_{cc} = 5V$ per stage, independent of the gain setting. Power supply voltage can be lowered, but this will limit the output voltage swing. The threestage amplifier consumes less than $120mW$ at a $5V$ supply.

- With the aforementioned power consumption, the $-3dB$-bandwidth of a threestage amplifier is about $70MHz$, which suffices for TV-IF applications.

- The active chip area in QUBiC1 of one stage is $0.15mm^2$. For a threestage amplifier the active area is $0.4mm^2$.

- The dependence of the gain on the differential gain control voltage is tanh-like. If necessary this dependence can be linearized with an appropriate converter.

There are several recommendations to make for further improvements. The exact application of the circuit will determine the final implementation. The work done so far is part of a research project which investigates digitalization of TV and radio receivers. The following points might be useful to investigate in the future:

- By using differential pair transistors with a higher β_F or by decreasing the differential pair tail currents, the base currents will be decreased. The ladder impedance can be increased, which will benefit power consumption.

- There are a number of measures which will improve harmonic distortion. The number of parallel pairs and thus the linear input range could be increased. However, this will not benefit power consumption. The gain range will increase. A second possibility is to avoid adjusting the circuit to maximum gain. Further possibilities are to decrease the input ladder impedance or to use the circuit for smaller input levels.

- By using transistors with larger emitter areas in the differential pairs, noise performance can be increased. However, this will influence the AC performance and it might be necessary to increase the tail currents to keep the same bandwidth.

- To make the gain digitally controllable, the routing pair and the current source in the input ladder can be replaced by a current D/A-converter. The emitter follower transistor has to be provided with a small current (not flowing through the ladder) to keep it conducting for all gain settings. With a suitable decoder, the dependence of the gain on the digital input code can be made linear.

- By using an active load instead of the resistor pair, the signal current can be separated from the common mode current. The output current can be transformed to a voltage by a suitable I/V-converter. In this way, the maximum output voltage swing is not limited by the present voltage space. Maybe, the circuit can be provided with a current input, which would make I/V-converters between two cascades obsolete.

- BiCMOS technologies might offer possibilities to improve the overall circuit performance. Current sources which need a small voltage space can be implemented in NMOS. The active load can be composed of PMOS transistors. Maybe it is even possible to implement the differential pairs in NMOS. The advantage of this would be that the currents that have to be supplied by the input ladder will be much smaller. A disadvantage is that MOS transistors have worse matching capabilities than bipolar transistors.

- The gain of the circuit can also be adjusted by varying the tail currents (which can be achieved by changing the bias voltage). When the offset voltage between the differential pairs is kept constant, the linear input range will also be constant. A drawback is that the common mode current at the output will vary with gain. Another drawback is that because of the non-zero emitter resistance of the differential pair transistors, the offset will vary a little with tail current.

Overviewing the previous conclusions and recommendations, it can be stated that the multi-tanh architecture appears to be a promising approach to the implementation of linear variable gain amplifiers with a high gain range. The proposed circuit can be used as a starting point for further improvements. Measurements of the chip will have to confirm the result obtained by simulations so far.

Chapter 7

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Eindhoven, June 1994

Pieter van Lieshout

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Appendix A

Harmonic distortion

Consider the system of figure A.1 with input x, output y and 3^{rd}-order transfer function

$$y = a_0 + a_1 x + a_2 x^2 + a_3 x^3. \tag{A.1}$$

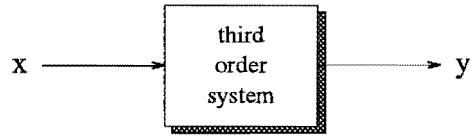

Figure A.1: *Third order system*

With two sine wave input signals at different frequencies ω_p and ω_q but with equal amplitudes p, that is

$$x = p\sin(\omega_p t) + p\sin(\omega_q t), \tag{A.2}$$

we get an output signal which also contains components at different frequencies than ω_p and ω_q due to second and third order effects. The output signal will contain the fundamentals

$$a_1 p(\sin(\omega_p t) + \sin(\omega_q t)), \tag{A.3}$$

where a_1 clearly is the gain of the system. The third order products, present in the output signal, are the third harmonics of both input components

$$\frac{1}{4}a_3 p^3(\sin(3\omega_p t) + \sin(3\omega_q t)) \tag{A.4}$$

and the cross products of the input components, of which the most important ones are

$$\frac{3}{4}a_3 p^3(\sin(2\omega_p t - \omega_q t) + \sin(2\omega_q t - \omega_p t)). \tag{A.5}$$

When the difference between ω_p and ω_q is small, the products from equation (A.5) will be close to the fundamentals. An important quality figure of the system is the level difference between the fundamentals and the cross products.

As can be seen from equation (A.3), the output level of the fundamentals will increase linearly with increasing input level. The level of the cross products however, is dependent on the 3^{rd} power of the input level. Converted to decibels, we get the graph of figure A.2. Here we can see that the first-order transfer has a unity slope and the third-order transfer has a slope equal to 3.

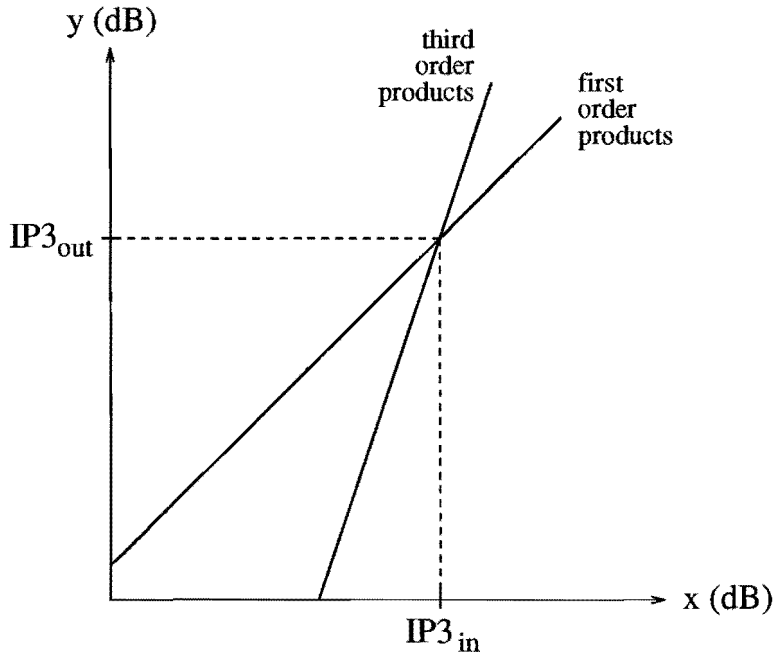

Figure A.2: *First and third order products versus input*

Definition of IP3

The two tone third order input intercept point $IP3_{in}$ is defined as the input level of two sine waves at different frequencies ω_p and ω_q but with equal amplitudes p which at the output produce third order products at $2\omega_p t - \omega_q t$ and $2\omega_q t - \omega_p t$ of the same level as the first order output components at ω_p and ω_q.

We can calculate $IP3_{in}$ from the transfer function by solving p from equations (A.3) and (A.5). We get

$$a_1 p = \frac{3}{4} a_3 p^3 \Rightarrow V_{IP3_{in}} = \sqrt{\frac{4a_1}{3a_3}}. \tag{A.6}$$

To obtain the third order output intercept point $IP3_{out}$, we have to multiply $IP3_{in}$ by the gain of the system. We then get

$$V_{IP3_{out}} = a_1 V_{IP3_{in}} = a_1 \sqrt{\frac{4a_1}{3a_3}}. \tag{A.7}$$

To calculate the third order harmonic distortion HD3 at a given input level from IP3 and vice versa, we can make use of the linearity of the transfer curves in figure A.2. In figure A.3 this is illustrated.

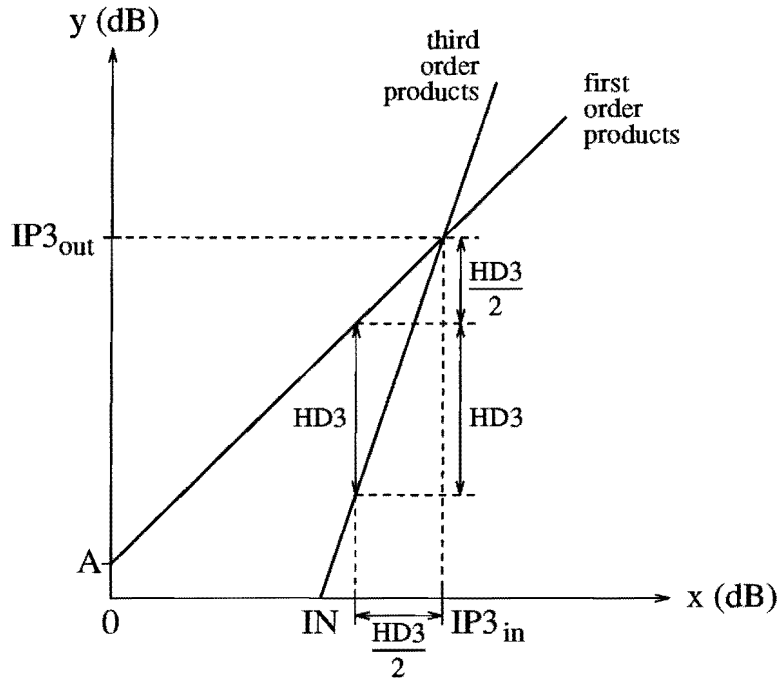

Figure A.3: *Relation between IP3 and HD3*

Notice that the distance between $IP3_{in}$ and V_{in} is $\frac{1}{2}$HD3. To calculate $IP3_{out}$ from a given V_{in} and HD3, the following formula can be applied:

$$IP3_{out} = IN + \frac{1}{2}HD3 + A, \tag{A.8}$$

with $IP3_{out}$, IN, HD3, and A, the gain of the system, all in decibels.

Appendix B

Circuit schematics

The following figures show the circuits from the Cadence library 'agc'.

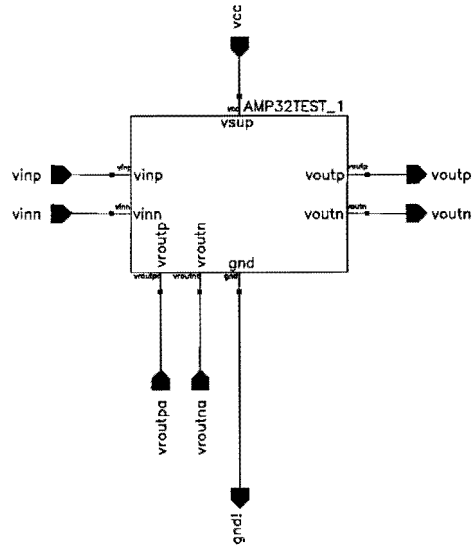

Figure B.1: *Top level schematic of 'onestage'*

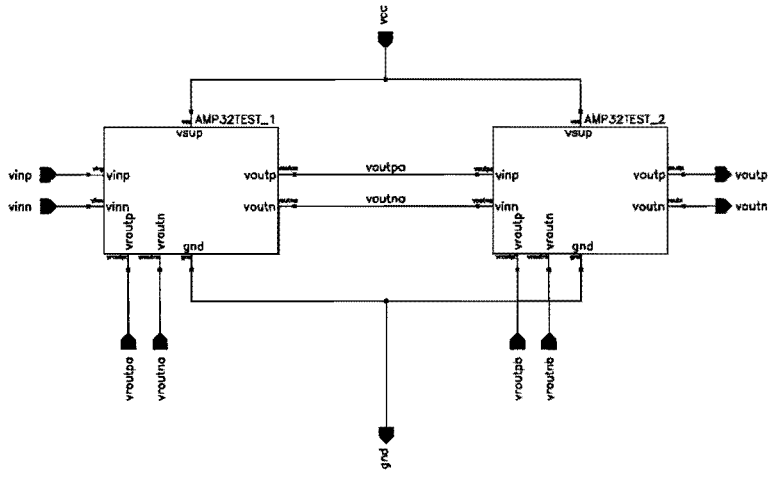

Figure B.2: *Top level schematic of 'twostage'*

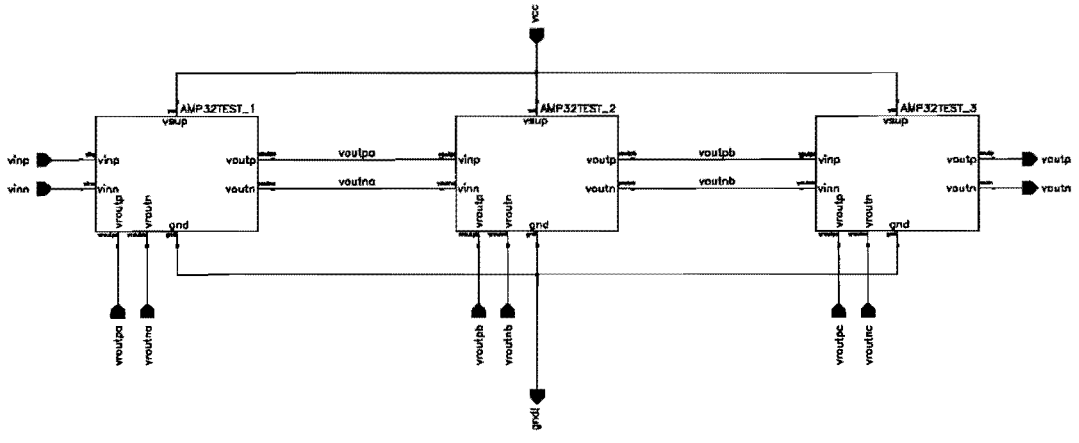

Figure B.3: *Top level schematic of 'threestage'*

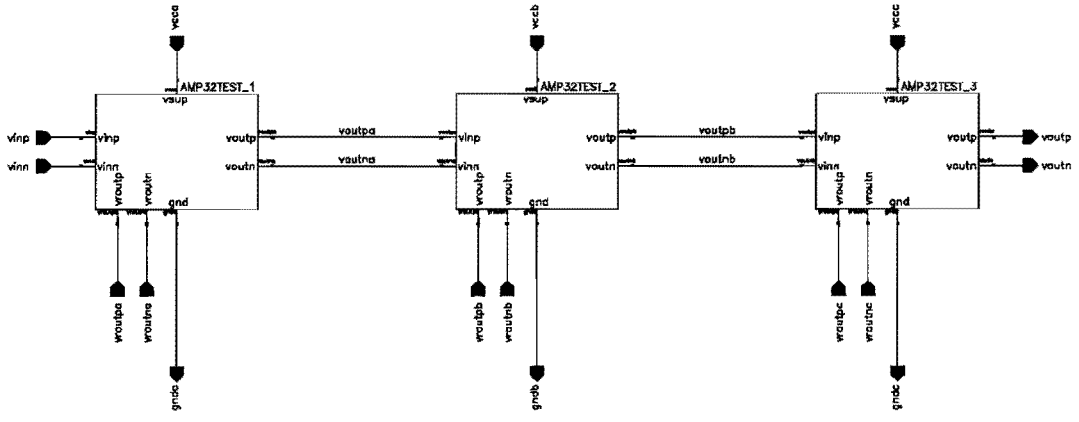

Figure B.4: *Top level schematic of 'threesep'*

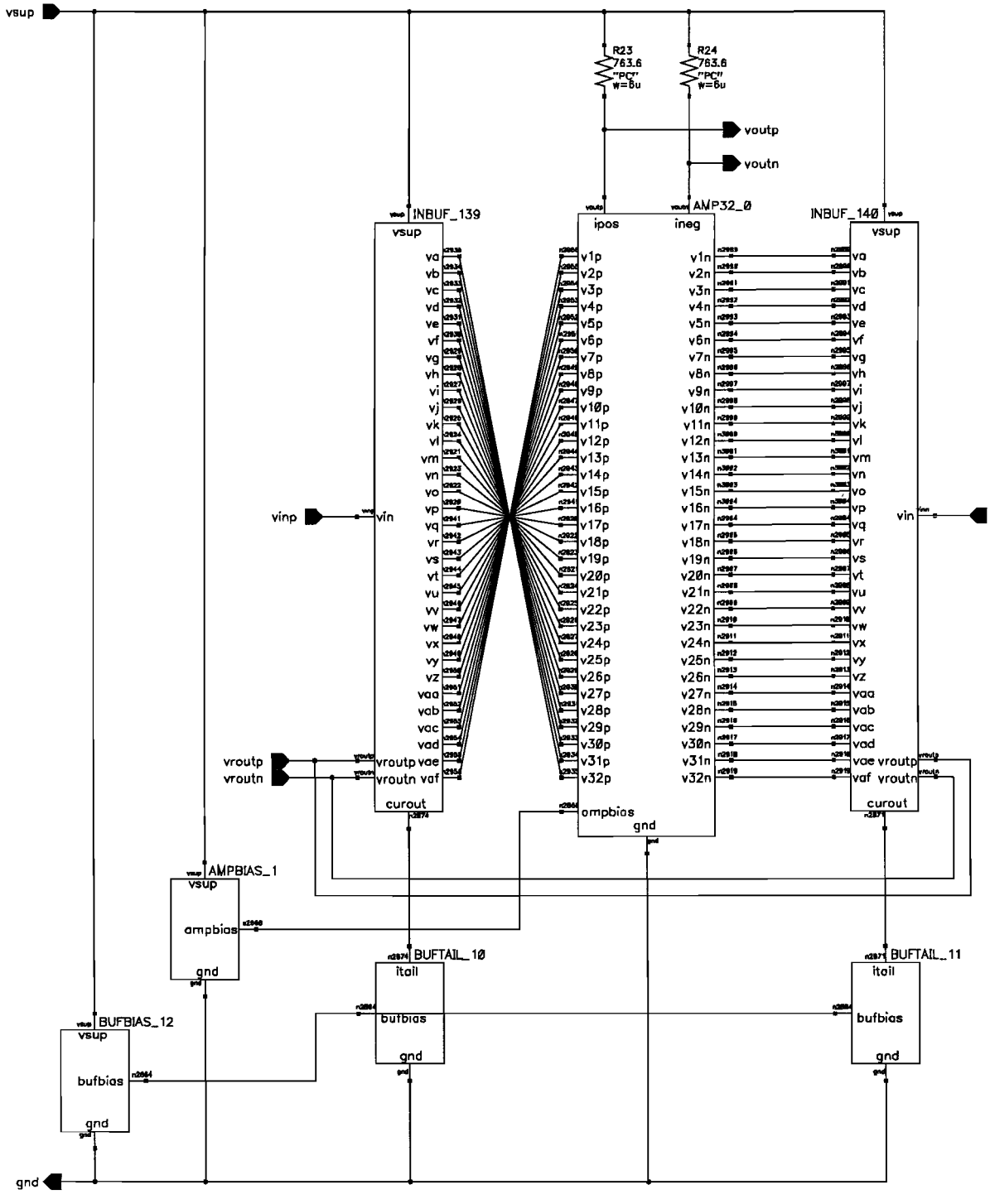

Figure B.5: *Multi-tanh circuit schematic*

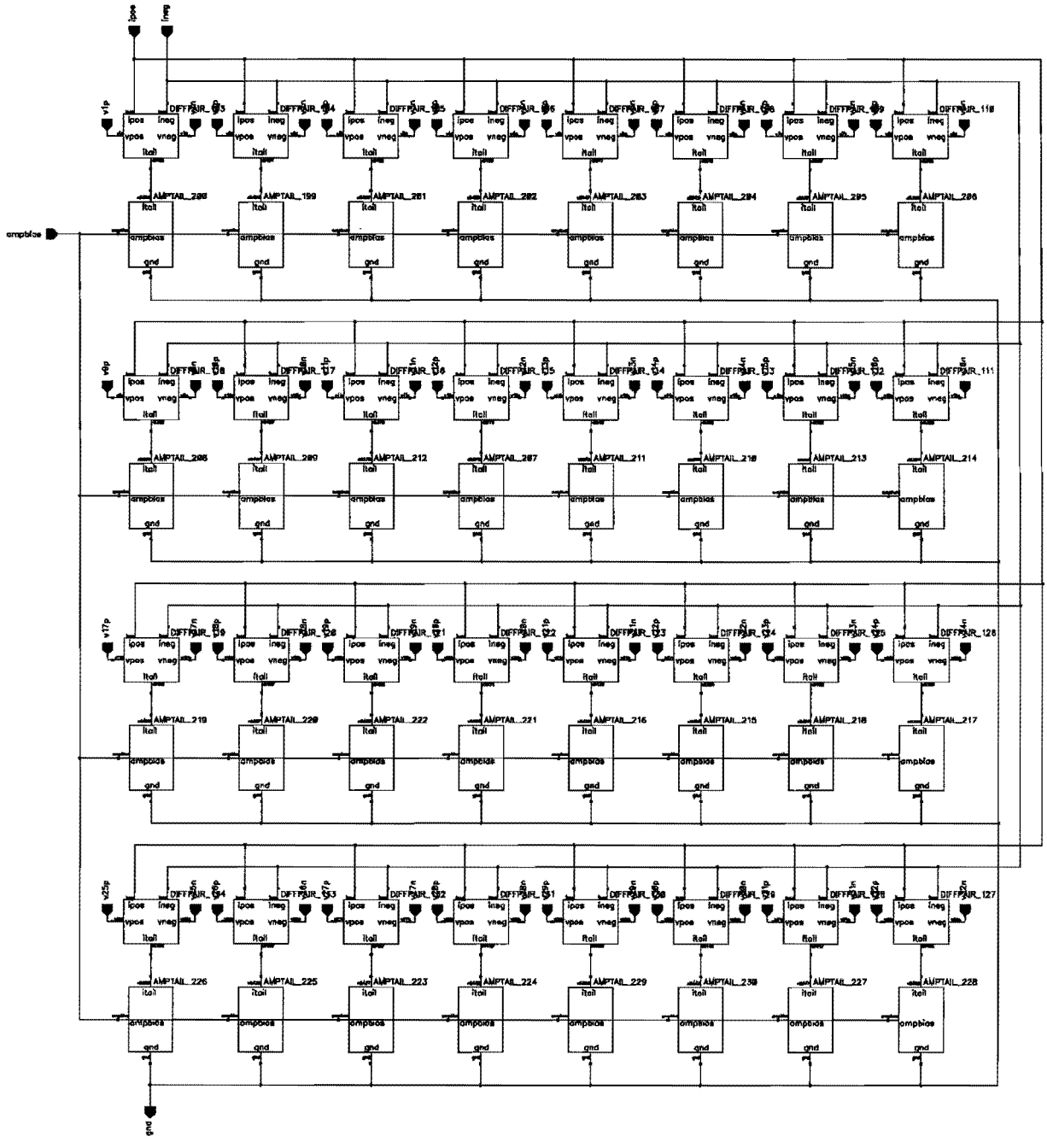

Figure B.6: *32 coupled differential pairs*

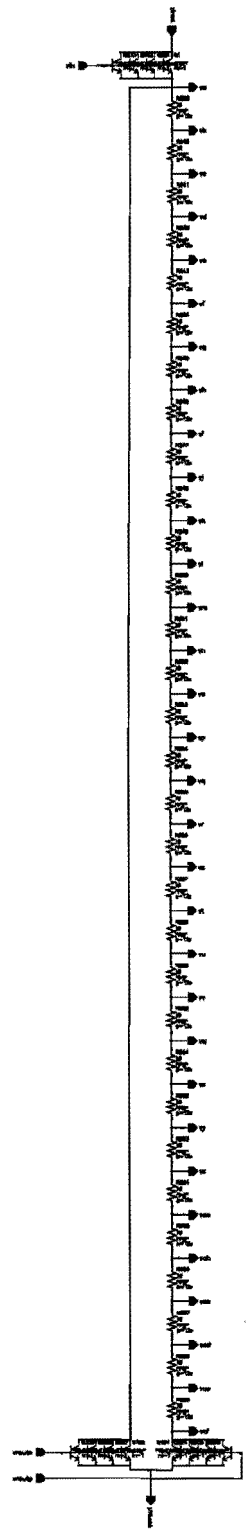

Figure B.7: *Input buffer with resistor ladder*

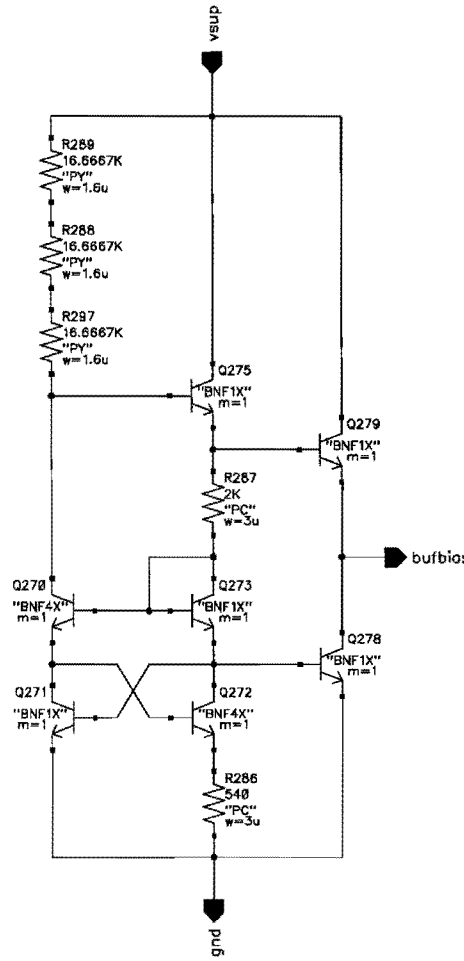

Figure B.8: *Bias circuit for ladder current sources*

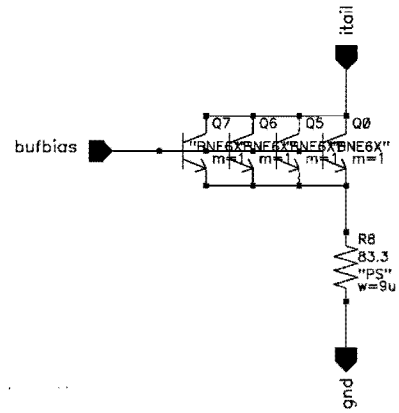

Figure B.9: *Ladder current source*

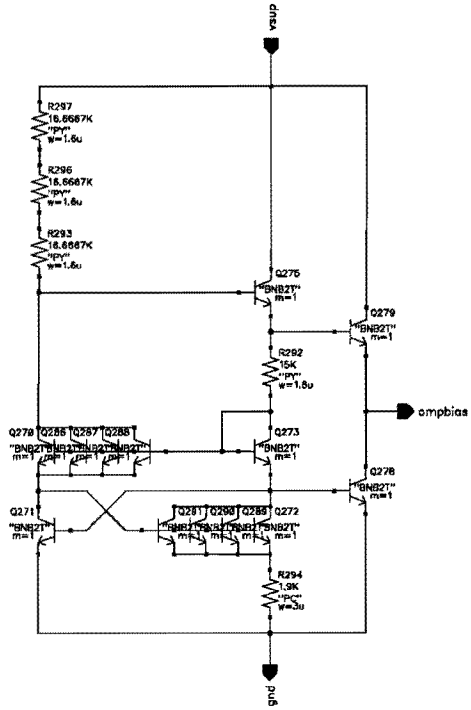

Figure B.10: *Bias circuit for differential pair tail current sources*

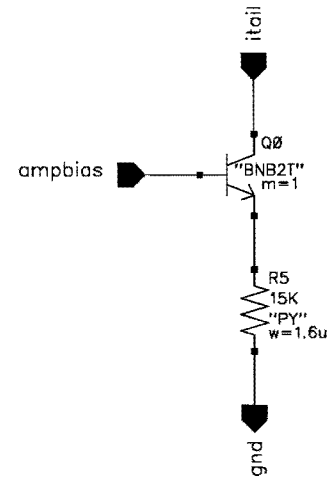

Figure B.11: *Differential pair tail current source*

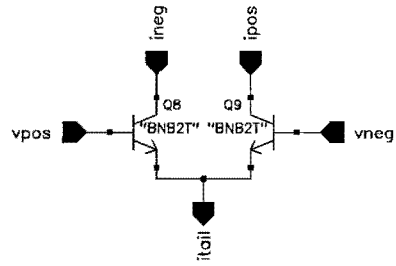

Figure B.12: *Differential pair*

Appendix C

QUBiC1 layouts

The following pages contain plots of the layouts of the multi-tanh cell and the chips 'one-stage', 'twostage', 'threestage' and 'threesep'.

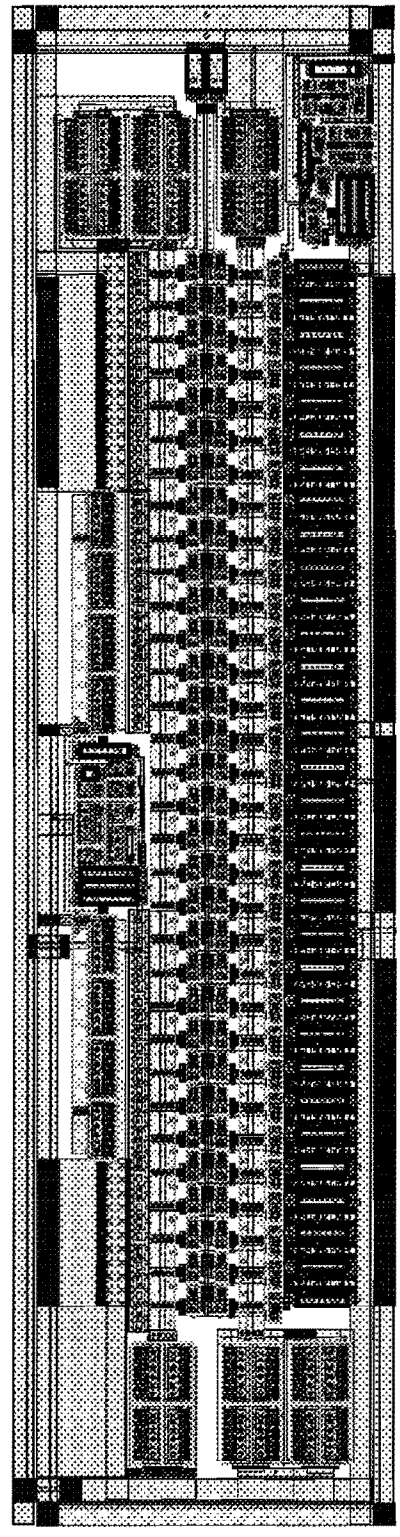

Figure C.1: *Multi-tanh cell layout*

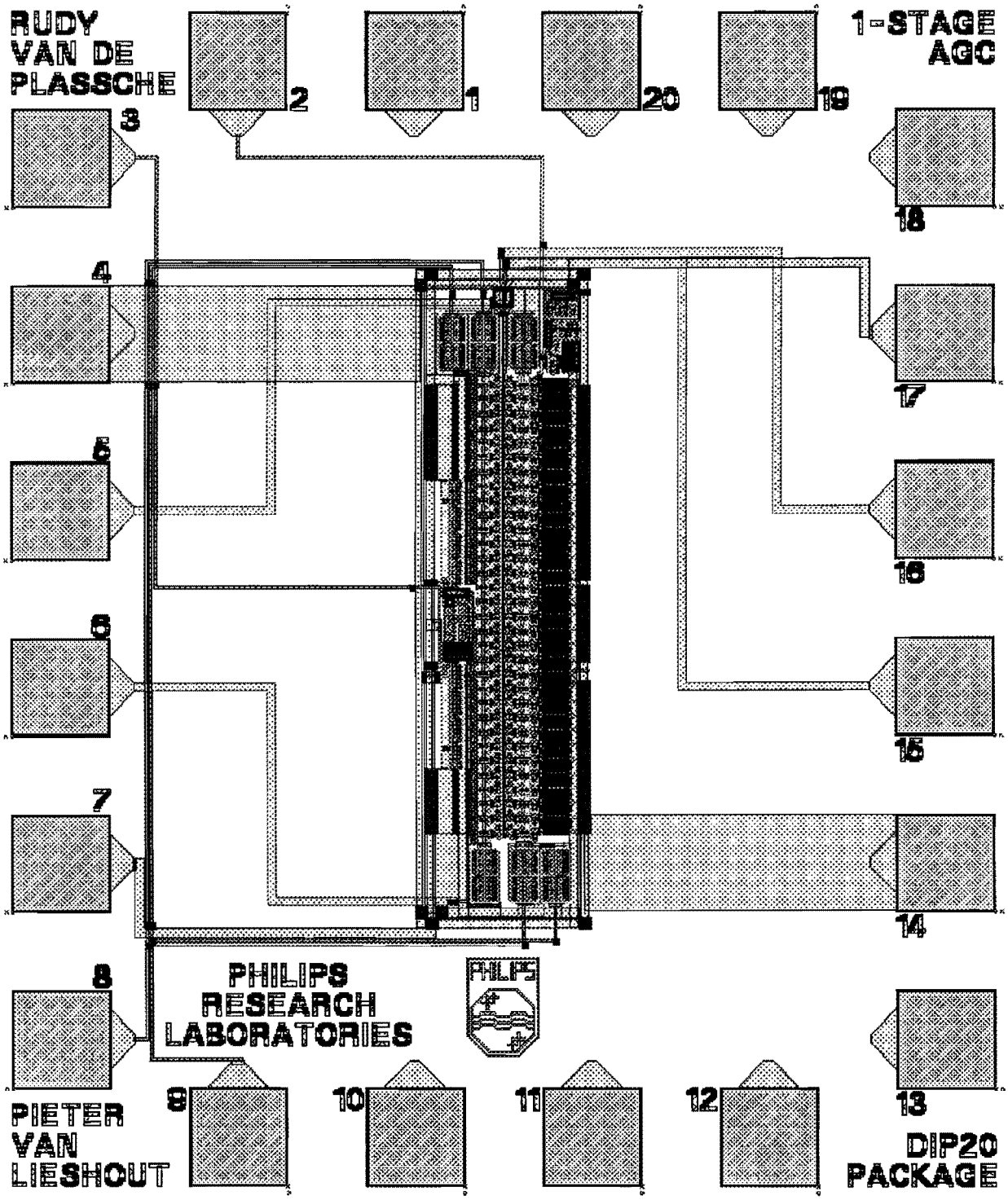

Figure C.2: *Top level of 'onestage' chip*

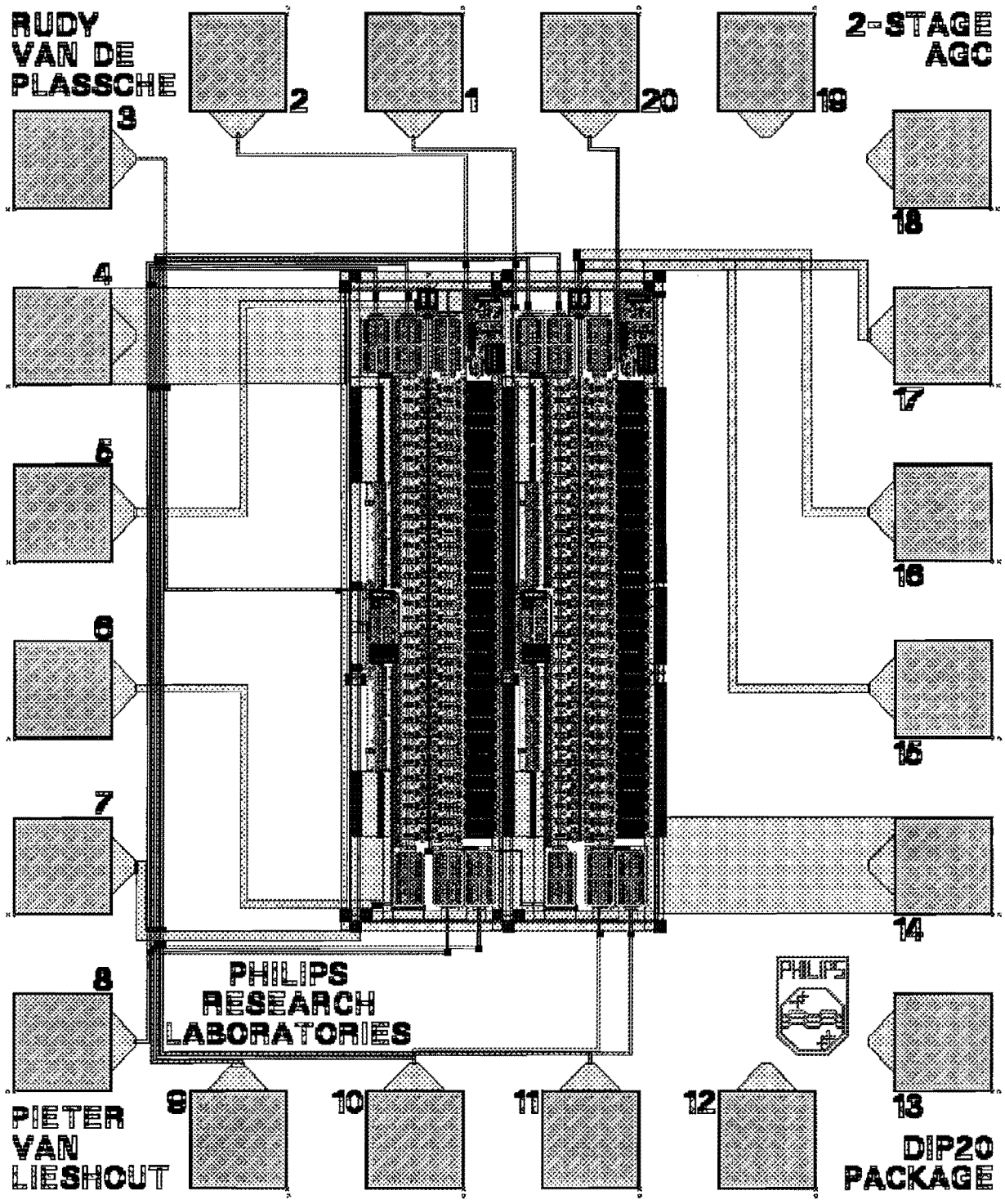

Figure C.3: *Top level of 'twostage' chip*

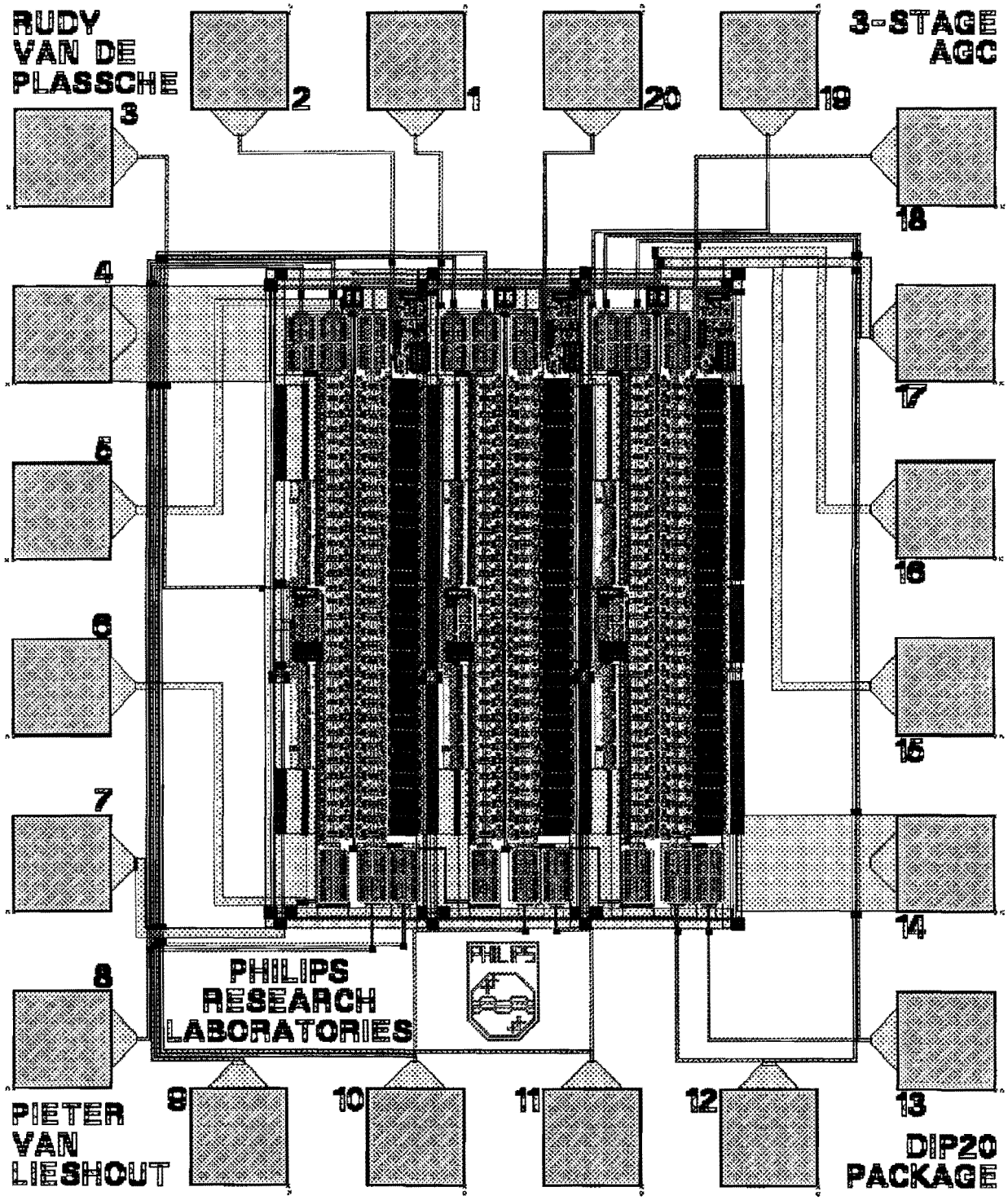

Figure C.4: *Top level of 'threestage' chip*

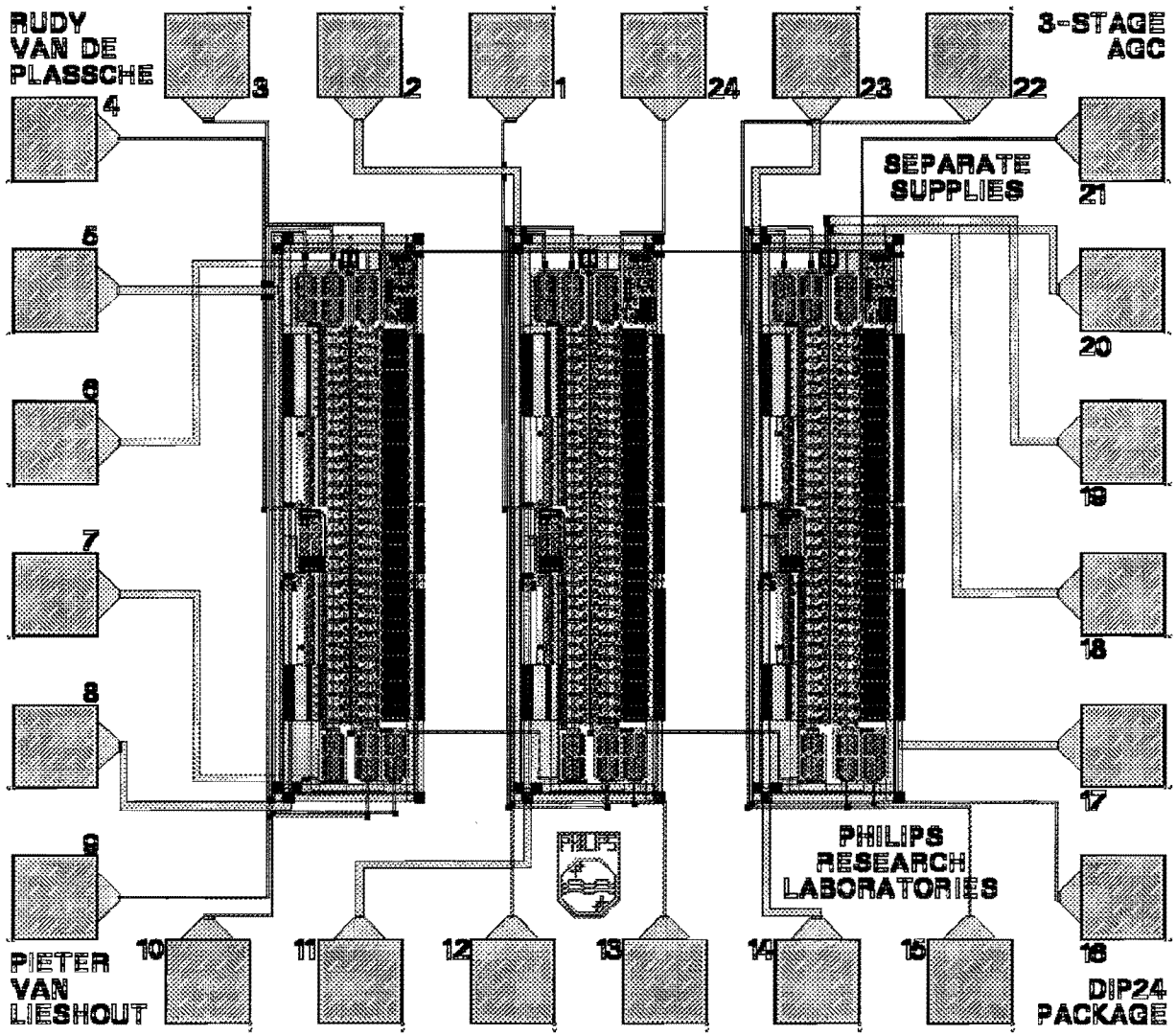

Figure C.5: *Top level of 'threesep' chip*

Appendix D

Pin configurations

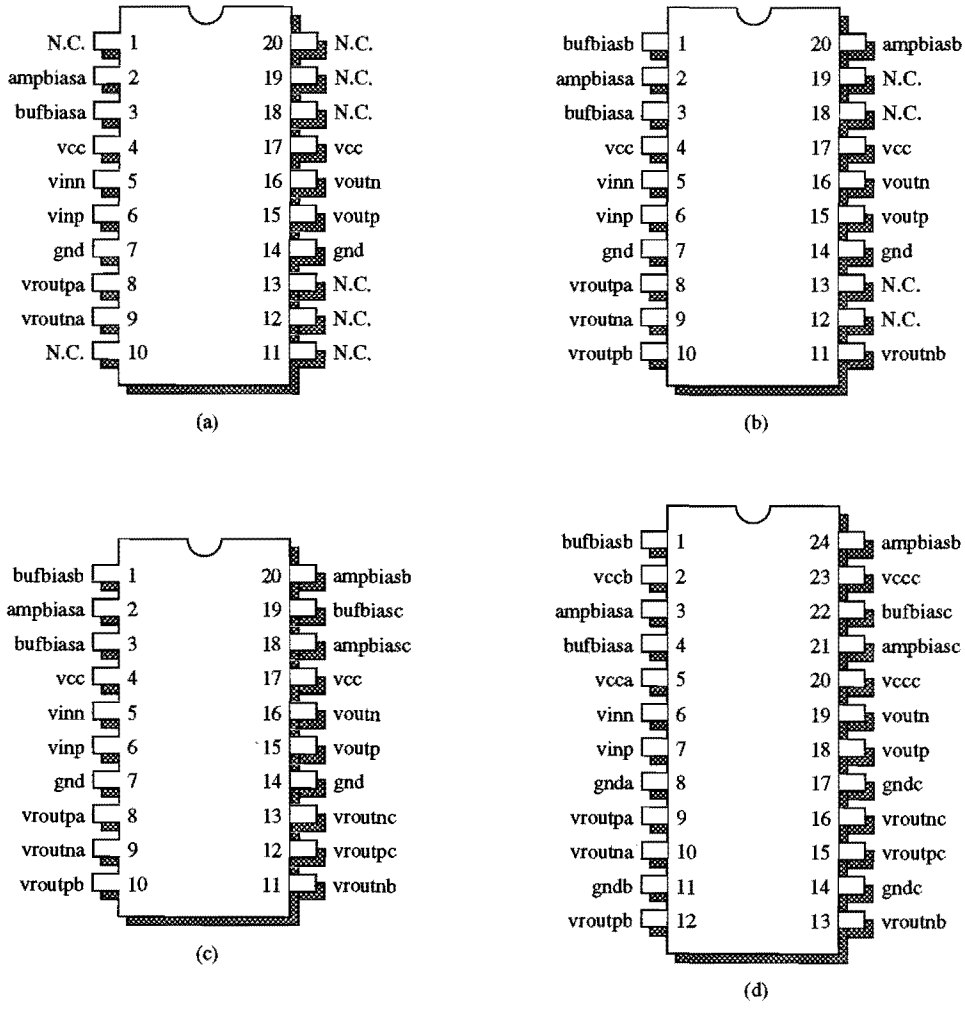

Figure D.1: *Pin configuration of* (a) *one stage chip,* (b) *two stage chip,* (c) *three stage chip,* (d) *three stage chip with separate supplies*