A 46 µw 13 b 6.4 MS/s SAR ADC with background mismatch and offset calibration

A 46μW 13b 6.4MS/s SAR ADC with Background Mismatch and Offset Calibration

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Abstract

A 6.4MS/s 13b ADC with a low-power background calibration for DAC mismatch and comparator offset errors is presented. Redundancy deals with DAC settling and facilitates calibration. A two-mode comparator and 0.3fF capacitors reduce power and area. The background calibration can directly detect the sign of the dynamic comparator offset error and the DAC mismatch errors and correct both of them simultaneously in a stepwise feedback loop. The calibration achieves 20dB spur reduction with little area and power overhead. The chip is implemented in 40nm CMOS and consumes 46μW from a 1V supply, and achieves 64.1dB SNDR and a FoM of 5.5 fJ/conversion-step at Nyquist.

Index Terms

SAR ADC, Low power, DAC mismatch, Comparator offset, Redundancy, Background calibration

I. Introduction

Wireless standards, e.g. 802.15.4g, need high resolution ADCs (>10b) and MS/s sampling rates with very low power to tackle with large interferences during communication. The SAR ADC is well-known for its excellent power efficiency. However, there are several challenges

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when the resolution goes beyond 10b: firstly, the intrinsic DAC matching is practically limited up to 10∼12b in modern CMOS technologies [1]. Scaling up the device dimensions can improve matching but it will deteriorate power-efficiency and speed. Alternatively, calibrations [2], [3], [4], [5], [6] are introduced to correct the errors and push the SNDR beyond 62dB. [2] uses an off-chip DSP engine to correct the ADC errors through a Least-Mean-Square (LMS) algorithm in the background but the overhead in area and power is high. [3] uses a similar idea with less overhead but it can not run in the background without interrupting the normal ADC operation. [4], [5] rely on a statistics-based method to calibrate the capacitor errors in the foreground. But the statistics-based methods usually have significant overhead in latency, area and power and are thus implemented off-chip.

Besides DAC mismatch, noise tends to limit the performance of high resolution SAR ADCs in modern CMOS, especially with reduced supply voltage ($\leq$1V). To achieve the required noise level while still saving power, several techniques have been proposed. A two-stage pipelined SAR ADC [6], [7], [8], [9], [10] can relax the comparator noise by introducing a low-noise amplifier between the two stages. Nonetheless, the effort to design a low-power amplifier and to overcome the induced errors (e.g., gain error, offset error) is not trivial. [11], [12] relax the comparator noise by over-sampling the comparator but they sacrifice speed due to the additional cycles. Alternatively, the comparator can be made as reconfigurable to save power while still maintaining precision [13], [14]. However, this also introduces a dynamic comparator offset, which may impede the overall accuracy of the ADC.

To counteract the issues mentioned above, this design successfully implements a 13b SAR ADC with a reconfigurable comparator and low-power on-chip background calibration for both DAC mismatch errors and dynamic comparator offset [15]. The background calibration utilizes a redundancy facilitated error-detection scheme and an analog correction scheme, which will be discussed later. Thanks to the low-power calibration, this ADC achieves an ENOB of 10.4b and

a state-of-the-art power-efficiency of 5.5fJ/conversion-step at 6.4MS/s.

Section II introduces the SAR ADC architecture as well as the principle of the calibration. In section III the implementation of the SAR ADC is shown. The measurement results will be presented in section IV and conclusions will be drawn in section V.

II. SAR Architecture and Sign-based Calibration

Calibration offers the possibility to save substantial power in the DAC and comparator by calibrating their errors. However, the calibration overhead in area, speed, power as well as architecture complexity should be kept to a minimum. Foreground calibration can compensate the error at one time but it usually needs special analog input signals (e.g., shorting input [5]) or doubled operating clock [3]. This becomes more cumbersome when more errors need to be calibrated. Besides, foreground calibration is not able to the track the time-varying errors (e.g., offset) due to environmental changes. To do that, the foreground calibration has to be repeated periodically. This is neither convenient nor efficient for a radio system. Instead, background calibration can run in the background and still calibrate the errors without interrupting the normal ADC operation.

In prior art, without knowing any information of the error, often the circuit errors are corrected indirectly in a digital fashion [2], [3], [10] via post processing. Fig. 1(a) shows the block diagram of the calibration method in [2], [3], [10]. Based on the ADC output data, a DSP engine can define a cost function, which reflects the error. Through an adaptive algorithm, e.g., LMS (Least-Mean-Square), the value of the cost function will be tuned towards zero once the coefficients W are correctly trained. To guarantee the precision of the coefficient training, redundancy is usually introduced in the DSP engine. On the other hand, a direct error detection and correction scheme is proposed as shown in Fig. 1(b). The sign of error can be detected as shown later. Thanks to the feedback loop and the analog correction circuit, it is very convenient to stepwise tune the error

towards zero based on its sign. In this way, only the sign needs to be processed compared to the whole ADC output in Fig. 1(a). Besides, power-hungry operations (e.g., multiplying in Fig. 1(a)) are avoided and only much simpler calculations (e.g, accumulation) are needed. Furthermore, instead of a blind algorithm requiring many iterations, the sign of the individual errors can be directly detected to compensate these errors, reducing the convergence time and required energy. Moreover, the actual correction is in analog domain instead of digital signal processing as shown later, consuming far less power. Overall, the proposed calibration method has very little overhead in circuit complexity, area, speed and power.

A. ADC Architecture

Fig. 2 shows the architecture of the 13b SAR ADC. In each SAR conversion, firstly the S&H samples the differential analog input voltage on the capacitor arrays inside the DAC. Using the comparator and the logic, the DAC output will approximate the sampled input voltage in several comparisons through a Successive-Approximation algorithm using a monotonic switching scheme [16]. In this design, a total of 15 cycles is used to perform a 13b conversion, where two of them are redundant cycles to overcome various errors during the conversion (e.g., DAC settling, noise), similar to [14]. The 13b output is calculated from the 15b raw code by an on-chip digital adder. A two-mode comparator is introduced to save power while still maintaining accuracy. Optionally, an additional (16^{th}) cycle can be activated for DAC mismatch calibration or comparator offset calibration as shown later. All the operations including the calibrations are asynchronously controlled. Thus, only one relatively low frequency sampling clock f_s is needed for both normal operation and calibration.

Fig. 3 shows the conversion scheme as well as the DAC of the 13b ADC. The 15 cycles include 10 coarse cycles and 5 fine cycles, where the 7^{th} and 11^{th} cycle are redundant cycles. The first redundant bit (7^{th} cycle) relaxes DAC settling time and facilitates the DAC mismatch

calibration, which will be explained later. Considering that the worst mismatch errors happen for the largest capacitors, only the first 5 DAC capacitors are calibrated in this work. The capacitors lower than the redundant bit are not calibrated thus they need to be sufficiently linear intrinsically. Thanks to the second redundant bit (11^{th} cycle), a two-mode comparator can be employed [14]. This redundancy allows, first of all, decision errors during the coarse comparisons due to the comparator noise, thus allowing a low-power mode comparator. Furthermore, since the redundancy can tolerate the residual comparator offset error after calibration as shown later, the comparator offset calibration accuracy can be relaxed. The combination of post-calibration comparator offset and coarse comparator noise should remain within the redundancy range of the 11^{th} bit, which can tolerate errors up to +/-8LSB.

B. Comparator offset error detection

As mentioned before, the comparator works in the low-power mode for the first cycles (coarse cycles) and it only switches to the low-noise mode with higher power for the last few cycles (fine cycles). In this way, the overall power consumption of the comparator is reduced while it still satisfies the noise requirement of the ADC. However, the two-mode comparator will have two different offsets for the corresponding two modes. Once this dynamic offset is beyond the redundancy range ($\pm$8LSB), the ADC performance can not be recovered. Therefore, calibration of the dynamic offset becomes necessary. The goal of the comparator offset calibration is to minimize the offset difference V_{delta}, which equals V_{off1}-V_{off2}. Since a feedback loop (Fig. 1(b)) is used to minimize V_{delta} stepwise, rather than post processing, it is sufficient to detect the sign of V_{delta} only in order to minimize its value.

The comparator dynamic offset detection is shown in Fig. 4. The equivalent voltage at the comparator input V_{eq} can be viewed as a summation of the sampled input signal V_{in}, DAC reference voltage (V_{DAC}) and the input-referred comparator offset ($V_{off1(2)}$). The optional

additional (16^{th}) cycle is performed on top of the 15-cycle comparison for a 13b ADC. The same comparison as the last (15^{th}) cycle is repeated in the additional (16^{th}) cycle. The DAC code remains unchanged, but the comparator switches from *mode2* to *mode1*. Ideally, if the two offsets are the same, the comparison result of the last cycle (D_{15}) and the additional cycle (D_{16}) would be the same. However, if the offsets are different, then the equivalent analog voltage (V_{eq}) would be different, thus causing different comparison results. The difference of D_{15} and D_{16} reveals the sign of the offset difference S_c and thus the direction in which the comparator correction circuit needs to be tuned.

C. DAC mismatch calibration

The unit capacitor C_u in a SAR DAC is mainly sized for two considerations: kT/C noise and capacitor mismatch error [17], [18]. When the ADC resolution goes beyond 10b, C_u tends to be limited by the capacitor mismatch and thus has to be sized significantly large, degrading power efficiency. Alternatively, C_u can be sized to just meet the kT/C noise to save power, and use calibration to compensate the capacitor mismatch error. To investigate the relation between the unit capacitor size and the ADC performance, a Monte-Carlo simulation in Matlab is performed. Fig. 5(a) and Fig. 5(b) show the simulated mean value of the worst-case INL and SFDR of the 13b ADC against the unit capacitor value with and without the proposed DAC capacitor calibration in 10 runs. For simplification, only capacitor mismatch errors are considered. In this design, to reach an acceptable INL error of $\leq$1LSB, C_u has to be as large as 3fF without calibration. As can be seen, with calibration, the unit capacitor value can be reduced to only 0.3fF while maintaining INL$<$1LSB and SFDR$>$90dB. In this way, calibration saves 10$\times$ switching power, while also reducing chip area and increasing conversion speed. Please note that only the first 5 capacitors are calibrated. The lower capacitors are not calibrated and are thus limiting the ADC performance after calibration.

For DAC capacitor mismatch calibration, the principle is based on the detection of DNL errors, which indicates capacitor mismatch. Fig. 6(a) shows an example of an ADC with an exaggerated DNL error Δ at the MSB capacitor. A similar picture could be drawn for the other bits of the DAC. Thanks to the redundancy, there is a convenient way to detect the sign of Δ, which is sufficient for the feedback loop in the ADC (Fig. 1(b)) to tune Δ towards zero. As shown in Fig. 6, the redundancy (i.e. 15 raw bits for a final 13 bits) implies there are multiple 15 bit codes describing the same final 13 bit output. For instance, codes A and B (Fig. 6(c)) will resolve the same 13 bit output code and are thus equivalent. However, the bits inside code A and B are different, and hence the activated capacitors to generate these two codes are also different.

V_A and V_B represents the DAC voltage of code A and B. If there is no capacitor mismatch, the sum of the activated capacitors in code A and B is equal and V_A and V_B are equal. On the other hand, if there is capacitor mismatch, the sum of the activated capacitors is not identical for codes A and B, and thus V_A and V_B will not be the same. This can be used as follows to perform a calibration as shown in Fig. 7(a): if code A is observed during a normal 15-cycle SAR conversion, a 16^{th} cycle is added and an additional comparison is performed. Before the 16^{th} cycle takes place, the internal code is updated to code B. On the other hand, if code B is detected, the internal code will switch to code A. In this way, the comparator result of the 15^{th} cycle (D_{15}) in comparison to the result in the 16^{th} cycle (D_{16}) will determine whether the analog value of code A (V_A) is larger or smaller than that of code B (V_B). With that information, the capacitors can be tuned to minimize Δ. In the calibration cycle for the MSB, the total switched capacitance here is approximately two times the MSB capacitor, resulting in about 1.2pJ DAC switching energy. This is acceptable since the calibration rate is very low as shown later, leading to a very limited power penalty.

Code A and code B are not random codes, instead they are determined by the specific DAC bit. In this example, code 1000000x and 0111111x can only reflect the MSB capacitor mismatch

errors. Only when this code occurs, the MSB capacitor will be calibrated. Similarly, other detection codes can be used for the other bit transitions. In this way, the calibrations of various bits can be performed separately and independently without interfering each other. Since the MSB capacitor mismatch can be influenced if the lower capacitors have any mismatch error, it will be only calibrated properly after the lower bits are well calibrated. Therefore, even though all capacitors are calibrated simultaneously, the resulted sequence in which the calibration stabilizes is from the lowest bit towards the highest bit as sketched in Fig. 7(b). This method works for any unknown input signal as long as the signal reaches the required codes for detection. On top of that, no additional requirement is needed for the input signal. Note that the calibration is redundancy-facilitated, as it allows permutation of the DAC code (A vs. B) at the end of the regular conversion to extract mismatch information. However, the redundancy is not absorbed by the calibration and still remains available during the conversion to deal with for instance DAC settling errors.

Fig. 8 shows the principle of the DAC mismatch correction for a single capacitor. In parallel to a nominal capacitor C_{NOM} with an ideal value (2^jC_u), a programmable capacitor array for calibration C_{cal} is connected. In this way, the capacitor values can be tuned stepwise to minimize the DNL error Δ based on the detection results. Please note that the initial value of C_{cal} is reset to zero and C_{NOM} ideally is equal to 2^jC_u. In order to either add or subtract a correction value C_{cal} from C_{NOM}, advantage is taken from the differential structure. As shown by the example in Fig. 8, switching a calibration capacitor C_{cal} either at the same or at the opposite side of the nominal capacitor C_{NOM} effectively creates an equivalent capacitor of $C_{NOM}+C_{cal}$ or $C_{NOM}-C_{cal}$, respectively. Since the switched calibration capacitor is small (a few LSBs in total, corresponding to a few fF at most), the penalty in common mode effects, power and speed are negligible. In this way, mismatches in the DAC capacitors can be corrected in a power-efficient way. To quantitatively compare the proposed analog correction method to a digital alternative, both analog

and digital correction methods for only the MSB capacitor were simulated. Both cases use a 5bit correction with a 0.25LSB correction step as shown in Fig. 9. The simulated extra power at 6.4MS/s due to the additional correction circuit for analog is 8nW, over 6 times lower than for the digital circuit (51nW). When calibrating for more bits, it is expected that analog method will be even more favorable because of the simpler layout. Besides this advantage, it should also be noted that in case of digital post-correction, the error detection should not only measure the sign but also the magnitude of each error. In case of analog correction though, it is sufficient to detect only the sign of the errors, as the feedback loop enables to tune the errors to zero.

III. Implementation of the SAR ADC

The block diagram of the implemented 13b SAR ADC is shown in Fig. 10 with the additional blocks for calibration. A clock booster circuit is used in the S&H circuit to achieve sufficient linearity [19]. A small total DAC capacitance (1.3pF) is achieved by using small unit capacitors to save power. The *Sense&Force* circuit will constantly monitor the internal DAC code. As mentioned before, certain DAC codes trigger the calibration. If one of these calibration codes occurs during the 15 comparisons, *Sense&Force* will activate the calibration by enabling the 16^{th} cycle. Before the 16^{th} comparison, either the DAC or the comparator needs to be switched as mentioned before for calibration. If the DAC calibration is detected, the *Sense&Force* will force the DAC code to its alternative (e.g., 1000000x to 0111111x) through the multiplexer. Similarly, if the comparator calibration is detected, the *mode set* block will switch the comparator from *mode2* to *mode1*. After that, the comparison of the 16^{th} cycle will be performed. Once the 16^{th} comparison is completed, the *calibration algorithm* block will determine the sign of the error (S_c or S_{dac}) based on the comparison results of the last two cycles (D_{15} and D_{16}). The sign of the error will first be processed by a digital low-pass filter (*LPF*) to filter out noise and then accumulated in the block *Cal. register* for the analog correction circuits.

A. Calibration logic implementation

Although the DAC calibration could be performed as a start-up foreground calibration since capacitor values are relatively stable against environment variations, in this work, it is still put in the background for two reasons. Firstly, it avoids dedicated time at start-up for calibration. Secondly, thanks to the low-power implementation, the penalty by performing it in the background is negligible. The proposed calibration methods can work continuously in the background to track time-varying errors due to environmental changes. Thus, the power consumption of the calibration circuit should be kept low to reduce the power consumption overhead. To reduce power, two methods have been used. First of all, to avoid unnecessary switching in the digital circuit, the specific codes that enable calibration are carefully chosen to limit the activation rate of the calibration. Table I shows the code pattern for the comparator calibration and the 5 capacitors in the DAC. For clarification, the 15-bit internal DAC code is divided into a 7bit *X*-code, a 3bit *Y*-code and a 5bit *Z*-code. For the DAC calibration, the first 7bit *X*-code is needed for detection as mentioned before. For the comparator offset calibration, it is arbitrarily set to 11000xx since it can be any code. Therefore, the total activation rate of both calibrations would be about 10.9% ((10+4)/2^7). Moreover, the *Y* code is set to code 110 to further reduce the activation rate down to 1.4% (10.9%/2^3). Overall, the detection codes are set around the center of the code range (2k$\sim$6k out of the 0$\sim$8k range), to ensure calibration even when the input is below full-scale.

As a second step to save power, the calibration logic is custom-designed. The following subsection describes several critical blocks in the calibration path, which are the Sense&Force, the low-pass filter and the calibration register implementation.

1) Dynamic logic for code detection: The *Sense&Force* circuit is continuously monitoring the internal DAC code, which changes in each conversion. The traditional CMOS logic (e.g., inverter) switches when the input signals toggle. If implemented in standard CMOS logic, the detection

circuit may still consume power even if the internal DAC code is irrelevant for calibration. In the example shown in Fig. 11(a), the circuit is used to detect the *X*-code 0111111. However, at any other *X*-code which is not desired for calibration, although the output stays unchanged, the internal logic gates in the circuits are still switching, increasing power consumption. To reduce this unnecessary switching activities, dynamic logic is introduced to implement the *Sense* circuit as shown in Fig. 11(b). In each conversion, the output node A of each single slice in the detection logic is reset to low. Only when the specific code pattern is observed in the DAC, node A of the dynamic logic will be charged to high. In the example slice shown, DAC calibration of the MSB is activated by $DAC\_U<4>$ if the *X*-code equals 0111111, *Y*-code equals 110 and DAC calibration is active (*EN_D*=1). The other 10 slices works in a similar way using the codes in Table I. The 16^{th} cycle is enabled when one of the calibrations is activated. Considering that for the 11 slices only 14 out of the 128 *X*-codes can activate the circuit, most of the time ($\sim 90\%$) the circuits are inactive. In this way, the switching frequency thus the power consumption of the detection circuit is significantly reduced.

2) Low-pass filter: After the sign of the error (S_c and S_{dac} in Fig. 10) is determined, it will be processed by a low-pass filter to filter out the noise. Fig. 12(a) shows the schematic of the implemented low-pass filter. In total, 6 filters are implemented: 5 for the DAC calibration and one for the comparator calibration. Each slice is implemented with a 6-bit bi-directional counter. The unit element of the counter, one D flip-flop and three logic gates, can perform both up counting and down counting. Two signals INC_I and DEC_I represents the polarity of the sign: up or down. In the example shown in Fig. 12(b), the counter is counting up when the signal INC_I is valid. If accidentally the signal DEC_I becomes high (e.g., due to noise), the counter will temporally count down. Once INC_I becomes valid again, the counter will count up to 63 and generate a short pulse for the signal INC_O. Similarly, a short pulse can be generated for DEC_O when the counter is counted down to 0. In such a way, the decision errors

during the calibration due to random noise can be filtered out. After that, INC_O (or DEC_O) will increment (decrement) the actual calibration register value. During normal operation when calibration is not active, both signals INC_I and DEC_I are low. In this case, the counter will stop counting while still maintaining the counted number. Therefore, the power consumption of the circuit is kept to a minimum when no calibration happens.

B. DAC architecture and capacitor mismatch correction

Fig. 13 shows the differential DAC structure for the 13b ADC, including the main DAC, the calibration DAC (for DAC calibration) and the level shifter (for comparator calibration). The main DAC uses 0.3fF as the unit capacitor to save power. As shown in Fig. 13(b), large calibration step will limit the calibration performance. In this design, the DAC calibration step is set to 0.25LSB to have a sufficiently linear DAC. Thus, the calibration unit capacitor value has to be as low as 75aF. Both unit capacitor are custom-designed utilizing the parasitic between two metal plates as shown in Fig. 13(b) [20]. Thanks to the feedback loop (Fig. 10), the DAC capacitor error will be incrementally calibrated towards zero based on the sign of the error. Moreover, the total switched capacitance for calibration is very small. Therefore, the matching of the 75aF calibration element is less critical. The capacitors for DAC calibration can be programmed through a calibration control word ($cal< k:0 >$). In such a way, the first 5 capacitors of the ADC can be calibrated with steps of 0.25LSB. The correction range is set to $\pm$7.75LSB for the MSB, while smaller ranges are used for the lower bits. The capacitor values of the regular DAC and the calibration capacitors are listed in Table II. Thanks to the small calibration circuits (NAND gates plus $\sim$aF capacitors), the overhead in area, speed and power consumption is negligible.

C. Comparator and offset correction circuit

Fig. 14 depicts the schematic of the comparator as well as the analog correction circuit for its offset. The dynamic comparator uses a preamplifier as its first stage and a cross-coupled latch as its second stage. Similar to [14], in each conversion, the load capacitor C_{load} of the first stage will be switched off in the coarse comparisons (*mode1*) to reduce the comparator energy consumption to 88fJ with a relatively high input-referred noise (IRN) of 0.6mV. Only in the fine comparisons, C_{load} is switched on to reduce the IRN of the comparator to 0.3mV with 337fJ energy consumption. In this way, the total energy consumption of the comparator is reduced from 5055fJ to 2565fJ, saving 2 times comparator power while still maintaining the same accuracy. Furthermore, a programmable array of C_{load} capacitors could be used for comparator offset correction [5]. However, this type of offset correction would also impact comparator power, speed, and noise. Therefore, to avoid these side effects,the offset difference in the two modes is corrected by two programmable capacitors (C_a and C_b) that switch when the comparator changes mode, thus inducing a voltage step V_P-V_N, which equals to $\frac{(C_a-C_b)}{C_s}V_{DD}$. This voltage step counteracts the offset step once the calibration is correctly settled. As shown in Fig. 14(b), C_a and C_b use a binary-scaled bank of capacitors and allow an offset correction of up to $\pm$63LSB with 1LSB steps. Note that the remaining offset error after calibration (within 1LSB) is inherently compensated by the redundancy.

Thanks to the simple calibration algorithm and the custom designed dynamic logic, the active area of the digital calibration circuit is only 0.0017mm^2 while the analog correction circuit is about 0.0009mm^2. To prove the concept of calibration, simulations in Matlab are executed with kT/C noise, comparator dynamic offset and DAC mismatch considered. Fig. 15 shows the Monte-Carlo simulation results (100 runs) of the ADC before and after calibration. The input signal is set to a sinewave. It is clear that calibration can correct the errors due to the device

imperfections and improve the ADC performance significantly.

IV. MEASUREMENTS

The SAR ADC is implemented in 40nm CMOS technology (Fig. 16) and occupies $0.0675mm^2$. With calibration enabled, the ADC consumes 46μW from a 1.0V supply voltage at 6.4MS/s. Fig. 17 shows the power break down of the ADC based on both the measured and simulated values. It can be seen that the calibration power is almost negligible (5%). Fig. 18 and Fig. 19 show the INL/DNL and the spectrum in three scenarios: without calibration, with comparator calibration only and with both comparator and DAC calibration. The large initial DNL errors, caused by dynamic comparator offset, are effectively reduced when comparator calibration is enabled. The DAC calibration suppresses the INL errors due to DAC mismatch, as indicated in Fig. 18. The final INL is limited by sampling switch distortion. Still, the spurs due to comparator offset and DAC mismatch are suppressed by 20dB (Fig. 19). Therefore, the SNDR and SFDR are enhanced to 64.1dB and 81.9dB at Nyquist, respectively, achieving a 5.5fJ/conv.step FoM. The SNDR is mainly noise limited by the total ADC noise (1.5LSB), which compromises for low power. Fig. 20 shows the dynamic performance with calibration enabled and the scaling of the power consumption (133nW leakage level) with sampling rate. Fig. 21 shows the performance of 4 measured samples before and after calibration. Regardless of the magnitude of the errors, the calibration is capable to suppress the errors and improve the ADC performance. The convergence time of the calibration can be measured in the following way: The ADC data is captured with the calibrations firstly disabled, and then enabled. By using a moving window over the time for the sampled ADC data, and performing Fast Fourier transforms (FFTs) for the data of each window, a figure of SNDR against time can be plotted as shown in Fig. 22. It takes approximately 400k cycles for the ADC performance to settle. The measurement results are summarized and compared with state of the art in Table III. The power efficiency of this ADC is in line with state-

of-the-art, while also integrating an on-chip background calibration technique for comparator offset and DAC mismatch.

V. Conclusion

This work demonstrated a SAR ADC with an on-chip background calibration. The calibration circuit can directly detect the sign of the errors and apply feedback to the analog correction circuits, correcting both the comparator dynamic offset error and the DAC mismatch error at the same time. Thanks to the simple calibration algorithm and the custom-designed dynamic logic, the ADC achieves 5.5fJ/conv.step at 6.4MS/s with negligible overhead in area and power.

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Benjamin Busze is a researcher with experience in digital signal processing and digital circuit design. He received his Dipl.-Ing. degree in Electrical Engineering and Information technology from the RWTH-Aachen University (Germany) in 2008. He joined Holst Centre/imec in 2008, where he works on digital baseband design for wireless systems.

Kathleen Philips is a program director at imec, in the area of Perceptive Systems for the IoT. Dr. Philips holds a PhD in Electrical engineering and has 20 years of experience in the domain of low power mixed-signal, RF and integrated system design. She started her career at Philips Research, The Netherlands, working an analog and mixed-signal circuits. She joined the Holst Centre/imec in 2007, where she is currently leading a program on ultra-low power wireless, processing and sensing systems. This is part of an open innovation collaboration, together with local and international industry. The research targets applications in the area of infrastructure and person-centric IoT systems, with a focus on ultra-low power communication and sensing.

Harmke de Groot is senior director at Holst Centre/imec for Perceptive Systems for the Intuitive Internet of Things. These heterogeneous connected systems use their own sensors as well as information from the cloud to build a view of the world surrounding them and in such a way realize a natural and intuitive experience for the end-user. Her team is internationally recognized for their work in the field of large scale sensor networks for IoT, high speed 5G networks and low power, low cost sensors. Imec contributes to the Internet of Things revolution by developing innovative algorithms, network, radio, dsp and sensor solutions for person-centric IoT, smart cities and buildings as well as automotive applications, realizing that the traditional borders between these applications domains are quickly fading. Together with a wide range of industrial and academic partners this R&D program addresses the challenges of limited autonomy, functionality, interoperability, ease of use, data fusion and security to enable a wide range of new applications and a truly intuitive user experience. She worked at NXP, Philips Research and Microsoft before joining Holst Centre/imec in 2008. De Groot is (co-)author of more than 80 publications including a book on embedded system design. De Groot received a Master of Science in Electrical and Electronics Engineering from the University of Technology Eindhoven in 1997 and a Master of Business Administration from TIAS Business school in 2013.

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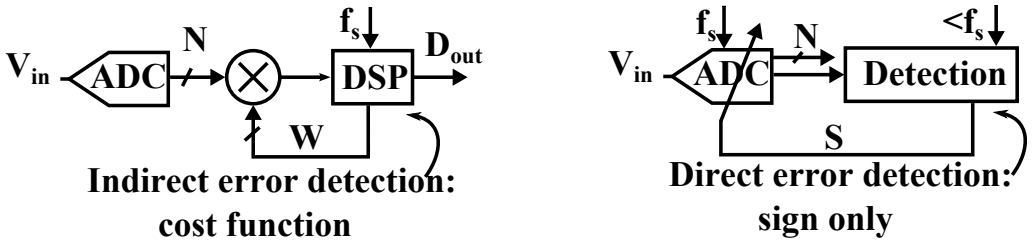

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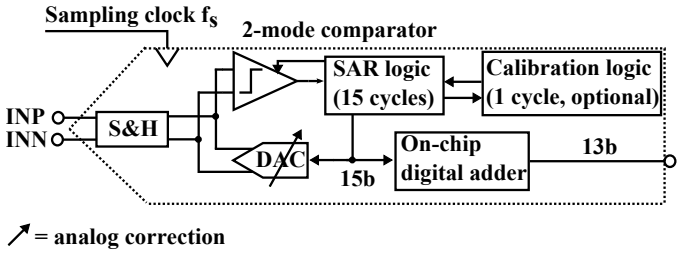

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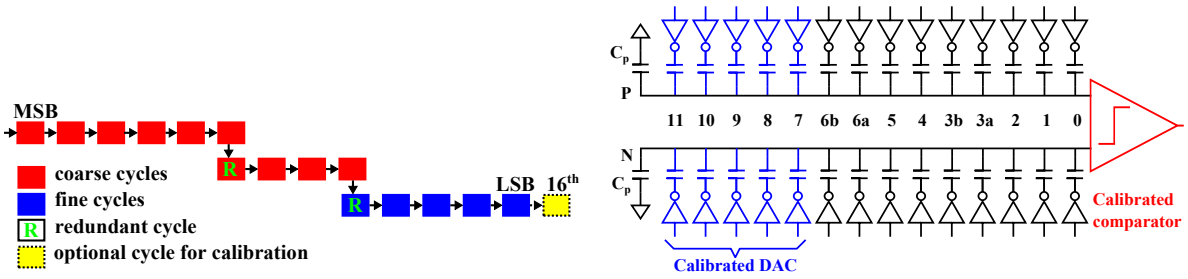

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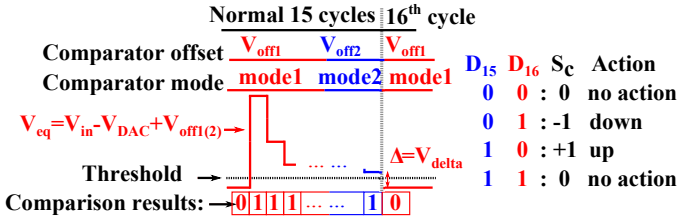

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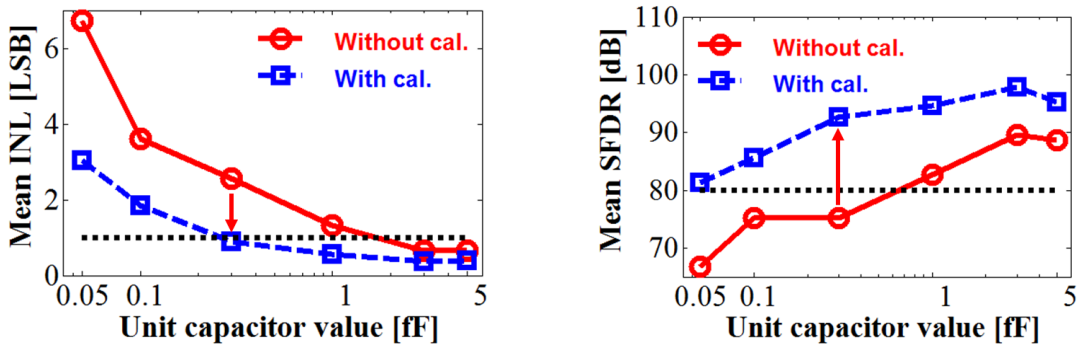

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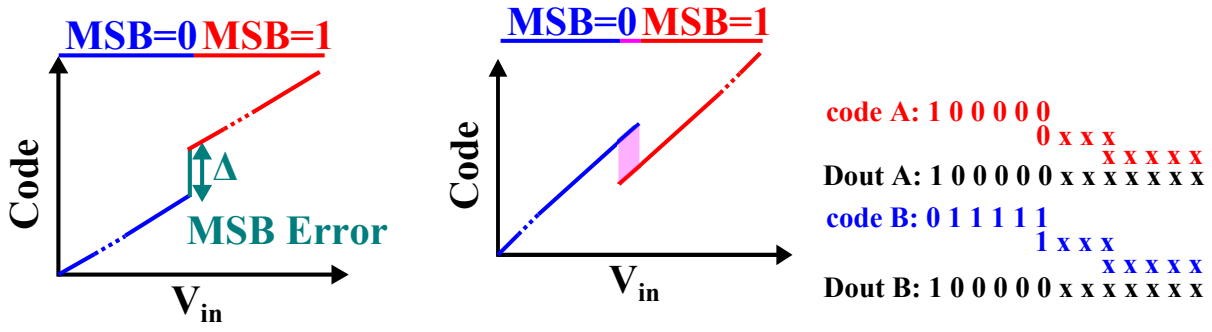

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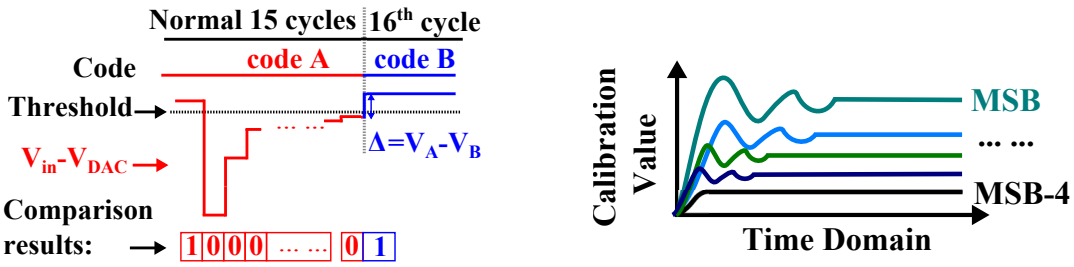

(a) (b)

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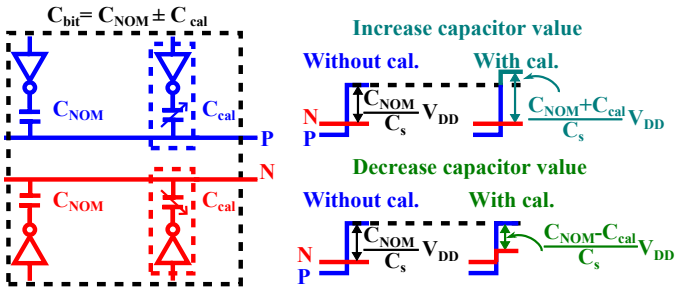

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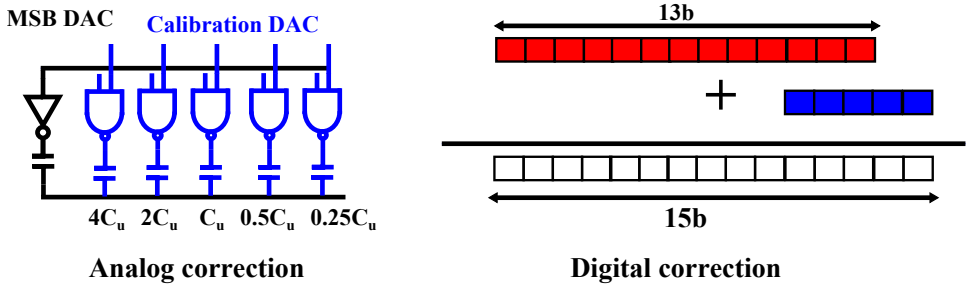

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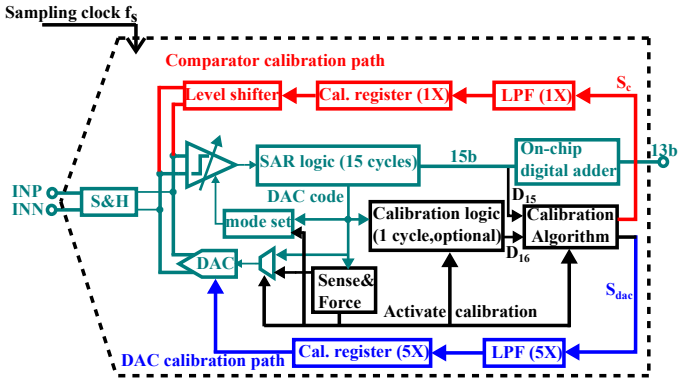
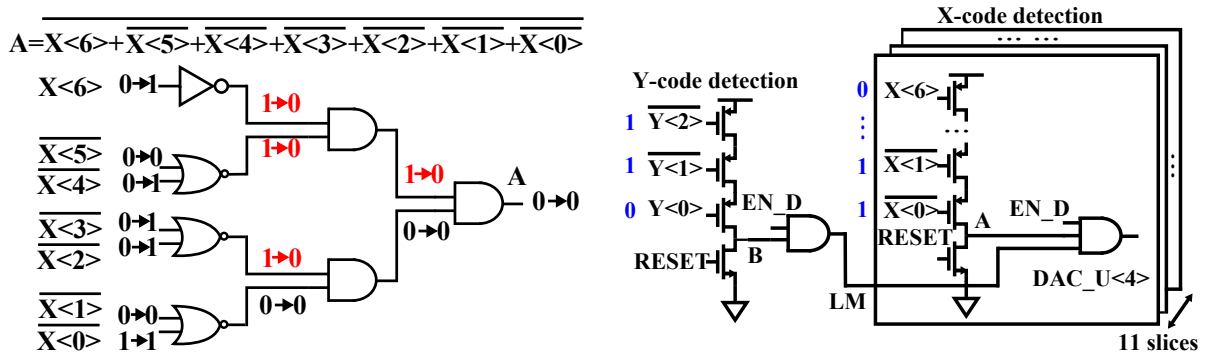


Fig. 10. Block diagram of the implemented 13bit SAR ADC.

TABLE I

THE CODE PATTERNS FOR CALIBRATION ACTIVATION.

Calibration of:	Code MSB		LSB
	XXXXXXX	YYY	ZZZZZ
MSB	0111111/1000000	110	xxxxxx
MSB-1	0011111/0100000	110	xxxxxx
MSB-2	0101111/0110000	110	xxxxxx
MSB-3	0110111/0111000	110	xxxxxx
MSB-4	0111011/0111100	110	xxxxxx
Comparator	11000XX	110	xxxxxx



(a) (b)

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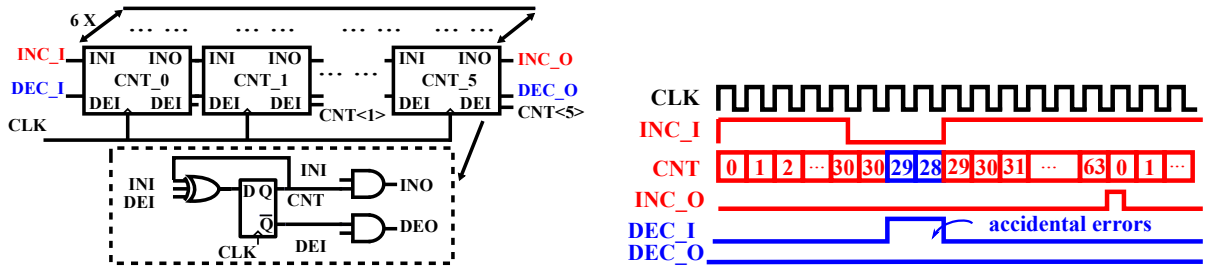

(a) (b)

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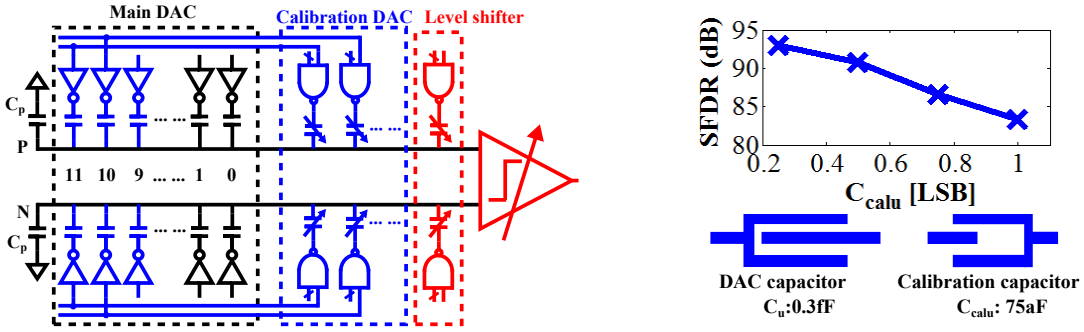


(a) (b)

Fig. 13. DAC structure (a) and unit element in the DAC and the calibration circuits (b).

TABLE II

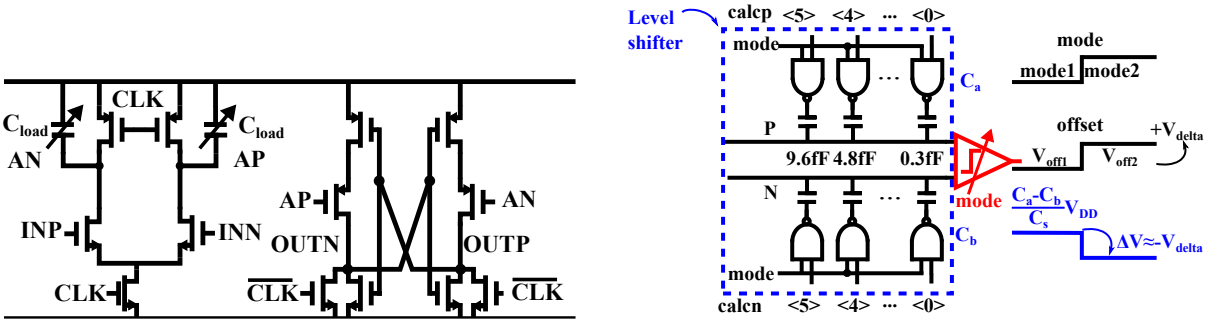
CAPACITOR VALUES IN THE MAIN DAC (A) AND THE CALIBRATION DAC (B)

(a)

DAC	C_{11}	C_{10}	C_9	C_8	C_7	C_{6b}	C_{6a}
Value (fF)	614.4	307.2	153.6	76.8	38.4	19.2	19.2
DAC	C_5	C_4	C_{3b}	C_{3a}	C_2	C_1	C_0
Value (fF)	9.6	4.8	2.4	2.4	1.2	0.6	0.3

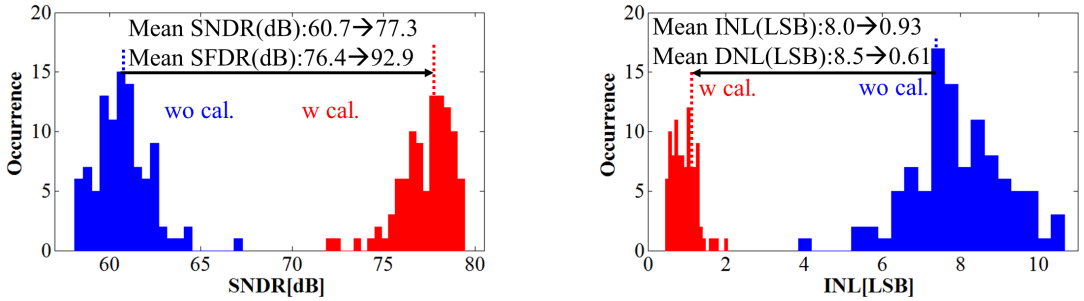
(b)

Bit / Capacitor value	<4>	<3>	<2>	<1>	<0>
MSB (fF)	1.2	0.6	0.3	0.15	0.075
MSB-1 (fF)	-	0.6	0.3	0.15	0.075
MSB-2 (fF)	-	-	0.3	0.15	0.075
MSB-3 (fF)	-	-	-	0.15	0.075
MSB-4 (fF)	-	-	-	0.15	0.075



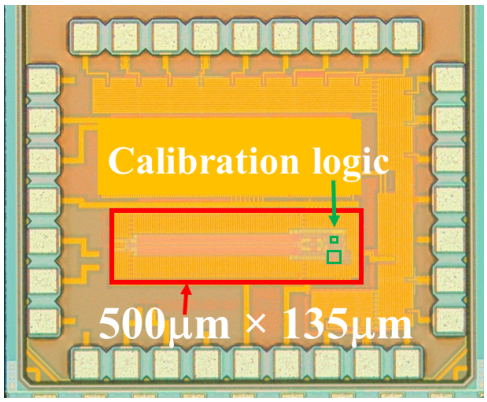
(a) (b)

Fig. 14. Comparator schematic (a) and correction circuits of comparator dynamic offset (b).



(a) (b)

Fig. 15. Simulated performance of the ADC with/without implemented calibrations (100 runs).



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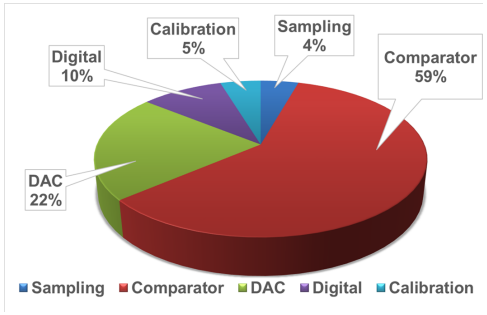


Fig. 17. Power consumption breakdown of the chip.

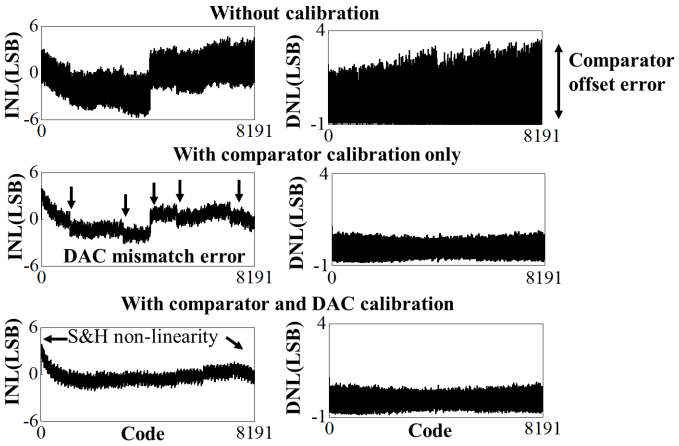


Fig. 18. Measured INL/DNL of the chip in three scenarios: without calibration, with comparator offset calibration and with both calibrations.

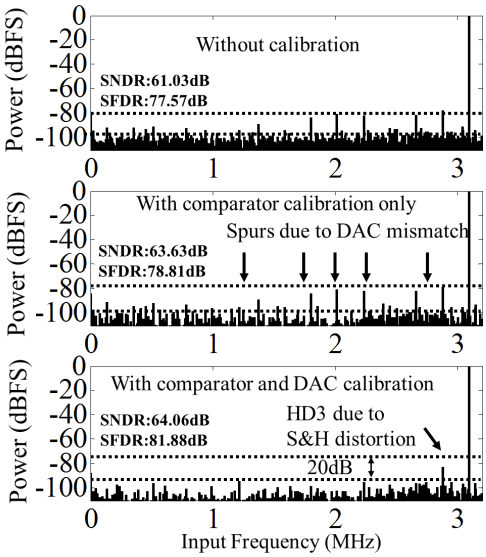


Fig. 19. Measured spectrum of the chip in three scenarios: without calibration, with comparator offset calibration and with both calibrations.

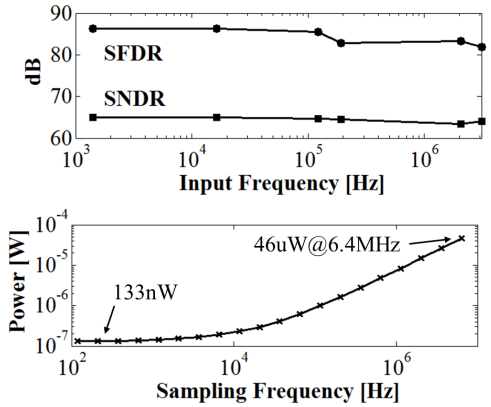
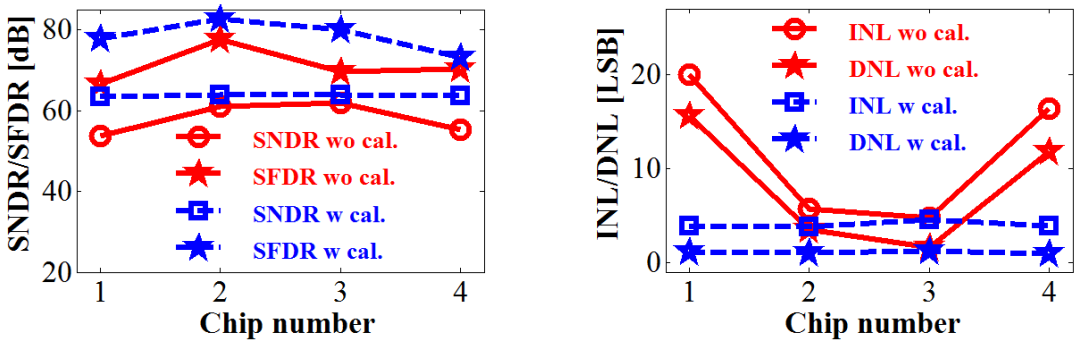


Fig. 20. Measured dynamic performance of the chip.



(a) (b)

Fig. 21. Measured performance of 4 samples.

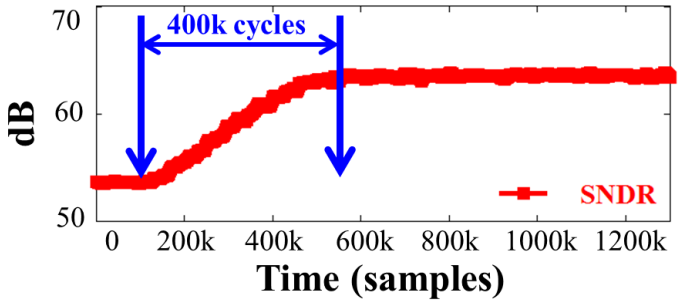


Fig. 22. Measured convergence time of the calibration loop.

TABLE III

PERFORMANCE COMPARISON OF THE ADC

	[2]	[3]		[6]	[12]	This work
Architecture	Algorithmic	SAR		Pipelined SAR TI	SAR	SAR
Technology (nm)	250	130		28	65	40
Area (mm^2)	1.6	0.059		0.1369	0.076	0.0675
Resolution (bit)	16	12		14	12	13
Supply voltage (V)	2.5	1.2		1.0	0.6	1.0
Reference Voltage (V)	2.5	1.2		1.8	0.6	1.0
Sample rate (MS/s)	1	22.5	45	80	0.04	6.4
Power (uW)	105000	2790	2820	1500	0.097	46
INL (LSB)	4.8	-	-	-	1.9	3.79
DNL (LSB)	0.66	-	-	-	0.97	1.08
Nyquist SNDR (dB)	89**	70.1	67.1	66	62.5	64.1
Nyquist SFDR (dB)	-	90.3	84.7	74	68.8	81.9
FOMW_Nyquist (fJ/conv.step)	4560**	50.8	36.3	11.5	2.2	5.5
Calibration	Off-chip	Off-chip		On-chip	-	On-chip
Cal. Circuit Area (mm^2)	Not included	0.01*		Included	-	0.0026
Cal. Circuit Power(uW)	Not included	200*		Included	-	Included

*Estimated
**Based on SNR