

Introduction to the Special Issue on the 46th European Solid-State Circuits Conference (ESSCIRC)

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Introduction to the Special Issue on the 46th European Solid-State Circuits Conference (ESSCIRC)

Welcome to this special issue of the Journal covering the 46th European Solid-State Circuits Conference, ESSCIRC 2016. The conference was held in Lausanne, Switzerland, September 13–15, 2016. From the 94 papers presented at the conference, a selection of 21 papers was made for inclusion in this special issue. As Guest Editors, we have used the inputs of the technical program committee and the session chairs, as well as the audience ratings. The selected papers are briefly introduced below.

The first seven papers belong to the RF category. The first paper by Iotti *et al.* describes a scalable arrangement of coupled LC-tank oscillators in which up to four VCO cores can be engaged on demand to improve phase noise as required by the communication channel conditions. When four cores are on, the VCO achieves record-low phase noise in E-band for backhaul infrastructure.

The second paper by Salem *et al.* proposes a fully integrated switched-mode PA that can be directly connected to a 4.8 V battery while using only thin-oxide CMOS transistors. The design uses dynamically configured stacked and flying class-D PA cells arranged in a so-called “House of Cards” architecture to deliver high efficiency at back-off levels.

The third paper by Monaco *et al.* introduces a high-resolution phase rotator for advanced serial interfaces. It linearly interpolates between eight phases spaced by $\pi/4$ and is continuously tuned by an analog/digital calibration loop. Realized in 28nm FDSOI CMOS, the 7-bit phase rotator consumes 18.6 mW at 11 GHz.

The fourth paper by Shin and Harjani describes a 4-channel polyphase-FFT I/Q filter implemented in 65nm CMOS. It uses passive switched-capacitor circuits to channelize wideband signals using linear-phase FIR filter bank with narrower main-lobe width and lower side-lobe amplitudes than in a standard FFT.

The fifth paper by Xiao *et al.* demonstrates a wideband transmit/receive (T/R) switching function without using any explicit switches in the signal path. The idea is to reconfigure the power amplifier as a low-noise amplifier in the receive mode and to utilize only DC controls to enable T/R switching. Implemented in 65-nm CMOS, the transmitter outputs up to 20 dBm with 32.7% efficiency.

The next two papers are from industry. The sixth paper by Erett *et al.* discloses Xilinx’ 0.5—16.3 Gb/s multi-standard serial link transceiver in 16nm FinFET technology. It pays special attention to the high-speed input/output interfaces. The seventh paper by Yan *et al.*, reveals Broadcom’s 802.11a/b/g/n/ac WLAN RF transceiver for 2x2 MIMO and capable of simultaneous dual-band operation. It is

realized in 40-nm CMOS and its integrated power amplifier produces up to 29 dBm saturated power.

The following three papers are power management papers. The fourth paper by Butzen and Steyaert proposes a switched-capacitor DC-DC converter that uses a multiple-input multiple-output approach to generate multiple DC voltages using only the parasitic capacitance already present in monolithic SC converters. Together with scalable parasitic charge distribution, these DC voltages can be used to power control blocks and gate drivers. This allows to achieve a peak efficiency of 98.9%. Paper number nine by Kar et al. describes a fully inductive buck voltage regulator combining wirebond inductance with on-chip capacitance. The regulator is all-digital for easy integration in standard CMOS technology. An auto-tune engine is added to compensate for passive variations. The chip was processed in 130-nm technology

Paper ten by Jiang et al. is also a DC-DC converter that employs digital techniques to enhance compatibility with CMOS processes and reduce design time complexity. A special ripple reduction scheme is added that achieves a up to 4x ripple reduction. The chip was processed in 130-nm CMOS.

Next we have two very interesting digital processors. Paper number eleven by Raina et al. is an accelerator for blind image deblurring. The clever architecture presented in the paper leads to a 56x reduction in processing time for a reference size image. Configurability in the kernel size and number of iterations gives a 10x energy scalability. The chip was fabricated in 40-nm CMOS. The second processor, paper number twelve by Keller et al. is a Risc-V SoC with an integrated power manager. Actually the power manager is based on a second, smaller, Risc-V core that can observe the main cores state and influence it voltage and frequency accordingly. No need to say that this leads to utmost flexibility in terms of dynamic power control. The chip was processed in 28-nm FD-SOI

Paper number thirteen by Jiang et al. describes a magnetic sensor that is not only very accurate but also very stable over temperature. It is designed for contactless current measurements. The main highlight is a novel multipath arrangement of hall sensors and pickup coils. The circuit is processed in 180 nm technology.

The fourteenth paper by Wu et al. is about an all-digital PLL. At its heart is a fine resolution delta-sigma Time-to-Digital converter. It realizes an error feedback topology, which is employed in the ADPLL to achieve low phase noise of the PLL via higher-order noise shaping in the loop. The ADPLL also contains a digitally controlled oscillator with nearly an octave frequency range. The chip is processed in 40-nm CMOS.

The next two papers deal with design methodologies and their application to circuit design. Paper number fifteen presents a design methodology that exploits standard cell design with differential transmission gate logic to enable ultra-low voltage and

energy-efficient operation, together with variation resiliency and high speed in microcontroller systems. The methodology is demonstrated with two prototype ICs in 40-nm CMOS. Paper sixteen proposes a methodology to compile ADCs from a SPICE netlist, a technology rule file, and an object definition file into a layout that is free from DRC and LVS errors. The method is applied to compile a 9-bit 20 MS/s 3.5 fJ/conv.step SAR ADC in 28 nm FDSOI.

The following two papers describe analog-to-digital converters. Paper number seventeen presents a single-channel calibration-free 12b ADC sampling at 600MS/s, which is based on a hybrid architecture incorporating a pipelined and an asynchronous SAR ADC. The circuit is implemented in 28-nm UTBB FD-SOI and exploits extensively forward body bias (FBB) to enhance performance. Paper number eighteen discusses a VCO-based continuous-time $\Delta\Sigma$ modulator, which includes a fully-digital phase extended quantizer that doubles the VCO quantizer resolution compared to prior art, and a tri-level resistor DAC that enables a dynamic power saving.

Paper number nineteen describes a true random number generator (TRNG) based on a discrete-time chaotic map approach, which shares the coarse-ADC with a sub-ranging SAR ADC to achieve area reduction. The system is designed for RFID applications requiring both data conversion and random number generation for secure communications.

Paper number twenty reports on a hybrid SAR-VCO $\Delta\Sigma$ Capacitance-to-Digital Converter which is implemented in 40-nm CMOS. The circuit samples a reference voltage on the sensing capacitor and quantizes the charge stored by a 9-bit SAR ADC. The residue is fed to a ring VCO and quantized in the time domain. The outputs of the two stages are combined to obtain a quantized output with first-order noise shaping.

The last paper presents a 4th-order continuous-time Follow-the-Leader-Feedback (FLFB) low-pass filter. The superior FLFB noise behavior is exploited together with a custom implementation based on combination of Active-RC/Active-gm-RC cells to bring power consumption down to 12.6 mW. The circuit achieves 21.5 dBm in-band IIP3 and 87 μ VRMS input-referred noise integrated in the 22.5 MHz band.

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Best regards,

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Eugenio Cantatore received his Master's and PhD Degree in Electrical Engineering from Politecnico di Bari, in 1993 and 1997 respectively. From 1997 to 1999 he was fellow at the European Laboratory for Particle Physics (CERN), Geneva. In 1999 he moved to Philips Research, Eindhoven, as senior scientist and in 2007 joined Eindhoven University of Technology, where he has been full professor since 2016. His research interests include the design and characterization of electronic circuits exploiting emerging technologies and the design of ultra-low power micro-systems. He has authored or co-authored more than 150 papers in journals and conference proceedings, and 13 patents or patent applications. He is active in the Technical Program Committees of IWASI, ESSDERC, ESSCIRC and ISSCC. From 2013 till 2016 he was chair of the Technology Directions subcommittee, and he is presently Program vice-chair of ISSCC. In 2006 he received the Beatrice Winner Award for Editorial Excellence from ISSCC and was nominated in the Scientific American top 50 list. He received the Philips Research Invention Award in 2007, the Best Paper Award from

ESSDERC in 2012 and the Distinguished Technical Paper Award from ISSCC in 2015. Eugenio Cantatore is a Fellow of the IEEE.



Wim Dehaene was born in Nijmegen, The Netherlands, in 1967. He received the M. Sc. degree in electrical and mechanical engineering in 1991 from the Katholieke Universiteit Leuven. In November 1996 he received the Ph. D degree at the Katholieke Universiteit Leuven. His thesis is entitled “CMOS integrated circuits for analog signal processing in hard disk systems.”

After receiving the M. Sc. Degree Wim Dehaene was a research assistant at the ESAT-MICAS Laboratory of the Katholieke Universiteit Leuven. His research involved the design of novel CMOS building blocks for hard disk systems. The research was first sponsored by the IWONL (Belgian Institute for Science and Research in Industry and agriculture) and later by the IWT (the Flemish institute for Scientific Research in the Industry). In November 1996 Wim Dehaene joined Alcatel Microelectronics, Belgium. There he was a senior project leader for the feasibility, design and development of mixed mode Systems on Chip. The application domains were telephony, xDSL and high-speed wireless LAN. In July 2002 Wim Dehaene joined the staff of the ESAT-MICAS laboratory of the Katholieke Universiteit Leuven where he is now a full professor and head of the MICAS division. His research domain is circuit level design of digital circuits. The current focus is on ultra-low power signal processing and memories in advanced CMOS technologies. Part of this research is performed in cooperation with IMEC, Belgium, where he is also a part time principal scientist.

Wim Dehaene is teaching several classes on electrical engineering and digital circuit and system design. He is also very interested in the didactics of engineering. As such he is guiding several projects aiming to bring engineering to youngsters in secondary education and he is a teacher in the teacher education program of the KU Leuven.

Wim Dehaene is a senior member of the IEEE. Wim Dehaene is the technical program-chair for ESSCIRC 2017



Robert Bogdan Staszewski (M'97—SM'05—F'09) was born in Bialystok, Poland. He received the B.Sc. (*summa cum laude*), M.Sc., and Ph.D. degrees in electrical engineering from the University of Texas at Dallas, Richardson, TX, USA, in 1991, 1992 and 2002, respectively.

From 1991 to 1995, he was with Alcatel Network Systems, Richardson, where he was involved in SONET cross-connect systems for fiber optics communications. In 1995, he joined Texas Instruments Incorporated, Dallas, TX, USA, where he was elected as a Distinguished Member of Technical Staff (limited to 2% of technical staff). From 1995 to 1999, he was involved in advanced CMOS read channel development for hard disk drives. In 1999, he co-started the Digital RF Processor (DRP) group within Texas Instruments with a mission to invent new digitally intensive approaches to traditional RF functions for integrated radios in deeply scaled CMOS technology. From 2007 to 2009, he was a CTO of the DRP group. In 2009, he joined the Delft University of Technology, Delft, the Netherlands, where he currently holds a guest appointment of Full Professor (*Antoni van Leeuwenhoek Hoogleraar*). Since 2014, he has been a Full Professor with the University College Dublin (UCD), Dublin, Ireland. He has authored or co-authored four books, five book chapters, 220 journal and conference publications, and holds 160 issued US patents. His current research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters and receivers. Prof. Staszewski was a chair of Technical Program Committee (TPC) of Dallas IEEE Circuits and Systems Workshop between 2005 and 2008. He was a TPC member of IEEE International Solid-State Circuits Conference (2008-2012), IEEE Radio-Frequency Integrated Circuits symposium (2010-2014), and IEEE International Symposium on Radio-Frequency Integration Technology (2009-2014). He is currently a TPC member of the IEEE European Solid-State Circuits Conference (since 2013) and IEEE International Symposium on Circuits and Systems (since 2010). He is an IEEE Fellow and a recipient of the 2012 IEEE Circuits and Systems Industrial Pioneer Award.