Wet-etched three-level silicon interposer for 3-D embedding and connecting of optoelectronic dies and CMOS ICs

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Wet Etched 3-Level Silicon Interposer for 3 Dimensional Embedding and Connecting of Opto-electronic Dies and CMOS ICs

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Abstract—Ultra-compact optical sub-modules for parallel optical interconnects are demonstrated based on a 3-level silicon interposer, which is fabricated through a low cost wet etching process. Using three steps of wet etching of silicon, a multi-level cavity is formed for embedding and flip-chipping optical and electrical dies, and opening optical through silicon vias. In order to reduce thermal coupling between CMOS and GaAs dies, a 50 μm thermal isolation air gap is formed between dies as part of the assembly concept, and thermal simulations and experiments are carried to validate its effectiveness.

Based on this 3D packaging concept, compact 4 mm × 6 mm, 10 Gbps 12-channel transmitter and receiver sub-modules are fully assembled and tested. Clear and uniform eye patterns for both modules are captured at 10 Gbps and 15 Gbps for every channel. Bit error rate (BER) testing is also performed. Both transmitter and receiver sub-modules show uniform BER curves, with receiver sensitivity spreading less than 1 dB at a BER lower than 10^{-12}. Also, crosstalk for both modules is tested, yielding only a 0.1 dB and 0.8 dB additional penalty for transmitter and receiver respectively.

Index Terms—Optical interconnects, transceiver, silicon interposer, thermal isolation, heterogeneous integration, flip chip

I. INTRODUCTION

The growth of data centre (DC) and high performance computer (HPC) is accelerated by the tremendous amounts of generated data, which requires the number and speed of interconnects to grow accordingly [1, 2]. Optical links have taken over all long haul transmission in past decades and, with the projected increase in intra data center bit-rates, offer a compelling alternative to electrical interconnects from board-to-board and chip-to-chip [3]. Due to the huge number of required interconnects, cost plays a major role in the choice of technology to be deployed. Short reach optical interconnects, which are made using vertical-cavity surface-emitting lasers (VCSELs) and multimode fiber, offer now the lowest cost option [4]. In addition, as the number of chip’s I/Os keeps increasing together with the data rate, the amount of channels in same area is also increasing, demanding optical interconnects to move closer to chip’s I/Os with higher bandwidth density [3, 4].

Electro-optical transceivers are essential parts in the optical communication links, converting electrical signals into the optical domain and back to the electrical domain. A small form factor electro-optical transceiver is needed to meet the demand of converting signal in close proximity to the CMOS ASIC. As mentioned above, multimode VCSEL and surface illuminated photodiode (PD) can be used to enable low cost solutions because of easy coupling with multimode fiber. However, small footprint transceiver modules are offered at very high prices due to the high cost of packaging and assembly [5]. A cost effective packaging concept, which considers the integration of electrical, optical and thermal connections, for opto-electronic dies and CMOS ICs is necessary.

Different platforms are explored for the packaging of those dies, such as glass carrier [6], flexible print circuits [7] and silicon carrier [8, 9]. All of these employ flip-chip technology to replace bond wires and shorten the trace between electronics and optics, and get higher density at the same time. In packaging solutions, 3D stacking is the best way to achieve highest bandwidth density and short connections [10]. Also the reflowing of photoresist has been demonstrated as a bridge for connecting traces at a low cost process [11]. However, when stacking dies, thermal removal becomes a big issue [12, 13]. In the heterogeneous integration, unwanted thermal crosstalk, especially for more sensitive optoelectronic dies, like VCSEL [14], is another big challenge. Therefore, an effective solution to reduce thermal crosstalk is essential for any viable 3D stacking solution involving CMOS and electro-optical dies.

Recently, we have presented initial results for a proposed 3D embedding concept of optical and electrical dies based on wet etched silicon interposer, while addressing the thermal issues at low cost [15]. In this paper, the concept is extended to fabricate silicon interposers for both transmitter and receiver sub-modules and a comprehensive set of measurements is carried out to evaluate the performance of the 3D stacked sub-modules. Firstly, the assembly concept will be described. Compared with the 2.5D silicon interposer platform [16], the resulting sub-module is 50% smaller. Secondly, thermal transfer is simulated for 3D module and 2.5D module. Through
this novel embedding approach, thermal crosstalk is reduced by providing an isolating air gap between opto-electronic and CMOS dies, while showing similar heat distribution of the 2.5D module. In section four, the process is summarized following the 3 wet etching steps. In section five, after assembling both 12-channel transmitter and receiver, we characterize them with commercial modules. Both modules show uniform eye patterns and excellent receiver sensitivity curves. Every channel can work up to 15 Gbps, 50% higher than chip nominal design specification, which means up to 180 Gbps data capacity per sub-module. Limited crosstalk related power penalty of less than 0.1 dB and 0.8 dB for transmitter and receiver respectively, is also measured. Finally, the working temperature is measured for both VCSEL and CMOS IC to validate the thermal isolation of the air gap.

II. PACKAGING CONCEPT

As shown in Fig. 1, the packaging concept is based on a low cost wet etching process, leading to a 3-level silicon interposer. We designate the area in the center of the CMOS die for the placement of the optics die. In this way, the silicon interposer is used to connect to the pads on CMOS IC which are normally located on the perimeter of the chip.

For the electrical connections, all of the traces are lithographically transferred and electroplated on the multi-level topology. In Fig. 1, the connections between the CMOS chip and the optical die are routed through the second etched face, and they can be made as short as 550 μm. The other pads on CMOS chip are routed through the first etched face and redistributed to fan-out 250 μm pitch on the surface of silicon interposer. The differential traces, which guide high speed signals, have been designed to be 100 Ω impedance matched traces.

For the optical connections, optical through silicon vias, for each channel, are opened by wet etching. A commercial right angled mirror lenses array (from Enplas Corporation), is utilized for light coupling into standard MT ferrule and is fixed at the bottom of the interposer.

The CMOS IC and opto-electronic die are respectively embedded and flip-chipped onto the wet etched 3-level cavity on the silicon interposer. The footprint of the fully assembled 12-channel transmitter/receiver module can be scaled down to 4 mm × 6 mm, which takes only half the area of a 2.5D assembly. An air gap is created between CMOS IC and optical die by insuring that the depth of the etched cavity exceeds the thickness of the opto-electronic chip.

III. THERMAL MODELING AND ISOLATION AIR GAP

When stacking a relatively high power consuming CMOS with a low power electro-optics die, proper thermal isolation is essential to avoid over heating the optics. Air, with a thermal conductivity of 0.026 W/m·K, is a good thermal isolator, and it has been used for thermal isolation by local wet etching of the substrate [17] or selective dry etching of silicon [18]. However, in both cases, extra process steps to create an air cavity are needed. In addition, in 3D integration, stacked dies are connected directly by vias or solders, and this connections will also transfer heat from high power chip to low power chip. In our packaging architecture, an isolating air gap between the stacked dies is formed after assembly, and the indirect connections between dies are patterned on the interposer. Therefore, most of the heat will be transferred by silicon. Besides, the thickness of air gap can be easily controlled by the etching time. We utilize COMSOL heat transfer module to simulate the heat transfer in the 3D packaged module, as well as 2.5D module as a reference.

The physical dimensions of the CMOS IC and optics are 3800 μm × 2250 μm × 200 μm and 3000 μm × 250 μm × 150 μm (L × W × H), respectively. Both dies are connected with a silicon interposer measuring 6000 μm × 4000 μm × 400 μm, through gold bumps. The mechanical representation of the fully assembled module is shown in Fig. 2a. The power dissipation of the CMOS IC is set to be 1.02W. In the scheme, the heatsink will be connected on the backside, so two blocks of copper, 6000 μm × 1000 μm × 500 μm, are designed attached to the interposer, which will be a part of heatsink.

To simplify the simulation, we treat the bottom side of the copper blocks as a convective boundary, with a heat transfer
coefficient (HTC) of 5000 W/°C·m². According to this heat dissipation capability, the thermal resistance of a heatsink can be calculated to choose a heatsink, which will be 1/(5000 × 2 × 6 × 10⁻⁶) = 16.67 °C/W. Any heatsink with similar or lower resistance can be used to satisfy this condition. We can also estimate the size of the heatsink [19], which should be further attached to these two copper blocks, shown in Fig. 1. A simple copper round pin heat sink, with the dimension of 6 mm × 6 mm × 15 mm (L × W × H) exhibit a thermal resistance of 14.13 °C/W in air flow rate of 1.0 m/s, which can fulfill the requirements given above.

The top side of the sub-module is in ambient air, and the thickness of air is set to 400 μm. The HTC of all other boundaries is set to 5 W/°C·m², nearly adiabatic. We assume the initial temperature is at room temperature (22 °C), and the solver runs the calculation until the system is in thermal equilibrium.

The simulation results of thermal gradient for the designed 50 μm air gap after fabrication is shown in Fig. 2 (b). The highest temperature in the module is 41.6 °C, located in the center of CMOS IC, and the temperature of the optics stays at 37.8 °C, 3.8 °C below CMOS IC, which exhibit better heat distribution than 3D packaging with air gap and TSV connection [18]. When the CMOS IC is working at higher power, the isolation effect will be more obvious. We also investigate thermal gradient with the same module in the same condition, when no air gap is present: the optics and CMOS IC experience, under these conditions, approximately the same temperatures (40.2 °C and 41.0 °C), in Fig.2(c). In addition, the different thickness of air gap is also simulated. In our concept, when it is thicker than 5 μm, the temperature difference becomes stable.

As a comparison, the 2.5D packaged module is also simulated. The same dies are connected on silicon interposer side by side. The heat dissipation is again included through the use of same copper blocks. The result is shown in Fig. 3. The temperature of optics is 5.8 °C below electronics, however, it stays at 42.8 °C, a little higher than optics in 3D module. This is due to the limited heat transfer possible via the thin layer of silicon underneath the dies. The simulation results are summarized in Table 1.

![Fig.3. Simulation results of heat transfer in 2.5D package architecture.](image)

<table>
<thead>
<tr>
<th>Module</th>
<th>Optics Temperature (°C)</th>
<th>Electronics Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3D no air gap</td>
<td>40.2</td>
<td>41.0</td>
</tr>
<tr>
<td>3D 50 μm air gap</td>
<td>37.8</td>
<td>41.6</td>
</tr>
<tr>
<td>2.5D</td>
<td>42.8</td>
<td>48.6</td>
</tr>
</tbody>
</table>

The heat transfer simulation results show a similar temperature distribution in optics and electronics, because the optics is in a similar thermal environment in both 2.5D and 3D packages. Due to the air gap between the optical die and CMOS chip and indirect electrical connection, the heat generated in the CMOS IC is not directly transferred to the electro-optic die: the vertical air gap reduces thermal crosstalk in this packaged module.

### IV. Fabrication and Assembly Process

![Fig.4. Process step of silicon interposer: (a) SiNx deposition; (b) 1st KOH etching for electronics; (c) 2nd KOH etching for optics; (d) lithography on etched topology; (e) electro-plating traces and solder bumps; (f) wet etching on both sides; (g) flip-chip bonding of optics, electronics and lens array.](image)

The fabrication process starts on a cleaved 1-inch silicon sample, with thickness of 400 μm. The process flow is shown in Fig. 4. A layer of silicon nitride is the mask for silicon etching in KOH, and it is selectively removed for the first and second etching. The convex corner is smoothened by TMAH etching, enabled by different etching rate of crystal faces [20], which will be beneficial for the spin coating. The cross section of etched cavity is shown in Fig. 5. Electro-plating base is sputtered, and lithography is performed on the etched topology.
for traces plating. After plating and removing the sputtered layer, the optical vias are vertically opened by wet etching [21]. As shown in Fig. 6, the differential traces are formed through the first etched face to fan out pads, and the traces between CMOS chips and optics are plated through the second etched face. Zoomed in photo shows the patterned traces and optical vias.

We fabricate the silicon interposers for 10 Gbps 12-channel transmitter and receiver in one process, and they are cleaved out for assembly after processing. Thermal compression bonding is used for both optics and electronics on a flip chip bonder. As shown in Fig. 7, optics are aligned and embedded in silicon interposer, and SEM photos are also taken at backside to check the alignment of the VCSEL and PIN array.

For the light coupling, a lens array is also passively aligned and fixed on the back side of silicon interposer. After that, a standard MT ferrule can be connected with the assembled module for testing purpose. The photos in Fig. 8 show the top side and back side of the assembly.

V. High Speed Characterization

The assembled transmitter and receiver are evaluated on the same probe station. The differential probes are used for high speed electrical signals connection. A standard 12-channel MT ferrule is connected through the guide pins, and break out to 12 LC fiber. A commercial SFP+ module (AFBR-709SMZ from Avago) and QSFP28 (Cisco QSFP-100G-SR4-S) are used as 10 Gbps and 15 Gbps light source and photo detector, respectively, for the module characterization. The BER curves are measured at 10 Gbps and compared with the SFP+ module, and eye patterns are captured at 10 Gbps and 15 Gbps.
A. Transmitter Sub-Module

During transmitter testing, all of the channel are turned on, and the input electrical signal is supplied by a pattern generator. A 10 Gbps non return to zero (NRZ) with a $2^{31-1}$ pseudo random bit sequence (PRBS) signal is fed by multiple differential RF probes (signal-signal) through fan-out pads of the silicon interposer of each channel. The converted optical signal is detected by the SFP+ module, and output electrical signal is characterized by an error detector and an oscilloscope. The BER curves of 12 channels transmitter, together with module to module, are shown in Fig. 9. A representative eye pattern is shown in the insert panel. Error free operation ($10^{-12}$) can be obtained, when received power is above -10.2dBm. The spread of BER curves is less than 1dB, which indicates uniform performance of all channels.

Fig. 9. The BER curves for each channel and SFP+ in transmitter test. Insert: representative eye pattern captured at 10 Gbps.

We also test the performance at 15 Gbps, PRBS $2^{31-1}$, 50% higher than the chip nominal design specification, by replacing the SFP+ with QSFP28. The clear eye patterns of all channels are captured and shown in Fig. 10.

B. Receiver Sub-module

Similarly, in receiver testing, the 10 Gbps NRZ $2^{31-1}$ PRBS optical signal is generated by the SFP+ module and fed through the MT ferrule. The converted differential electrical signals are picked up by differential probes and characterized by the same error detector and an oscilloscope. A representative eye pattern of receiver output is shown in the insert panel. Also, the BER curves of 12 channels, together with module to module performance, are shown in Fig. 11. Uniform performance of all channels are also obtained, and spread of BER curves is less

Fig. 11. The BER curves for each channel and SFP+ in receiver test. Insert: representative eye pattern captured at 10 Gbps.

Fig. 12. The uniform eye patterns of 12-channel receiver, which are working at 15 Gbps.

Fig. 10. The uniform eye patterns of 12-channel transmitter, which are working at 15 Gbps.
than 1 dB. However, a penalty of about 1.5 dB is measured, which can be attributed to the coupling losses of the angled mirror lens array. The receiver module is also tested at 15 Gbps, PRBS $2^{31}-1$, and clear eye patterns are shown in Fig. 12.

C. Crosstalk Effect Characterizing

The effect of channel crosstalk (including electrical and optical crosstalk) is characterized by the penalty of receiver sensitivity curve. The 10 Gbps NRZ $2^{31}-1$ PRBS electrical and optical signals are used for this experiment.

For the transmitter, 3 pairs of differential signals are fed into three adjacent channels with longest differential lines, channels 9, 10 and 11, and the BER curves are measured and shown in Fig. 13 left panel. Comparing with one channel, the observed power penalty is 0.1 dB. The effect of crosstalk can be neglected, since the power penalty is within the measurement error.

In receiver crosstalk testing, we measured the BER curves of channel 10 by an error detector, while feeding optical signals to one and two adjacent channels. The optical signals are generated by a CXP module controlled by a standard switch ASIC. As shown in Fig. 13, right panel, there is a 0.4 dB power penalty, if two adjacent channels (CH10, CH11) are working together. There is an additional 0.4 dB power penalty, if channel 9 (CH9) is turned on. The cross talk penalty may be due to the distortion of adjacent differential trace, since they are terminated with $50 \, \Omega$ resistance during testing. The possible addition of ground planes between channels may improve the performance. We further generated and fed more optical signals into other channels, and there is no further impact on the tested channel.

VI. THERMAL CHARACTERIZATION

To validate the thermal isolation of the air gap, the temperature values of the VCSEL array and CMOS driver are tested. For the VCSEL, since the peak value of the output wavelength is linearly changing with the temperature [22], the temperature increase can be calculated from wavelength shift. The temperature of the CMOS driver is tested from the top surface by attaching a thermistor to it.

Firstly, the wavelength shift as a function of temperature is measured using a similar VCSEL array. The VCSEL array is placed on the plate of flip chip bonder, on which the temperature can be controlled precisely, with the range from 40 °C to 250 °C. An optical connector, which is connected with fibers, is clamped and aligned. A single VCSEL is powered by two probes, and the optical output spectrum is analyzed using a spectrum analyzer. The different emitted wavelengths are monitored while the temperature is changed from room temperature (22 °C) to 70 °C. The test results are shown in Fig. 14. Five peaks are recorded, the average values (nearby central wavelength) are linear fitted with temperature, showing a wavelength shift of 0.06543 nm/°C.

![Fig. 14. The temperature dependence of the VCSEL emission lines. The linear fitting shows a slope of 0.06543 nm/°C.](image)

Using the information obtained on a stand alone VCSEL, the temperature value of the embedded VCSEL can now be derived by monitoring the wavelength changes. We perform the test on the same probe station, and the assembled transmitter is placed on an aluminum cylinder carrier (diameter 600 mm, height 10 mm), contacting the same area shown in scheme in Fig. 1. Since the volume of aluminum is larger than the simulated copper heat-sinks in section III, the carrier exhibits much better heat transferring. The 12 VCSELs are switched on through the CMOS driver, and the output of the VCSEL array is fed into the same spectrum analyzer. Since there’s no high speed data input during this thermal characterization, the power consumption of the module is lower than the maximum consumption and is measured to be 0.48 W. The changes of peak wavelength is 0.11 nm between the starting temperature (21.5 °C) and the stable temperature, which indicate 1.7 °C increase. The temperature of the VCSEL is stable at 23.2 °C, when the thermistor shows the temperature of the CMOS driver is 25.0 °C. The thermal characterization shows 1.8 °C difference between the CMOS driver and the VCSEL array, due to the effect of thermal isolation. This effect will be more obvious, if the chips work at higher temperature under full loading conditions, as anticipated by the thermal simulations shown in section III.
VII. CONCLUSION

In this paper, opto-electronic dies and CMOS ICs have been packaged by a novel 3D packaging scheme. A 3-level silicon interposer is fabricated with semiconductor technology and deeply wet etching of silicon. The electrical connections are designed for 12-channel parallel optical transceiver, and very short traces between dies are achieved by routing through the etched face. 10 Gbps transmitter and receiver have been assembled with an air gap. The opto-electronic die in this new packaging concept is shown using simulation to experience similar conditions as those obtainable using the 2.5D package concept yet with higher density. The simulation results show the temperature of optics is 3.8 °C lower than CMOS, which indicate that good thermal decoupling is obtained. The actual temperature of the working module is also tested and shows to support a lower operating temperature for the embedded VCSEL array compared to the CMOS driver. This proposed 3D scheme exhibits therefore a thermal advantage over conventional 3D stacking approaches.

A standard optical connector is included in the module, which is connected with break out fiber for testing purposes. Both transmitter and receiver assemblies have uniform performance. All of 12 channels show similar sensitivity, with a maximum 1 dB spread between channels for both transmitter and receiver. Clear and uniform eye patterns are captured at 10 Gbps and 15 Gbps. Finally, only limited crosstalk is measured 0.1 dB and 0.8 dB power penalty for the transmitter and receiver respectively.

This 3D embedding platform, with thermal advantages and advanced RF performance, can be used for heterogeneous integration and opto-electronic packaging. In the future, higher data rate chips will be packaged to fulfill 400 Gbps (25 Gbps × 16 or 50 Gbps × 8) data transmission for next generation optical interconnection.

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