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Speeding up the simulation of periodic circuits

Circuit miniaturization (Moore's law) and diversification are common trends in the electronics world. These imply high-volume, power-efficient integrated circuit designs, all while increasing performance like faster computations, or extended battery life of portable devices. As a consequence of that the verification process – quality assessment of the circuits before manufacturing – becomes increasingly complex. To enable new technologies on the market in short time, a reliable, accurate and fast transistor-level simulation (so-called SPICE) is a key factor.

A SPICE (Simulation Program with Integrated Circuit Emphasis)-like simulator is composed of a set of numerical methods to perform such simulations on a mathemathical model representing the circuit. In recent years the electronic industry demands for advanced mathematical methods that increase the simulation speed of such simulators while keeping high accuracy. This dissertation deals with speeding up simulations of a certain class of periodic circuits, namely PLL, DLL and SMPSs. These have different applications in the real world, such as telecommunication, clock generation and power supply. They have a very long simulation time (weeks or even months) when current numerical methods are adopted, due to the strongly nonlinear behavior they have at start-up.

This dissertation presents two main contributions. First, a novel methodology for industrial integer-N PLLs for noise-free and device noise analyses was developed, speeding up their simulations with respect to brute-force numerical integration while accurately extracting all the PLL's factors of interest. The unifying, fast and accurate method is non-invasive for simulators equipped with techniques well known in the circuit simulation community, such that it could be implemented with little efforts.

Second, a comparison is made of the robustness of two techniques meant to accelerate the computation of the periodic steady-state solution (SST) when applied to industrial DLLs and SMPSs**.** Preliminary experiments show that the two techniques have numerical issues when applied to the circuits under analysis, which makes them ineffective and unreliable in some cases. We understand that the numerical errors coming from the numerical integration are amplified when an acceleration technique is used. Thus, we advise to keep these error low by increasing the accuracy of the computation of the solutions during the integration. We also proposed to use multiple methods in a "parallel" fashion to compute the SST, and pick the one with the lowest amplification factor.

Title of PhD-thesis: Advanced Numerical Methods for Simulating Non-Autonomous Periodic Strongly Nonlinear Circuits. Supervisors: W.H.A. Schilders (TU Eindhoven, NL), P. Bolcato (Mentor Graphics, Grenoble, FR)