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Aanstellingen

Onderzoeker
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Electronic Systems
Technische Universiteit Eindhoven
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1 feb. 2015 → 21 jul. 2020

Student, Computer Science
Student, Automated test control block generation and minimization.
Mathematics and Computer Science
Technische Universiteit Eindhoven
1 sep. 1984 → 14 mrt. 1992

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Electronic Systems
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Lecturer
High Tech Institute
Nederland
1 jan. 2016 → present

Principal Scientist
1imec
Hasselt, België
1 okt. 2008 → present

Senior Principal Scientist

NXP Semiconductors
Eindhoven, Nederland
1 aug. 2006 → 30 sep. 2008

Principal Scientist
Philips Research Laboratories
Eindhoven, Nederland
1 mrt. 1992 → 31 jul. 2006

Onderzoeksoutput

A Bypassable Scan Flip-Flop for Low Power Testing with Data Retention Capability
Cao, X., Jiao, H. & Marinissen, E. J., 1 feb. 2022, In: IEEE Transactions on Circuits and Systems II: Express Briefs. 69, 2, blz. 554-558 5 blz., 9481937.

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Podpod, A., Velenis, D., Phommahaxay, A., Bex, P., Fodor, F., Marinissen, E. J., Rebibis, K. J., Miller, A., Beyer, G. & Beyne, E., 25 okt. 2018, *2018 International Wafer Level Packaging Conference, IWLPC 2018.* Piscataway: Institute of Electrical and Electronics Engineers, 5 blz. 8573262

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Corrections
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Minas, N. & Marinissen, E. J., 2 feb. 2012, IPC-nummer G01R 27/ 02 A I, Octrooi Nr. US2012025846, Prioriteitsdatum 29 jul. 2011, Prioriteitsnummer US201113194818

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On scan chain diagnosis for intermittent faults
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Guest Editors' introduction: the status of IEEE Std 1500
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Marinissen, E. J. & Nicolici, N., nov. 2007, In: IET Computers and Digital Techniques. 1, 6, blz. 659-660

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30/05/17
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imec, TU Eindhoven, and Cadence - Advances in Defect Location Identification
Zhan Gao & Erik Jan Marinissen
30/05/19
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imec, TU Eindhoven, and Cadence – Advances in Defect Location Identification
Zhan Gao, Santosh Malagi, Erik Jan Marinissen, Joe Swenton, Jos Huisken & Kees Goossens
7/05/19
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Intel Joins CHIPS Alliance; 3D Stack Testing Standardized
Erik Jan Marinissen
3/03/20
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Leila De Floriani Voted 2019 IEEE Computer Society President-Elect
Erik Jan Marinissen
2/10/18
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Micro-scale pre-bond probe array automates tests for chips to be stacked
Erik Jan Marinissen
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New Solution for Testing Chips Prior to 3D Stacking
Erik Jan Marinissen
21/08/17
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New Solution for Testing Chips Prior to 3D Stacking
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New Standard Allows Stacked Dies in 3D ICs to Connect with Test Equipment
Erik Jan Marinissen
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New standard allows stacked dies in 3D integrated circuits to connect with test equipment
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New Standard Allows Stacked Dies in 3D Integrated Circuits to Connect with Test Equipment
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Pre-bond testing development hikes 3D chip yields
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Stacked dies to connect with test equipment
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Stacked package standard for IEEE Xplore Digital Library
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Test Access Opened to Every Die in 3D IC Stack
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Testing stacked dies in 3D integrated circuits
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