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Wideband Data Converters
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Quote

"As long as society relies on digital electronics, technologies for analog-to-digital conversion and vice versa are unavoidably necessary – in particular in the communication domain, where society will always need higher speeds for lower costs."

Aanstellingen

Universitair Docent

Universitair Docent
Integrated Circuits
Technische Universiteit Eindhoven
Eindhoven, Nederland
15 feb. 2009 → 30 jun. 2012

Promovendus

Promovendus
Integrated Circuits
Technische Universiteit Eindhoven
Eindhoven, Nederland
1 sep. 2008 → 14 feb. 2009

Promovendus

Promovendus
Integrated Circuits
Technische Universiteit Eindhoven
Eindhoven, Nederland
1 sep. 2004 → 14 feb. 2009

Onbekend

onbekend
Integrated Circuits
Technische Universiteit Eindhoven
Eindhoven, Nederland
1 jan. 2003 → 31 aug. 2004

Universitair Docent

Universitair Docent
Integrated Circuits
Technische Universiteit Eindhoven
Eindhoven, Nederland
1 jul. 2012 → 21 jul. 2020

Wideband Data Converters

Technische Universiteit Eindhoven
Eindhoven, Nederland
1 sep. 2004 → present

Center for Astronomical Instrumentation

Technische Universiteit Eindhoven
Eindhoven, Nederland
1 jul. 2019 → present

Student, Information and Communication Technology

Student, 12bit self-calibrated DAC
Electrical Engineering
Technische Universiteit Eindhoven
1 feb. 2002 → 1 feb. 2004

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Integrated Circuits
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1 jan. 2020 → 14 apr. 2021

Universitair Docent

Universitair Docent
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Technische Universiteit Eindhoven
Eindhoven, Nederland
5 mrt. 2021 → 3 apr. 2022

Universitair Hoofddocent

Universitair Hoofddocent
Integrated Circuits
Technische Universiteit Eindhoven
Eindhoven, Nederland
1 feb. 2022 → present

Onderzoeksoutput

Systems and methods for processing errors in digital beamforming receivers

Athanasiadis, P., Doris, K., Neofytou, M. & Radulov, G. I., 14 apr. 2022, Octrooi Nr. US20220113373, 13 okt. 2020

A 5GS/s 360MHz-BW 68dB-DR Continuous-Time 1-1-1 Filtering MASH $\Delta\Sigma$ ADC in 40nm CMOS

Liu, Q., Breems, L., Zhang, C., Bajoria, S., Bolatkale, M., Rutten, R. & Radulov, G., 17 mrt. 2022, *2022 IEEE International Solid-State Circuits Conference (ISSCC 2022)*. Institute of Electrical and Electronics Engineers, blz. 414-416 3 blz. 9731789

Systems and methods for calibration of in-phase/quadrature (I/Q) modulators

Neofytou, M., Doris, K., Ganzerli, M., Radulov, G. I. & Athanasiadis, P., 18 jan. 2022, Octrooi Nr. US11228478, 13 okt. 2020, Prioriteitsnummer US202017069669 20201013

Sub-Milliwatt Transceiver IC for Transcutaneous Communication of an Intracortical Visual Prosthesis

Omisakin, A., Radulov, G., Mestrom, R. & Bentum, M., 1 jan. 2022, In: *Electronics*. 11, 1, 20 blz., 24.

A 6GS/s 0.5GHz BW continuous-time 2-1-1 MASH $\Delta\Sigma$ modulator with phase-boosted current-mode ELD compensation in 40nm CMOS

Zhang, C., Breems, L., Liu, Q., Radulov, G., Bolatkale, M., Bajoria, S., Rutten, R. & Van Roermund, A. H. M., 26 okt. 2021, *ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC)*. Institute of Electrical and Electronics Engineers, blz. 491-494 4 blz. 9567777

A novel 2-Dimensional correction method for mm-Wave Cartesian I/Q Modulators

Neofytou, M., Athanasiadis, P., Ganzerli, M., Lont, M., Radulov, G. I. & Doris, K., 27 apr. 2021, *2021 IEEE International Symposium on Circuits and Systems, ISCAS 2021 - Proceedings*. IEEE/LEOS, 5 blz. 9401408

Time Interleaved ADC mismatch error correction technique in I/Q Digital Beamforming Receivers

Athanasiadis, P., Neofytou, M., Ganzerli, M., Radulov, G. I. & Doris, K., 27 apr. 2021, *2021 IEEE International Symposium on Circuits and Systems, ISCAS 2021 - Proceedings*. Institute of Electrical and Electronics Engineers, blz. 1-5 5 blz. 9401645

Analysis of Time-Interleaved ADC Offset and Gain Mismatch Errors in PMCW Radar

Rosenmuller, D., Doris, K., Radulov, G. & Matters-Kammerer, M., 3 feb. 2021, *2020 17th European Radar Conference (EuRAD)*. Institute of Electrical and Electronics Engineers, blz. 434-437 4 blz. 9337377

A 0.037mm² 1GSps 12b self-calibrated 40nm CMOS DAC cell with SFDR>60dB up to 200MHz and IM3 < -60dB up to 350MHz

Radulov, G. I. & Quinn, P., 9 okt. 2020, *ECCTD 2020 - 24th IEEE European Conference on Circuit Theory and Design*. Institute of Electrical and Electronics Engineers, 4 blz. 9218326

Analysis of the inter-stage signal leakage in wide BW low OSR and high DR CT MASH $\Delta\Sigma$

Liu, Q., Breems, L. J., Bajoria, S., Bolatkale, M., Zhang, C. & Radulov, G. I., 28 sep. 2020, *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. Institute of Electrical and Electronics Engineers, 5 blz. 9180951

A novel analysis of the beam squinting in wideband phased array digital I/Q transmitters

Manev, V., Neofytou, M., Radulov, G. & Doris, K., sep. 2020, *ECCTD 2020 - 24th IEEE European Conference on Circuit Theory and Design*. Institute of Electrical and Electronics Engineers, 4 blz. 9218366

Novel Baseband Analog Beamforming through Resistive DACs and Sigma Delta Modulators

Ringeling, S., Steinebach, L., Liu, Q., Zhang, C., Bajoria, S., Bolatkale, M., Breems, L. & Radulov, G., sep. 2020, *ECCTD 2020 - 24th IEEE European Conference on Circuit Theory and Design*. Institute of Electrical and Electronics Engineers, 4 blz. 9218408

A 1.9 mW 250 MHz Bandwidth Continuous-Time $\Sigma\Delta$ Modulator for Ultra-Wideband Applications

Neofytou, M., Zhou, M., Bolatkale, M., Liu, Q., Zhang, C., Radulov, G., Baltus, P. & Breems, L., 26 apr. 2018, *2018 IEEE International Symposium on Circuits and Systems, ISCAS 2018 - Proceedings*. Piscataway: Institute of Electrical and Electronics Engineers, 5 blz. 8351046

A 2 GHz 0.98 mW 4-bit SAR-based quantizer with ELD compensation in an UWB CT $\Sigma\Delta$ modulator

Zhou, M., Neofytou, M., Bolatkale, M., Liu, Q., Zhang, C., Cenci, P., Radulov, G., Baltus, P. & Breems, L., 26 apr. 2018, *2018 IEEE International Symposium on Circuits and Systems, ISCAS 2018 - Proceedings*. Piscataway: Institute of Electrical and Electronics Engineers, 5 blz. 8350889

Current-mode multi-path excess loop delay compensation for GHz sampling CT $\Sigma\Delta$ ADCs

Zhang, C., Breems, L. J., Radulov, G. I., Bolatkale, M., Liu, Q., Hegt, J. A. & van Roermund, A. H. M., 29 mei 2017, *IEEE International Symposium on Circuits and Systems*. Piscataway: Institute of Electrical and Electronics Engineers, blz. 547-550 4 blz. 8050369

High-speed linear digital-to-analog converters

van Roermund, A. H. M. & Radulov, G. I., 9 feb. 2017.

A digital calibration technique for wide-band CT MASH $\Sigma\Delta$ ADCs with relaxed filter requirements

Zhang, C., Breems, L. J., Radulov, G. I., Bolatkale, M., Hegt, J. A. & van Roermund, A. H. M., 24 mei 2016, *IEEE International Symposium on Circuits and Systems 2016 (ISCAS), 22-25 May 2016, Montreal, Canada*. Piscataway: Institute of Electrical and Electronics Engineers, blz. 1486-1489

A wideband RF mixing-DAC achieving $IMD < -82$ dBc up to 1.9 GHz

Bechthum, E., Radulov, G. I., Briaire, J., Geelen, G. J. G. M. & van Roermund, A. H. M., 16 mei 2016, In: IEEE Journal of Solid-State Circuits. 51, 6, blz. 1374-1384 11 blz.

A Design Methodology for Wide-Band Continuous-Time MASH $\Sigma\Delta$ ADC Architectures

Zhang, C., Breems, L. J., Radulov, G. I., Hegt, J. A. & van Roermund, A. H. M., 22 mrt. 2016.

Classification for synthesis of high spectral purity current-steering mixing-DAC architectures

Bechthum, E., Radulov, G. I., Briaire, J., Geelen, G. & Roermund, van, A. H. M., 1 dec. 2015, In: Analog Integrated Circuits and Signal Processing. 85, 3, blz. 497-504 8 blz.

Comparison of the implementation options of a summation function in high speed continuous-time sigma-delta ADCs

Zhang, C., Xin, H., Radulov, G., Breems, L., Hegt, H. & van Roermund, A. H. M., 24 mrt. 2015.

A 28-nm CMOS 1 V 3.5 GS/s 6-bit DAC with signal-independent delta-I noise DfT scheme

Radulov, G. I., Quinn, J. A. & Roermund, van, A. H. M., 2015, In: IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 23, 1, blz. 44-53 10 blz.

A 28-nm CMOS 7-GS/s 6-bit DAC with DfT clock and memory reaching SFDR > 50 dB Up to 1 GHz

Radulov, G. I., Quinn, P. J. & Roermund, van, A. H. M., 2015, In: IEEE Transactions on Very Large Scale Integration (VLSI) Systems. 23, 9, blz. 1941-1945 5 blz.

A 5.3 GHz 16b 1.75 GS/S wideband RF mixing-DAC achieving IMD

Bechthum, E., Radulov, G. I., Briaire, J., Geelen, B. & Roermund, van, A. H. M., 2015, *2015 IEEE International Solid-State Circuits Conference (ISSCC), 22-26 Februar 2015, San Francisco*. Piscataway: Institute of Electrical and Electronics Engineers, blz. 1-3

A novel timing-error based approach for high speed highly linear Mixing-DAC architectures

Bechthum, E., Radulov, G. I., Briaire, J., Geelen, G. & Roermund, van, A. H. M., 2014, *Proceedings of the 2014 IEEE International Symposium on Circuits and Systems (ISCAS 2014), 1-5 June 2014, Melbourne, Australia*. Piscataway: Institute of Electrical and Electronics Engineers, blz. 942-945

Methods and systems for high frequency clock distribution

Radulov, G. I. & Quinn, P. J., 22 okt. 2013, Octrooi Nr. 8564330

Integrated test support features for multi-GHz DACs in 28nm CMOS

Quinn, P., Radulov, G. I. & van Roermund, A. H. M., 13 sep. 2013, *TVHSAC: IEEE International Workshop on Test and Validation of High Speed Analog Circuits Anaheim, CA, USA*. 3 blz.

A novel output transformer based highly linear RF-DAC architecture

Bechthum, E., Radulov, G. I., Briaire, J., Geelen, G. & Roermund, van, A. H. M., 2013, *Proceedings of the 21st European Conference on Circuit Theory and Design (ECCTD 2013), 8-12 September 2013, Dresden, Germany*. blz. 1-4

Challenges in high-speed single-bit continuous-time $\Sigma\Delta$ analog-to-digital converters

Meuleman, G., Zhang, C., Radulov, G. I., Breems, L. J. & Roermund, van, A. H. M., 2013.

High-resolution continuous-time sigma-delta converters with multi-Bbit quantization

Zhang, C., Meuleman, G., Radulov, G. I., Breems, L. J. & Roermund, van, A. H. M., 2013.

Automatic generation of layout of arrays of current sources and capacitors

Balmaekers, B. M., Harpe, P. J. A. & Radulov, G. I., 2012, *Proceedings of ICT.Open 2012, 22-23 October 2012, Rotterdam, The Netherlands*. Rotterdam: NWO

Systematic analysis of the impact of mixing locality on Mixing-DAC linearity for multicarrier GSM

Bechthum, E., Radulov, G. I., Briaire, J., Geelen, G. & Roermund, van, A. H. M., 2012, *Presentation at the 2012 IEEE International Symposium on Circuits and Systems (ISCAS 2012), May 20-23, 2012, Seoul, Korea*. Piscataway: Institute of Electrical and Electronics Engineers, blz. 241-244

A novel temperature and disturbance insensitive DAC calibration method

Bechthum, E., Radulov, G. I. & Roermund, van, A. H. M., 2011, *Proceedings of the 2011 International Symposium on Circuits and Systems (ISCAS), 15 - 18 May 2011, Rio de Janeiro, Brazil*. Piscataway: Institute of Electrical and Electronics Engineers, blz. 2003-2006

A temperature and disturbance insensitive calibration method for high speed digital to analog converters

Bechthum, E., Radulov, G. I. & Roermund, van, A. H. M., 2011, *Proceedings of the interface for dutch ICT-research(ICT.OPEN), 14-15 November 2011, Veldhoven, Netherlands*. blz. 1-6

Smart and flexible digital-to-analog converters

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Roermund, van, A. H. M., 2011, Dordrecht: Springer. 309 blz. (Analog circuits and signal processing series)

Flexible and self-calibrating current-steering digital-to-analog converters : analysis, classification and design

Radulov, G. I., 2010, Eindhoven: Technische Universiteit Eindhoven. 289 blz.

Calibration of current-steering D/A Converters

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Roermund, van, A. H. M., 2009, *Proceedings of Analog/Mixed-signal Innovation Network "Digitally Assisted Analogue", 22nd October 2009, Dublin, Ireland*. blz. 1-26

DAC correction and flexibility, classification, new methods and designs

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Roermund, van, A. H. M., 2009, *Analog Circuit Design - Smart Data Converters, Filters on Chip, Multimode Transmitters*. Roermund, van, A. H. M., Steyaert, M. & Casier, H. J. (redacties). Dordrecht: Springer, blz. 79-105 342 blz.

Functionals of Brownian bridges arising in the current mismatch in D/A converters

Heydenreich, M. O., Hofstad, van der, R. W. & Radulov, G. I., 2009, In: *Probability in the Engineering and Informational Sciences*. 23, 1, blz. 149-172 24 blz.

Smart and flexible DACs, classification and design

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Roermund, van, A. H. M., 2009, *Proceedings of Advances in Analog Circuit Design, AACD 2009, March 31-April 2, 2009, Lund, Sweden*.

Smart front-ends, from vision to design

Roermund, van, A. H. M., Baltus, P. G. M., Bezooijen, van, A., Hegt, J. A., Lopelli, E., Mahmoudi, R., Radulov, G. I. & Vidojkovic - Andjelovic, M., 2009, In: *IEICE Transactions on Electronics*. E92.C, 6, blz. 747-756 10 blz.

Method and apparatus for calibrating a scaled current electronic circuit

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Roermund, van, A. H. M., 16 dec. 2008, Octrooi Nr. US7466252

A flexible 12-bits self-calibrated quad-core current-steering DAC

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Roermund, van, A. H. M., 2008, *2008 IEEE Asia Pacific Conference on Circuits and Systems - Macau - China*.

Brownian-bridge-based statistical analysis of DAC INL caused by current mismatch

Radulov, G. I., Heydenreich, M. O., Hofstad, van der, R. W., Hegt, J. A. & Roermund, van, A. H. M., 2007, In: *IEEE Transactions on Circuits and Systems II: Express Briefs*. 54, 2, blz. 146-150

Parallel current-steering D/A Converters for flexibility and smartness

Radulov, G. I., Quinn, P. J., Harpe, P. J. A., Hegt, J. A. & Roermund, van, A. H. M., 2007, *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2007) 27 - 30 May 2007, New Orleans, Louisiana, USA*. Piscataway, New Jersey, USA: Institute of Electrical and Electronics Engineers, blz. 1465-1468

Parallel current-steering D/A Converters for flexibility and smartness

Radulov, G. I., Quinn, P. J., Harpe, P. J. A., Hegt, J. A. & Roermund, van, A. H. M., 2007, *proceeding of ProRISC 2007*.

Method and Apparatus for Calibrating A Current -Based Circuit

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Roermund, van, A. H. M., 11 jul. 2006, Octrooi Nr. 7076384

A binary-to-thermometer decoder with built-in redundancy for improved DAC Yield

Radulov, G. I., Quinn, P. J., Beek, van, P. C. W., Hegt, J. A. & Roermund, van, A. H. M., 2006, *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2006) 21 - 24 May 2006, Island of Kos, Greece*. Piscataway, New Jersey, USA: Institute of Electrical and Electronics Engineers

A binary-to-thermometer decoder with redundant switching sequences

Radulov, G. I., Quinn, P. J., Beek, van, P. C. W., Hegt, J. A. & Roermund, van, A. H. M., 2006, *Proceedings of the 17th ProRISC, Annual Workshop on Circuits, Systems and Signal Processing (ProRISC 2006) 23 - 24 November 2006, Veldhoven, the Netherlands*. Utrecht, the Netherlands: Technology Foundation, blz. 1414-1417

Functionals of Brownian bridges arising in the current mismatch in D/A-converters

Heydenreich, M. O., Hofstad, van der, R. W. & Radulov, G. I., 2006, Eindhoven: Eurandom. 21 blz. (Report Eurandom; vol. 2006016)

A start-up calibration method for generic current-steering D/A converters with optimal area solution

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Van Roermund, A. H. M., 1 dec. 2005, *2005 IEEE International Symposium on Circuits and Systems*. Piscataway: Institute of Electrical and Electronics Engineers, blz. 788-791 4 blz.

An On-Chip Self-Calibration Method for Current Mismatch in D/A Converters

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Roermund, van, A. H. M., 2005, *ESSCIRC 2005*. blz. 169-172

A Parallel Current-steering DAC Architecture for Flexible and Improved Performance

van den Hoven, R. A. T., Radulov, G. I., Hegt, J. A. & Roermund, van, A. H. M., 2005, *ProRisc 2005*.

Smart AD and DA Converters

Roermund, van, A. H. M., Hegt, J. A., Harpe, P. J. A., Radulov, G. I., Zaniopoulos, A., Doris, K. & Quinn, P. J., 2005, *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS 2005) 23 - 26 May 2005, Kobe, Japan*. Piscataway, New Jersey, USA: Institute of Electrical and Electronics Engineers, Vol. 4. blz. 4062-4065

A Calibration Algorithm for current-steering DACs with Relaxed design requirements

Radulov, G. I., Hegt, J. A., Quinn, P. J. & Roermund, van, A. H. M., 2004, *Proceedings of the 9th Biennial Baltic Electronics Conference 3-6 October, Tallin, Estonia*. blz. 105-108

A New Current Calibration Scheme Suitable for Generic DAC Architectures

Radulov, G. I., Hegt, J. A., Quinn, P. J. & Roermund, van, A. H. M., 2004, *Proceedings of the 15th ProRISC, Annual Workshop on Circuits, Systems and Signal Processing (ProRISC 2004) 25 - 26 November 2004, Veldhoven, the Netherlands*. Utrecht, the Netherlands: STW Technology Foundation, blz. 577-584

A Self-calibrating current-steering 12-bit DAC based on new 1-bit self-test scheme

Radulov, G. I., Quinn, P. J., Hegt, J. A. & Roermund, van, A., 2004, *Proceedings of the IEEE IC Test Workshop 2004, 13-14 September 2004, Limerick, Ireland*. blz. 49-54

Design of a calibrated 12-bit current-steering Digital-to-Analog Converter

Radulov, G. I., 2004, Eindhoven: Technische Universiteit Eindhoven. Stan Ackermans Instituut.

Courses

Electronic circuits 2

Electronics: selected topics

Semiconductor physics and materials

Data converters 2: design

Advanced CMOS design